# Matlab Use in Design of Digital Systems on the FPGA in CAD Xilinx VIVADO

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*Abstract*—Matlab is a high-level language and an interactive environment that can help to analyze data, develop algorithms, create models and applications. There are many extensions for Matlab. One of these extensions is the Xilinx System Generator for DSP, a key component of the Xilinx specialized digital signal processing platform, that allows to implement DSP algorithms with less time costs than traditional RTL design.

### Keywords—MATLAB, VHDL, XILINX, VIVADO.

## I. INTRODUCTION

Matlab is a high-level language and an interactive environment for programming, numerical calculations, visualization of results, technical calculations. Has a large number of packages of application extensions. With Matlab you can analyze data, develop algorithms, create models and applications.

Matlab is widely used in the following areas:

- working of signals and communications;
- image and video processing;
- system of management;
- automation of testing and measurements, and so on.

The Matlab system consists of the following main parts:

MATLAB matrix (matrix and array language);

- MATLAB environment;
- controlling graphics (high-level teams for visualizing two- and three-dimensional data, etc.);
- built libraries and numerous extensions packages (including Simulink);
- program interface (a library that allows you to use programs in C and Fortran that interact with MATLAB).

For Matlab there are many extensions (Toolboxes and Blocksets) for different industries. One of these extensions is the Xilinx System Generator for DSP, a key component of the Xilinx specialized digital signal processing platform (DSP).

# II. MATLAB XILINX DSP SYSTEM GENERATOR

System Generator for DSP is the industry-leading tool for developing high-performance digital signal processing systems built by Xilinx's FPGA and SoC. System Generator for DSP allows you to implement DSP algorithms with less time costs than traditional RTL design.

System Generator for DSP provides:

- the development of high-performance parallel systems on the most advanced FPGA;
- system simulation and automatic code generation from Simulink and MATLAB;
- integration of RTL code, IP modules, MATLAB codes and hardware components into the DSP system.

System Generator for DSP is included in the Vivado System Edition. Using System Generator for DSP developers with small design experience allows to quickly create highquality DSP projects at a lower cost compared to traditional RTL design.

Simulink System Generator for DSP allows the developer to access the set of Xilinx FPGA hardware components and, at the same time, can use standard Simulink units such as signal sources and receivers, logic and math operations, subsystem blocks, and more. And System Generator libraries contain blocks that represent elements of communication, logic management, signal processing, memory work, and built-in microprocessor devices, and more.

# III. FEATURES AND BENEFITS OF SYSTEM GENERATOR FOR DSP

Key Features and Benefits of System Generator for DSP:

#### A. DSP simulation

DSP-simulation. Creating and debugging highperformance DSP systems using optimized RTL IP addresses of Xilinx as blocks in Simulink for signal processing (eg FIR, FFT filters), error correction (for example, Viterbi decoder, Reed-Solomon encoder / decoder), arithmetic, memory such as FIFO, RAM, ROM, and digital logic. Allows access to Simulink's DSP48 primitives for high frequencies.

## B. Bit and cyclic realization with floating and fixed-point

Bit and cyclic implementation with floating and fixedpoint. The system generator supports bitwise and cyclic precision with fixed point and bit and clock accuracy with single, dual and user-defined floating-point accuracy.

# C. Automatic generation of code VHDL or Verilog, or Packaged IP from Simulink

Automatic generation of VHDL or Verilog code, or Packaged IP from Simulink. Implementation of behavioral (RTL) generation and targeting to specific Xilinx IP cores with Xilinx Blockset. Pack the project as an IP kernel, which can be added to the Vivado IP directory for use in another project, allowing you to reuse the design and share the developed model.

### D. Hardware co-simulation

Hardware common simulation. The code generation option, which allows validation and acceleration of simulation by compiling projects into FPGA hardware, which can be used in a Simulink simulation loop to test the running equipment and simulink simulation acceleration. System Generator supports Ethernet (10/100 / Gigabit) and JTAG communications between the hardware platform and Simulink for supported platforms and platforms.

## E. Strings and resource analysis

Track and analysis of resources. Checking the synchronization closure and use of resources of your projects (after synthesis or after implementation) and mapping the results with the Model Generator system into Simulink through cross-sensing speeds up the process of project refinement, which increases productivity or detects synchronization failures.

Integrated with Kintex®-7, Virtex®-7, Zynq®-7000, Artix®-7, Kintex UltraScale <sup>TM</sup>, Kintex UltraScale +, Virtex UltraScale, Virtex UltraScale +, Zynq UltraScale + RFSoC.

# IV. CONCLUSIONS

Using System Generator, that included in the Vivado System Edition for DSP, allows for developers with small design experience, to quickly create high-quality DSP projects at a lower cost compared to traditional RTL design.

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