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There proceedings depict: mathematical modeling of information signals and systems; hardware description languages; systems of computer aided design of devices on microcontrollers, microprocessors and FPGAs; features of device development on microcontrollers and microprocessors; aspects of the development of devices in the FPGA; architecture and microarchitecture of specialized computing systems; modern trends in the design of microprocessor technology; the problem of improving the quality of training specialists.

Papers are presented in authors' edition.

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Experience of Developing a Laboratory Base for the Study of Modern Microprocessor Systems

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***Abstract*—A laboratory workshop was developed, consisting of a series of works aimed at studying and studying the principles of microcontroller programming, practical implementation of interaction with sensors, organization of work with input / output devices, and development of interface devices. By changing sensors that are connected to laboratory mockups or real equipment, and reprogramming the micro-controller system, you can perform laboratory work on almost all engineering profile courses.**

Keywords—programming, microcontrollers, sensors, interface devices, layouts.

I. INTRODUCTION

The study of modern microprocessor systems and programmable logic integrated circuits cannot be qualitative without a laboratory base, which allows the student to develop practical skills and teach him to work with a real hardware, not computer simulators [1, 2]. Therefore, the authors' team developed a laboratory workshop consisting of a cycle of works aimed at studying and studying the principles of microcontroller programming, practical implementation of interaction with sensors, organization of work with information input / output devices and development of interface devices [1, 3]. By changing sensors that are connected to laboratory mockups or real equipment, and reprogramming the microcontroller system, you can perform laboratory work on almost all engineering profile courses [4], for example, when training specialists in the field of biomedical engineering [5, 6] to develop modern medical appointments [7, 8].

II. SCOPE OF THE DEVELOPED LAYOUTS

These devices can be used (and are already used) as a laboratory base for basic disciplines related to the study of digital and microprocessor technology, and in special technical disciplines courses aimed at studying the principles of operation and the development of real microprocessor-controlled devices [9 – 11].

Principles are being developed for the implementation of remote laboratory work. The main disciplines in which this laboratory base is already used are: “Digital devices and microprocessors”, “Microprocessor technology”, “Circuit design of microelectronic devices”, “Automation of designing electronic devices and systems”, “Designing specialized devices on microchips of grammable logic","Application of microprocessor systems in medical equipment ","Application of microprocessor systems in home appliances","Pairing microprocessor systems with external devices" et al. Consider in more detail designed laboratory equipment.

III. TECHNICAL CHARACTERISTICS OF ML-1

The ML-1 laboratory layout for studying micro-controller control systems allows you to create flexible technical solutions for the development of digital devices with embedded control systems of low and medium levels of complexity and can be used in a wide range of household and medical devices, security systems, etc. The layout includes: the most common in Ukraine multifunctional 8-bit microcontroller by ATMEL AVR ATMEGA-128, an 8-bit LED display unit, user-programmable keys and a 4x3 matrix keyboard, additional 32 Mbit Flash-RAM external memory modules , DATA RAM 32K, 10-position Holtek HT-10 digital indicator, monochrome graphic display 240x128 LCD EPSON, RS-232 serial interface, 12-bit ADC and DAC modules, an external connector that allows you to connect non-standard devices, actuators and sensors iki. The microcontroller is programmed via the ISP programmer, JTAGICE interface with a debugger. The appearance of the laboratory layout is shown in Figure 1.

Fig. 1. ML-1 laboratory model.

IV. TECHNICAL CHARACTERISTICS OF ML-2

Laboratory layout ML-2 is designed to study the principles of the development of digital devices based on programmable logic chips. This model is used in disciplines that study digital circuitry and address issues related to the development of complete, full-featured digital devices and

systems of high complexity, such as audio / video processors, modules for digital signal processing. The layout includes: FPGA (programmable logic integrated circuit), type FPGA by Altera ACEX EP1K100QC208, operating at 50 MHz, auxiliary microcontroller AT-Mega-128, additional memory block of 32 MB Flash RAM, EPSON 320x240 LCD display, video D / A 80 MHz, user-programmable LED modules, external high-power and keyboard; supports USB 2.0, RS-232 and PS / 2 interfaces. Multiple FPGA configuration modes are supported: upload via USB interface, boot using Byte-Blaster, boot using Flash RAM, boot using an AVR microcontroller. The appearance of the laboratory model ML-2 is shown in Figure 2.

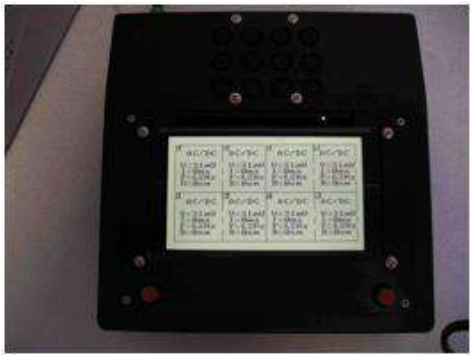

Fig. 2. ML-2 laboratory model.

V. TECHNICAL CHARACTERISTICS OF ML-3

Laboratory Layout ML-3 is designed to study the architecture of high-performance ARM microcontrollers. The structure of the ML-3 includes: ARM microcontroller company PHILIPS LPC-2106, operating at 50 MHz, LCD display with a resolution of 320x240, user-programmable LED modules, external pins and keyboard; Supports USB 2.0 and RS-232 interfaces. Supports multiple modes of flashing and debugging ARM microcontroller. The appearance of the printed circuit board of the laboratory layout ML-3 is shown in Figure 3.

VI. TECHNICAL CHARACTERISTICS OF ML-4

Laboratory layout ML-4 is designed to study the principles of signal processing with the help of signal processors. This layout is applied in disciplines that deal with issues related to digital signal processing. The structure of the ML-4 includes: signal processor ADSP-BF532 BlackfinB® Processor, dynamic memory block 32 MB (16M x 16-bit) SDRAM, 2 MB (512K x 16-bit x 2) FLASH, AD1836 96 kHz audio codec , ADV7183 video decoder, ADV7171 video encoder, ADM3202 for RS-232, USB 2.0, user-programmable LEDs, buttons and user-programmable pins.

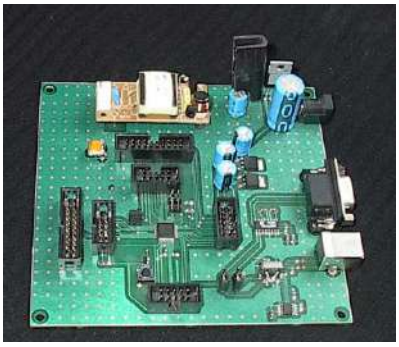

Fig. 3. ML-3 laboratory model.

The appearance of the printed circuit board of the laboratory layout ML-4 is shown in Figure 4.

When conducting an educational process in the system of secondary special, technical and higher education, in scientific departments, research institutes, the modernization of laboratory equipment and measuring equipment is relevant. The existing outdated equipment does not provide requirements for accuracy and reliability of measurements, it is morally and physically outdated, having repeatedly developed its resource. Often in the educational process in the universities of Ukraine are used devices that were manufactured in the 50-60s of the 20th century. Most of the measuring instruments do not pass the metrological tests, and the measurements obtained with their help contain a large proportion of errors and errors, and therefore require updating and replacement.

Fig. 4. ML-4 laboratory model.

Professional measuring equipment, for example, manufactured under the brand name Tectronics and Ag-ilent, is very expensive and is not acquired even by large firms. In the same time, the emergence of new micro-controllers with a rich set of peripherals and support for a high-speed data exchange channel with a computer that do not require additional power supplies made it possible to create a compact device that combines all the above listed functions, at a price significantly lower compared to branded counterparts. As a result, a measuring complex was developed and manufactured, which contains 10 measuring devices in one housing:

- two-channel oscillograph, recorder;
- multimeter, which includes a voltmeter, ammeter, frequency meter, phase meter;
- functional generator;
- logic analyzer;
- logical generator;

- spectrum analyzer,

which allows for a full cycle of work in the presence of one such device at the workplace. The developed device has small overall dimensions and is several times cheaper than the corresponding foreign analogues. Today, there are two versions of the measuring complex. In the first case, it is a complex oriented to work with software installed on a computer, in the second case it is an independent complex with its LCD display, fully functioning without a computer. The developed measuring complex IK-1 is recommended for use in the educational process of technical-oriented universities.

CONCLUSIONS

In KNURE more than 200 such laboratory models are used for specialties and areas of training, such as information control systems and technologies; Computer systems and networks; system Programming; specialized computer systems; control systems; microelectronics and semiconductor devices; biomedical engineering, radio-electronic devices, systems and complexes; radio communications and television equipment; electronic household equipment; information security systems; metrology and measuring equipment. This equipment is introduced into the educational process of the following universities of Ukraine: Kharkiv National Polytechnic University "KPI"; Kiev University of Economics and Technology of Transport; Ukrainian State Academy of Railway Transport; Cherkasy State Technical University; Ivanofrankovsky National Technical University.

In addition, the use of this laboratory base allows to transfer the thesis design to a qualitatively new level, providing the opportunity to create real graduation projects, the output of which is not only an explanatory note with a theoretical presentation of the material, but also actual devices and mock-ups.

It should be noted that the problem of introducing such laboratory mockups requires appropriate preparation of teaching materials (lecture courses, instructions for practical training and laboratory workshops, as well as multimedia courses and electronic teaching aids for distance and distance learning). In this regard, there is a need to organize training of teaching staff, retraining courses and advanced training of specialists working in industry.

In conclusion, we can conclude that, based on the principle of remote programming of microcontrollers, it is possible to implement courses for remote laboratory work on the study of microprocessor control systems of various degrees of complexity. The perspectives of the work are the improvement of the software and hardware to expand the functional and educational capabilities of the remote laboratory workshop. The introduction of modern laboratory facilities in the educational process allows us to interest the modern student and teach him practical skills of working with real equipment.

REFERENCES

[1] V. Semenets, "Technical aspects for development laboratory base for learning FPGA and microcontroller systems," *2009 10th International Conference - The Experience of Designing and Application of CAD Systems in Microelectronics*, Lviv-Polyana, 2009, pp. 145-145.

[2] V. Semenets, V. Kauk, O. Avrunin. "The advanced technology of remote training at the initial process" ["Vprovadjennya tehnologiy dystantsiynogo navchannya u navchalnii protses"], High School, 2009. – No. 5 .– P. 40– 45

[3] O. Avrunin, S. Sakalo and V. Semenetc, "Development of up-to-date laboratory base for microprocessor systems investigation," *2009 19th International Crimean Conference Microwave & Telecommunication Technology*, Sevastopol, 2009, pp. 301-302.

[4] O. Avrunin. The experience software-based design of virtual medical in trascopy systems for simulation study International Journal / O. Avrunin, L. Aver'yanova, V. Golovenko, O.Sklyar // Information Technologies and Knowledge. – 2008. – Vol.2. – P. 470–474.

[5] Sakalo S.M., Semenets V.V., Azarhov O.Yu. High frequencies in medicine (therapy and diagnostics): Teaching manual - X.: KNURE; Collegium, 2005. - 264 p.

[6] Y. Nosova, O. Avrunin and V. Semenets, "Biotechnical System for Integrated Olfactometry Diagnostics", Innovative technologies and scientific solutions for industries, vol. 0, no. 11, pp. 64-68, 2017. doi: 10.30837/2522-9818.2017.1.064.

[7] Avrunin OG, Faruk H. "On the possibility of using modern proportional electronics for modeling human breathing" Industrial voice and pneumatic. 2013. № 3 (41). Pp. 78–82.

[8] Y. Nosova, K. Faruk and O. Avrunin, "Radio Technology in Biomedical Investigation", *Telecommunications and Radio Engineering*, vol. 77, no. 15, pp. 1389-1395, 2018. doi: 10.1615/telecomradeng.v77.i15.90.

[9] Farouk, H., Avrunin, O. Comparison Discriminate Characteristics Between Modern TNDA-PRH Rhinomanometer And Previously Methodology. International Journal of General Engineering and Technology (IJGET) ISSN 2278-9928. – 2013 – Vol. 2, Is. 2, – P. 39-50.

[10] O. Avrunin, N. Shushlyapina, Y. Nosova and O. Bogdan, "Olfactometry diagnostic at the modern stage", *Bulletin of the National Technical University «KhPI» Series: New solutions in modern technologies*, vol. 0, no. 12(1184), p. 95, 2016. doi: 10.20998/2413-4295.2016.12.13.

[11] Y. Nosova et al., "The use of statistical characteristics of measured signals to increasing the reliability of the rhinomanometric diagnosis", *Photonics Applications in Astronomy, Communications, Industry, and High-Energy Physics Experiments 2016*, 2016. doi: 10.1117/12.2248364.

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Testability Increasing Method by Introducing Hardware Redundancy in the Easy-tested Finite State Machines

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***Abstract*—Testability increasing methods by introducing hardware redundancy into the circuit implementation are sufficiently developed and widely used in the design. Since the construction of the testing sequence is based on the use of automaton diagrams, it eliminates the need to analyze the circuit implementation of the remote control when building a diagnostic experiment. This approach allows us to extend the class of detectable faults, which in structural-analytical test generation methods is limited, as a rule, to a multitude of single constant faults. The use of automaton models in the construction of tests allows to detect any malfunction that changes the automaton diagram of a serviceable remote control and does not increase the number of states of remote control memory elements. There was described finite state machine using hardware description language. The method of computer-aided design of the easytested control FSM by introducing the hardware redundancy is presented in the paper. The FSM model is represented in VHDL in the form of the FSM template. The solution way is to add additional fragments of the VHDL code, which ensure the forced setting of the FSM into an arbitrary state without the use of synchronizing sequences. The use of the shift register in the memory part of the control FSM for organizing the path scanning was considered. The method of FSM state table expansion, which ensures the mode of bypassing all nodes of the FSM' state diagram in the diagnostic mode was proposed.**

Keywords—easy tested finite state machine, Hamiltonian cycle, distinguishing sequence, homing sequence, shift register.

I. INTRODUCTION

During design of a digital devices such model of a digital device with memory as finite state machine (FSM) is widespreaded [1-3]. Finite state machine, like other digital devices models are presented in languages VHDL, Verilog , intended for designing digital circuits on modern basis of field-programmable gate array (FPGA). According to VHDL descriptions of finite state machine is synthesized synchronous logical circuits in a given basis of logical elements. Today, the process of synthesis is automated [4-5] and the most important problem when creating projects and system-on-a-chip (SoC) is the problem of verifying the original submitted to the VHDL. The actual task is the further development of procedure of computer-aided design of easy tested finite state machines, which are presented using hardware description language, and their verification.

II. TESTABILITY OF FINITE STATE MACHINE

Testability increasing methods by introducing hardware redundancy into the circuit implementation are sufficiently developed and widely used in the design. In technical diagnostics, the direction associated with the use of the classical theory of experiments with finite state machines for constructing testing sequences is known [6].

An experiment with finite state machines refers to the process of applying input sequences, observing the corresponding output sequences, and deriving conclusions based on these observations. A characteristic feature of the theory of experiments with finite state machines is the use of the functional approach and the transition-output tables of the automaton model of remote control to build a complete testing sequence.

The fundamental work, in the theory of experiments with finite state machine, is the work [7]. In this paper, it is proposed to use a number of characteristic sequences that allow identification of the transition table-output of an finite state machine. The procedure proposed in [7] gives the best results for a class of minimal strongly connected finite state machine having distinguishing. In the same paper, the class of installation synchronization and characteristic sequences is defined, which allows one to construct verifying experiments for finite state machine that do not have distinguishing sequences. In the future, this direction was developed in the work [8].

The main advantage of this direction is the simplicity of constructing a testing sequence for a given finite state machine and a wide class of detectable faults, which is limited only by faults that increase the number of states of the machine. The complexity of constructing a testing experiment with an finite state machine is determined by the properties of its diagram. To easily tested finite state machine [6-10], we will assign finite state machine, for which the tasks of test diagnostics are solved as simply as possible within the established costs. Before discussing the design of checking experiments, it is appropriate to recall several definition relating to experiments performed on sequential circuits or finite state machines. A synchronizing sequence for a given sequential circuit is an input sequence whose application is guaranteed to leave the circuit in a certain final state, regardless of the particular initial state of the circuit. Some circuits have synchronizing sequences, others do not. A homing sequence for a given sequential circuit is an input sequence whose application makes it possible to determine the final state of the circuit by observing the output sequence that the circuit produces. Both synchronizing and homing sequences have to do with the determination of the final state of a circuit. A distinguishing sequence is an input sequence whose application makes it possible to determine the initial state of the circuit by observing the output sequence that the circuit produces [7]. The opinion of experts in the field of the theory of experiments with finite state machine is that the class of finite state machine having distinguishing, synchronizing and homing sequences of minimal length is a class of easily tested finite state machine. This class of finite state machine is a model of testable discrete devices with memory elements. Therefore, the analysis of the properties of finite state machine models is directly related to the analysis of the conditions for constructing testable devices, that is, with the development of methods for testable design. Currently, testability is one of the main criteria by which the design level is assessed, and is informally defined as follows: financial costs, time and values of indicators characterizing the object's ability to detect faults, search for a fault site and implement test diagnostics.

III. Functional Approach to Synthesis of Diagnostic Experiments with Finite State Machines

An experiment with an finite state machines is the process of applying the input sequences, observing the corresponding output sequences and deriving conclusions based on these observations. Depending on the purpose of the experiment, experiments on identification of the states of the finite state machines, identification of the input sequence of the finite state machines, and identification of the finite state machines with the states differing from all other finite state machines with the same number of states differ.

In the development of approaches, principles, methods and used mathematical models in the technical diagnostics of complex discrete or digital objects, several directions were formed. The first direction includes structural-analytical test generation methods based on knowledge of the circuit implementation and explicit models of logical faults.

The second direction, based on the functional approach and a wider class of implicit models of detectable faults, involves the use of automatic models and the construction of a test sequence that allows to check the conformity of the diagram or transition-output table of the tested device to the transition- output table of the healthy device.

In the development of the second direction of test diagnostics, the methods of the classical theory of experiments with finite state machines are widely used. A characteristic feature of this theory is the use of the functional approach and the transition-output tables of the automaton model to build a complete testing sequence. Since the construction of the testing sequence is based on the use of diagrams, it eliminates the need to analyze the circuit implementation when building a diagnostic experiment. This approach allows to extend the class of detectable faults, which in structural- analytical test generation methods is limited, as a rule, to a multitude of single constant faults. The use of finite state models in the construction of verification tests allows detecting any malfunction that changes the diagram of a healthy device and does not increase the number of states of the elements of the memory [10-11].

IV. Graph Model of Easy Tested Finite State Machines

The methods of graph theory was used during development graphic models of easy tested finite state machine, methods of the theory of digital machines was used for the organization of diagnostic experiments with automaton models of functional modules.

The shift register (SR), as a standard, homogeneous and easy-to-test structure, is widely used in discrete devices of various uses. The structural methods of increasing the reliability of the test, the method of the path scanning, as well as some methods of converting automated device models into easily tested ones, ultimately, are reduced to providing in the diagnostic mode a controlled reconfiguration of memory elements in one shift register, the serial input and output of which are the external poles of the device. In addition, the device implemented on shift registers is easy to test, since shift register has a distinguishing minimum-length sequence. In this connection, the study of the diagnostic properties of sequences generated by shift register is an important task directly related to solving the problem of synthesis of easily tested devices and systems. automaton models for certain rules of construction trees and truncating its finite vertices [10].

V. Realization of Easy Tested Finite State Machine

Computer-aided design of digital devices (DD) based on specification which is represented in the form of hardware description language (HDL). Spesialized data processing and control DD as a rule described by finite state machines (FSM). The form of finite state machine representation are state table (ST) and state diagram (SD). The FSM template, i.e. a way to describe of the models of the control FSM, the specification of which is specified by the state table or by the state diagram. This is a special structure of the HDL-model, in which the functions of transitions and outputs are isolated into separate processes (process), and the assignment of the new state is carried out in a special process associated with synchronization [9-11]. One of ways to describe DD models in the form of FSM using VHDL language is the FSM template, i.e. a way to describe of the models of the control FSM, the specification of which is specified by the state table

or by the state diagram. This is a special structure of the HDL-model, in which the functions of transitions and outputs are isolated into separate processes (process), and the assignment of the new state is carried out in a special process associated with synchronization (Fig.1).

```
architecture FSM_MX of FSM_MX is
signal  State, NextState:
          STD_LOGIC_vector (2 downto 0);
signal a1: STD_LOGIC_vector (2 downto 0):="001";
signal a2: STD_LOGIC_vector (2 downto 0):="010";
signal a3: STD_LOGIC_vector (2 downto 0):="011";
signal a4: STD_LOGIC_vector (2 downto 0):="100";
signal a5: STD_LOGIC_vector (2 downto 0):="101";
begin
Sreg0_CurrentState: process (Clk, Reset)
begin
   If Reset='1' then State <= a1;
   elsif Clk'event and Clk = '1' then
      if A='1' then State <= NextState;
      else          State <= State(1 downto 0) & TDI;
      end if;
  end if;
end process;
```

Fig. 1. The architecture fragment of the VHDmodel of Moore FSM with shift register.

Let's extend the ST of Mealy finite state machine (Fig. 2) by adding shift register Sh. If Sh=1, the finite state machine operates in the setting mode in any given state, and if Sh=0, the finite state machine realizes the given algorithm.

Simulation of extended VHDL-models of the control finite state machine using Active-HDL confirmed the operability of this approach. Synthesis of these models using CAD XILINX ISE confirmed the receipt of testable structures.

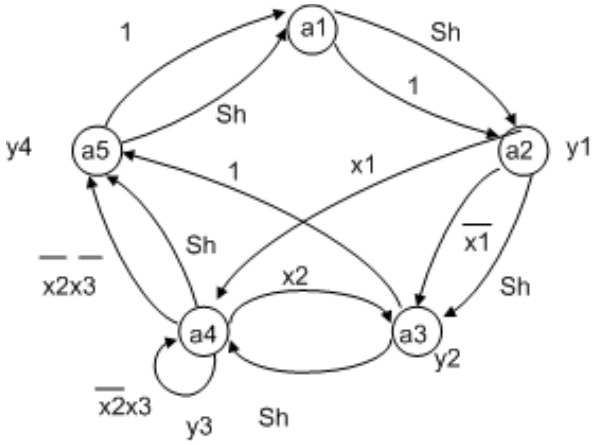

Fig. 2. Graph model of Moore FSM with shift register [10].

VI. Conclusion

The practical significance of the obtained results is to develop the procedures for adding redundancy and expanding the input alphabet of HDL-models by adding additional conditional operators in the HDL-code, which is conduct to an arbitrary state. Developed procedures can be applied during the development of an additional program module for CAD, which will automatically generate the HDL code of the easy- tested finite state machine.

References

[1] P. Bibilo and V. Romanov, "Construction of compact tests for functional verification of VHDL descriptions of finite automata", Control systems and machines, №1, 2017, pp.35-45.

[2] V. Semenets, G. Krivulya, A. Gorbatyuk, and A. Shilverst, VHDL for designing computer devices. Kharkov: Publishing House of Kharkov Technical University of Radio electronics, 2001, p.164.

[3] P. Bibilo Synthesis of logic circuits using the VHDL language. M: SOLON-P, 2009, p.384.

[4] A. Dolmatov and A. Petrov, XILINX XST synthesis technology. Laboratory work 3. Ekaterinburg: Publishing House of Ural State Technical University, 2005, p.23.

[5] ISE. In-Depth Tutorial, UG695 (v14.1). 2012. Xilinx, p.150.

[6] P. Parkhomenko and E. Soghomonyan, Basics of technical diagnostics. M: Energy, 1981, p.320.

[7] F. Hennine, "Fault detecting experiments for sequential circuits," 5th Annual Symposium on Switching Circuit Theory and Logical Design, 1964, pp.95-100. doi: 10.1109/SWCT.1964.8.

[8] V. Totsenko, Algorithms for technical diagnostics of discrete devices. M: Radio and communication, 1983, p.240.

[9] M. Miroschnyk, T. Korytchinko, O. Demihev, V. Krylova, D. Karaman and I. Filippenko, "Practical methods for de Bruijn sequences generation using non-linear feedback shift registers," 2018 14th International Conference on Advanced Trends in Radioelecrtronics, Telecommunications and Computer Engineering (TCSET), Slavske, 2018, pp. 1157-1161. doi: 10.1109/TCSET.2018.8336400.

[10] M. Miroshnyk, Y. Pakhomov, E. German, A. Shkil, E. Kulak and D. Kucherenko, "Design automation of testable finite state machines," 2017 15th IEEE East-West Design and Test Symposium (EWDTS), Novi Sad, 2017, pp.1-6. doi: 10.1109/EWDTS.2017.8110034.

[11] M. Miroshnyk, S. Poroshin, A. Shkil, E. Kulak, I. Filippenko and D. Kucherenko, "Design logical control units with finite state machine patterns,".2018 16th IEEE East-West Design and Test Symposium (EWDTS), Kazan, 2018, pp.203-208. doi: 10.1109/EWDTS.2018.8524869.

[12] O. Drozd, M. Kuznietsov, O. Martynyuk and M. Drozd, "A method of the hidden faults elimination in FPGA projets for the critical applications," 2018 IEEE 9th International Conference on Dependable Systems, Services and Technologies (DESSERT), 2018, Kiev, pp. 218-221. doi:10.1109/DESSERT.2018.8409131.

[13] G. Kuchuk, V. Kharchenko, A. Kovalenko and E. Ruchkov, "Approaches to selection of combinatorial algorithm for optimization in network traffic control of safety-critical systems," 2016 IEEE East-West Design and Test Symposium (EWDTS), 2016, Yerevan, pp. 1-6. doi: 10.1109/EWDTS.2016.7807655.

[14] I. Furman, M. Malinovsky, S. Bovchaliuk, A. Allashev, "Retrospective analysis of the development of a parallel-action PLC architecture," Bulletin of Kharkiv National Technical University for Petro Vasylenka, 2016, №176, pp.35-38.

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In-circuit Signal Analysis in the Development of Digital Devices in Vivado 2018

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***Abstract*—Considered the implementation of in-circuit analysis of logical signals in digital devices synthesized in Xilinx Field-Programmable Gate Array. Designed a digital control device streaming analog-to-digital converter. An analysis of the results of the analog-digital conversion was carried out and measures were taken to smooth out the false results of the conversion.**

Keywords—analog-digital converter, Field-Programmable Gate Array, in-circuit debugging, Logic Analyzer, bus, clock signal .

I. INTRODUCTION

Xilinx is one of the world leaders in developing and selling Field-Programmable Gate Array (FPGA). The company produces several FPGA series, such as Spartan, Artix, Kintex. For the design of digital devices based on FPGA is available free software Vivado. Its current latest version is Vivado 2019. The process of developing a digital device consists of a number of mandatory steps: a description of the device in VHDL or Verilog, synthesis and simulation of the device, description of limitations, generation of the firmware file, firmware download and testing of the device. Built-in simulation tools allow you to analyze the work of synthesized timers, signal generators, etc. However, almost any digital device communicates with external sensors, RAM and flash memory, analog-digital and digital-analog converters. Therefore, analysis of the interface and internal digital signals in a working digital device is necessary. The in-circuit debugging capability of a digital device in the Vivado environment is provided by the IP core Integrated Logic Analyzer (ILA). It allows you to make a temporary sample of up to 1024 digital signals (single-bit or multi-bit). The depth of sampling of each of the signals is from 1024 to 131071 counts. Consider the capabilities and configuration of the IP core ILA on the example of high-speed analog-to-digital converter (ADC) control AD9235.

II. ADC AD9235 SPECIFICATIONS AND MANAGEMENT

ADC AD9235 is widely used to digitize: signals of digital radio receivers at intermediate frequency, signals of optical arrays, etc. The ADC has the following characteristics: conversion frequency up to 65MSPS, 12-bit conversion result width, parallel output bus, analog input voltage range up to 0.5 or up to 1V when using an internal voltage source. ADC refers to the conveyor type of converters. For each pulse of the clock signal at the CLK input on the output bus D0 ... D11, a conversion result is generated. The delay in establishing data on the D0 ... D11 bus is less then 6 ns relative to the rising edge of the clock signal. The conveyor delay of the output of the result of analog-to-digital conversion is equal to 7 periods of the clock signal. Figure 1 shows the working principle of the ADC.

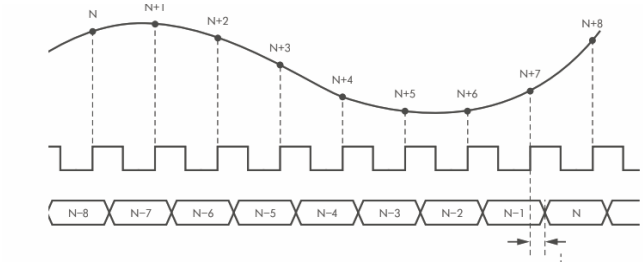

Fig. 1. Working principle of the ADC.

III. INTEGRATED LOGIC ANALYZER

To configure the ILA's IP core in the Vivado environment, use the Wizard, which allows you to configure the interface structure for connecting input and output signals. Customizable parameters include: the number of analyzed signals (probe), probe storage buffer depth, the resolution of using an external trigger, the use of an additional trigger. The ILA core can work in automatic mode and by trigger. Auto mode allows you to capture 1024-131071 samples of input signals on a command from the Vivado environment from the moment you receive the command. Figure 2 shows the ILA kernel settings.

The sampling frequency is determined by the frequency of the clock signal arriving at the clock input. This mode is effective for analyzing periodic signals with a sample time limit. For example, at a clock frequency of 100 MHz, the maximum analysis interval is 1.3 ms. When asynchronous interaction with external devices, the formation of signals of the interface VGA, etc. It is advisable to use the operation mode using the trigger trigger.

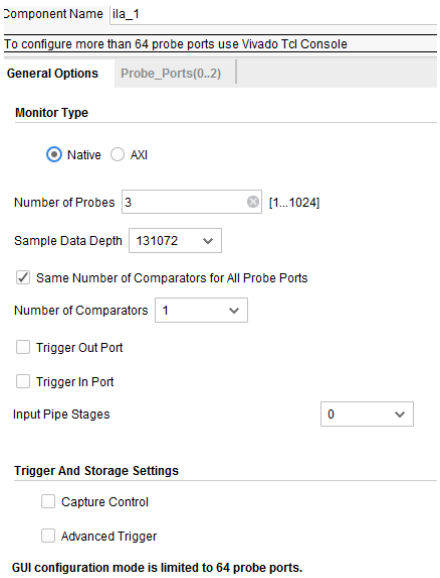

Fig. 2. ILA kernel settings.

After completing the configuration of the ILA core, a component description is generated that is embedded in the main program.

IV. In-circuit debugging of the control unit AD9235

For research work ADC was used Demo Board Nexys 4DDR. Based on the Artix7 FPGA, a 40 MHz clock frequency module was developed in VHDL. The generated clock frequency was applied to the clock input Clk AD9235. Reading the conversion results from the output data bus is performed on the falling edge of the clock signal. The delay between the launch of the ADC and the reading of the conversion result is 12.5 ns, which meets the requirements of the manufacturer of the ADC. For in-circuit debugging of the digital control device AD9235, the ILA core is built into the program. The core is configured to analyze three signals: the clock signal Clk, 12-bit data bus D0 ... D11, the signal over-range (OTD). The depth of sampling is 131071 counts. The ILA component description is shown below.

```
COMPONENT ila_0
PORT (clk : IN STD_LOGIC;
probe0 : IN STD_LOGIC_VECTOR(0 DOWNTO 0);
probe1 : IN STD_LOGIC_VECTOR(0 DOWNTO 0);
probe2 : IN STD_LOGIC_VECTOR(11 DOWNTO 0)
);
```

V. Simulation results

An analog input AD9235 from the signal generator was fed a sinusoidal signal with a frequency of 4 MHz. The amplitude of the signal is 1B. Figure 3 shows waveforms of analog-to-digital conversion results and interface signals of the AD9235.

Analysis of the conversion results shows that some samples may be distorted, as evidenced by setting the output of the OTR logical signal to “1”. The main causes of such distortions can be: interference in the power supply circuits and over-amplification of the input signal. The solution of such problems should be complex - hardware and software. To solve such phenomena, it is necessary to use a hardware power isolation between the digital and analog part of the circuit. The software part of the solution must contain an interpolating filter. The filter should interpolate an unreliable measurement result based on neighboring time samples of the signal being processed. Such a filter for the case of continuous input signal was developed by the authors in the language of VHDL.

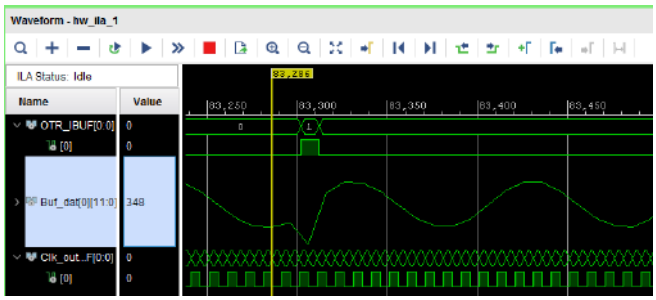

Fig. 3. Waveforms of analog-to-digital conversion results.

The filter module uses a buffer of seven 12-bit analog signal times, as well as a buffer of seven OTR signal samples. The quadratic interpolation method was implemented by software.

After applying the filter to the results of the analog-digital conversion, the probability of distortion decreased from from $3 \cdot 10^{-4}$ to $1.3 \cdot 10^{-8}$.

The residual error is due to cases where the OTR signal does not indicate the occurrence of distortion.

VI. Conclusion

Intracircuit debugging based on the ILA core allows you to identify the features of the digital nodes that the synthesized FPGA interacts with. Such features are almost impossible to model because of the random nature. Through the use of ILA, distortion of the result of converting an analog signal to digital form was detected using the ADC AD9235. The use of an interpolating filter made it possible to significantly reduce the effect of distortion.

References

[1] C. Sisterna, M. Segura, M. Guzzo, G. Ensinck and C. Gil, "FPGA implementation of an ultra-high speed ADC interface", *2011 VII Southern Conference on Programmable Logic (SPL)*, 2011. doi: 10.1109/spl.2011.5782642.

[2] Jinyuan Wu, Sten Hansen and Zonghan Shi, "ADC and TDC implemented using FPGA," *2007 IEEE Nuclear Science Symposium Conference Record*, Honolulu, HI, 2007, pp. 281-286. doi: 10.1109/NSSMIC.2007.4436331.

[3] V. Semenets, "Technical aspects for development laboratory base for learning FPGA and microcontroller systems," *2009 10th International Conference - The Experience of Designing and Application of CAD Systems in Microelectronics*, Lviv-Polyana, 2009, pp. 145-145.

[4] Semenets V. V., Kratts Dzh., Nevlyudov I. Sh., Palagin V. A. Tekhnologiya mezhsoedinenii elektronnoi apparatury. Ucheb. dlya vuzov. Khar’kov: «SMIT», 2005.

[5] S. Sakalo, V. Semenets and O. Azarhov, *High frequencies in medicine (therapy and diagnostics): Teaching manual*. Kharkov: KNURE; Collegium, 2005, p. 264.

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Field Programmable Counter Arrays Integration with Field Programmable Gates Arrays

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Abstract–Field Programmable Counter Arrays (FPCAs) have been recently introduced to close the gap between Field Programmable Gates Arrays (FPGA) and Application Specified Integrated Circuits (ASICs) for arithmetic dominated applications. FPCAs are reconfigurable lattices that can be embedded into FPGAs to efficiently compute the result of multi-operand additions.

Keywords–Field Programmable Counter Arrays, arithmetic applications, integration, shadow cluster.

I. FPCA INTEGRATION WITH FPGAS

This thesis presents a study of the issues related to integration of hard blocks (and/or coarse-grained blocks) into FPGAs. It then proposes some integration scenarios for FPCAs and describes a generic platform for implementation and evaluation of some of these scenarios based on Stratix II devices and the FPCA architecture.

The Problem

The introduction of hard logic blocks and coarse-grained blocks for FPGAs creates a new problem: their seamless integration. In simple words, the problem asks how should these blocks be floor planned and placed in the homogeneous array of soft logic, and how should they be connected to the routing fabric efficiently? The floor plan should result in shorter critical paths and reduced congestion and an interface must be designed for the block that meets the following requirements:

- it should provide the required level of connectivity (i.e. all typical circuits using the block should be routable);
- it should be fast and consume minimum chip area;
- it should minimize the negative impact on the rout ability of other blocks.

II. RELATED WORKS

Field Programmable Counter Arrays (FPCAs) are one-dimensional array of basic computational elements called Compressor Slices (CSlices). FPCAs are configurable lattices that perform Multi-Operand Additions (MOA) efficiently. MOAs – either explicitly or implicitly in the heart of other blocks – occur frequently in arithmetic circuits used in video applications, cryptography, wireless communication, etc. In multipliers, the partial product bits generated by a level of AND gates, represent MOA as well.

Dadda and Wallace trees reduce the partial products to a two input addition. They are also referred to reduction trees. Verma and Ienne have proposed a set of transformations which expose large multi-operand additions from arithmetic circuits. In this way, datapath circuits can be be implemented more effectively by specific digital circuits like FPCAs (also called here compressor trees) rather than general logic produced by using commercial synthesis tools.

Although there has been significant study on new architectures for hard and coarse-grained blocks for FPGAs, few of them have studied their detailed interface. In [1], formal optimization methods are used to design mixed-granularity FPGA architectures. Integer Linear Programming (ILP) is incorporated to determine the best floor plan to optimize the architecture for a set of DSP applications, including the choice of the best mix of hard 18*18-bit multipliers.

A similar problem is studied for block RAMs in [2]. In this work, without any investigation and inspired by commercial FPGAs, it is assumed that a row of block RAMs is located in the middle of the chip (like Figure 1). The authors have tried to determine the ideal flexibility of the memory/logic interconnect block (illustrated in Figure 2). The flexibility of a memory/logic block is defined as the number of (or portion of) available routing wires to which each memory pin is connected. This study shows that if the flexibility is too low, many circuits become unroutable, while excessive large flexibility values increase the memory access time and also waste chip area.

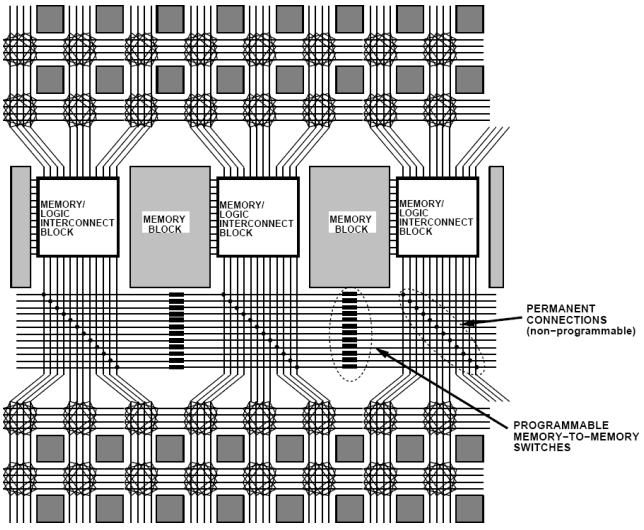

Fig. 1. An example of integrating RAMs as hard blocks [1].

Alternatively, the authors have made several enhancements to the routing architecture based on the characteristics of memory-to-memory connections, such as busses, in their benchmark circuits. Since nets connecting to multiple memory blocks are common in many circuits' blocks, the authors have proposed to add additional programmable switches between adjacent memories to support these nets. This significantly improved the results on architectures with lower interconnect block flexibility.

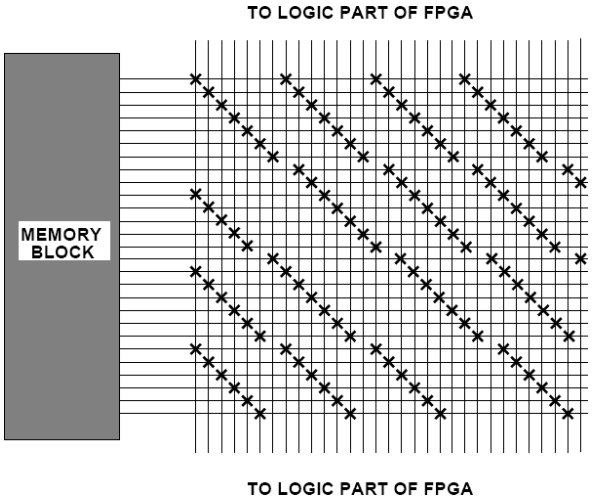

Fig. 2. Example of memory/logic interconnect block [1].

The large M-RAM blocks in Stratix II device resemble this style of integration. This solution enhances the ability to tile island-style architecture, and requires a completely new design for interfacing with the rest of routing fabric. Greater integrity and speed are achieved with larger hardwired blocks, but the layout design and interface design becomes a more complicated.

It doesn't seem that the results obtained for memory block integration could be used for arithmetic blocks such as FPCAs. The functionality of the pins and their contribution to total routing resource demand are different for blocks with different functionalities.

A very recent work [3], has studied the integration of coarse grained Floating Point Units (FPUs) in a fine-grained soft logic array. Different floor planning strategies for placement of the FPUs, different aspect ratios and possible pin placement methods are evaluated to find the optimum architecture. The approach taken is again an empirical one based on the delay and minimum channel width requirement of a set of benchmarks. Unlike the previous approach, they have assumed that the gridded routing fabric extends over their Embedded Blocks (EBs). Figure 3 shows a scenario where a 3*3 super-tile is replaced by an embedded block.

The M512 RAMs, M4K RAMs, and the DSP blocks in Stratix II devices are examples of this approach, but with a small difference. Tiles in the same column are all of the same kind. These tiles are all the same height (or multiples of same height) but their widths may slightly differ. In this way, the general routing fabric could be designed as easily as the general island-style routing fabric consisting of horizontal and vertical channels of routing wires with switch blocks in their intersections points. The problem of interconnect interface block design in this approach; will be to minimize the re-design of the intra-cluster connections in such a way that matches the actual pin-demand of the new hard blocks.

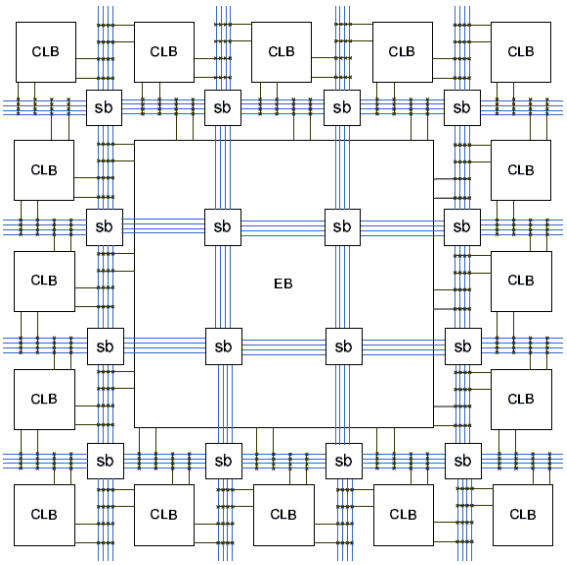

Fig. 3. Expansion of the gridded routing fabric over the embedded block [3].

As an example, the DSP blocks in the Stratix II architecture span 4 blocks vertically. The blocks are designed in such a way that they can be decomposed into four tiles. Each tile has the same height as other logic tiles and has a switch box, intra-cluster connections and the DSP core itself. The intra-cluster connection design for DSP blocks is interesting. LAB tiles in Stratix II devices have 45 local interconnect lines that are selected by a level of switches from the general routing network. These lines drive all the ALM inputs which are around 65 input pins. For the DSP tiles (¼ each DSP block), there are 60 local lines that drive approximately 40 input pins. This information is summarized in table 1. The reason for this local interconnect-input pin difference is that it is the actual pin-demand of the tiles which is important, not just the number of input pins. Many of the 65 input pins of the ALMs in each LAB could be shared or driven by the local feedback lines. This lowers the actual pin demand to 44. On the other hand, DSP block input pins are arithmetic bits, which are all distinct, and needed to be routed separately. Thus, more connections than the total number of input pins are provided by the local lines to ensure the required routing flexibility. FPCAs, from this point of view, are more similar to DSP blocks than to block RAMs.

TABLE I. INTRA-CLUSTER DESIGN OF LAB AND DSP TILES

Tile Type	*Local Interconnect Lines*	*Input Pins*
LAB Tile	44	=65
DSP Tile	60	=40

Hard blocks improve the area and speed of the designs mapped to FPGAs, but only if they are used. Otherwise, the silicon area devoted to them and, the expensive routing resources around them are wasted. This also suggests that the integration of hard blocks is only feasible if they are used often. Shadow clusters are introduced in [4,5] to take

better advantage of the routing resources around hard blocks, when they are not used. A shadow cluster is a soft logic block, placed "behind" the hard block so that if the design doesn't use the hard block, then some general FPGA logic within the shadow cluster can be used to implement a portion of the real circuit. Shadow clusters come at the expense of additional area, but, if properly used, the advantage obtained by making better usage of the routing network dominates this extra area overhead. Figure 4 depicts this idea. The inputs, which come from the routing network, are shared between the shadow cluster and the hard block. Depending on the mode of operation, either the output of hard block or the shadow cluster is selected.

Design Space Exploration (DSE) is a method to tackle problems where an analytical approach is difficult to take or there is no analytical solution based on the available theories and models. FPCA architecture design – according to our investigations – falls into this group of problems. By twisting every single knob in FPCA architecture, two trends affecting the performance in opposing directions could be identified that suggest the existence of an optimum point for each parameter. Alternatively, this optimum point depends on the value of other parameters, the technology used for VLSI implementation and, most importantly, the application (benchmarks) being mapped on the FPCA.

For example, increasing the MORC of the CSlices reduces the number of CSlices required to synthesize an application on the FPCA, improves the performance by making the critical path pass through fewer output multiplexers, and saves area by using fewer first-level counters. But, if the configuration of the GPCCC or the characteristics of the benchmarks does not allow exploitation of output ranks, thicker output multiplexing layers decrease the performance, and the area dedicated to extra parallel counters columns in the CSlices are wasted. An empirical approach could help overcoming such problems by examining all possible points in the design space, which can not be identified just by analysis. Since the intention is to have a real hardware model on which the benchmarks could be mapped and the area/delay values be extracted, the model is developed using synthesizable subset of VHDL.

Each FPCA sub-block was modeled in a generic fashion and sub-blocks were connected together in higher level blocks (also generic). In VHDL, generic statements are used to model generic blocks. Some of these generic values are calculated using a Perl script and written to a VHDL package which is included by other modules. The rest of the model is developed in pure VHDL.

Developing a generic HDL model of FPCAs was a non-trivial task.

Two of the most significant challenges were (1) Modeling parallel counters in an efficient way and (2) Modeling the interconnection of components inside a CSlice.

The first approach taken for modeling parallel counters was using behavioral VHDL as a loop in a process statement which counts the input bits and produces outputs. These models were synthesized using Synopsys Design Compiler v2006.06 and the compile_ultra optimization capability of the tool. The result for a 31:5 counter was poor. The synthesis tool could not find an efficient way to restructure the counter to produce acceptable results. One of the well known ways for efficient implementation of parallel counters is using a tree of Full-Adders and Half-Adders [6]. In this work, based on the ability of VHDL to model recursive circuits [7] a generic adder tree is modeled to mimic a tree of full adders and half adders. The results obtained by this approach were more acceptable and comparable to manual description of fixed size counters. More advanced methods for synthesis of parallel counters are also suggested [8].

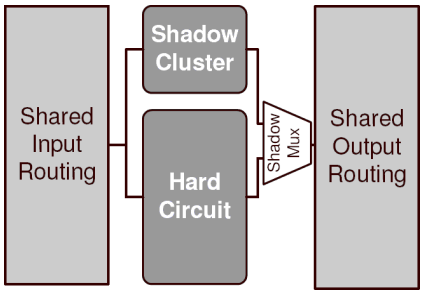

Fig. 4. Illustration of shadow cluster concept [3, 4].

III. Conclusions

A design space exploration tool for FPCAs consisting of a generic model of FPCAs, a mapping heuristic with synthesis and report automation facilities were developed. An analysis of the design space was performed and a new metric called utilization was suggested to prune the DSE.

A set of benchmarks were chosen and the DSE were performed, and some of the best performing architectures in terms of speed and area were highlighted.

The problem of integrating FPCAs with FPGAs was also studied.

References

[1] A.M. Smith, G.A. Constantinides, and P.Y.K. Cheung, "Integrated Floorplanning, Module-Selection, and Architecture Generation for Reconfigurable Devices," Very Large Scale Integration (VLSI) Systems, IEEE Transactions on, vol. 16, 2008, pp. 733-744.

[2] S. Wilton, J. Rose, and Z. Vranesic, "The memory/logic interface in FPGAs with large embedded memory arrays," Very Large Scale Integration (VLSI) Systems, IEEE Transactions on, vol. 7, 1999, pp. 80-91.

[3] C.W. Yu et al., "The Coarse-Grained / Fine-Grained Logic Interface in FPGAs with Embedded Floating-Point Arithmetic Units," Programmable Logic, 2008 4th Southern Conference on, 2008, pp. 63-68.

[4] Peter Jamieson and Jonathan Rose, "Enhancing the area-efficiency of FPGAs with hard circuits using shadow clusters," Field Programmable Technology, 2006. FPT 2006. IEEE International Conference on, 2006, pp. 1-8.

[5] P. Jamieson and J. Rose, "Architecting Hard Crossbars on FPGAs and Increasing their Area Efficiency with Shadow Clusters," Field-Programmable Technology, 2007. ICFPT 2007. International Conference on, 2007, pp. 57-64.

[6] B. Parhami, *Computer Arithmetic: Algorithms and Hardware Designs*, Oxford University Press, USA, 1999.

[7] P. Ashenden, "A comparison of recursive and repetitive models of recursive hardware structures, *VHDL International Users Forum. Spring Conference, 1994. Proceedings of*, 1994, pp. 80-89.

[8] A. Verma and P. Ienne, "Automatic Synthesis of Compressor Trees: Reevaluating Large Counters," *Design, Automation & Test in Europe Conference & Exhibition, 2007. DATE '07*, 2007, pp. 1-6.

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Organization Features of Parallel Processes in Programs for Microcontrollers with a Small Amount of Program Memory

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***Abstract*—A way of organizing parallel processes without the use of real-time operating systems is described, which is convenient for writing programs for microcontrollers with a small size of program memory.**

Keywords—microcontroller, program, parallel process

I. INTRODUCTION

Microcontrollers have found wide application in various kinds of radio equipment. Depending on the design task, microcontrollers can be used from the simplest models to the edvanced, which have a significant number of peripheral modules and a large amount of program memory.

The most popular programming languages for microcontrollers is the assembler and C. The assembler language's uncomfortabling is the compiler's dependence on the kernel being used, among which the most popular are PIC, AVR, 8051, and Cortex [1, 2, 3].

In terms of program portability, C / C ++ compilers are more convenient. Using this language, various types of real-time operating systems are written specifically for microcontrollers (RTOS) [4, 5]. They allow you to implement flexible interfaces with different peripherals (displays, keyboards, memory cards, data ports, etc.) and perform parallel processes.

Application of operations system requires a sufficient amount of program memory (> 16 kilowords), which can only be used in complex applications.

In simple applications, the use of expensive microcontrollers is not appropriate. The volume of program memory in this case may not be enough to accommodate the operating system.

II. BRANCHED PROCESSES

Microcontrollers are used not as a separate unit, but as the main controller of the device. It must interact with the entire periphery connected to it. The knowledge and skills of a programmer who writes programs for a computer differ for the programmer of microcontrollers. The style of writing programs is made with experience and years.

For beginners it is typical to use standard software constructions. When organizing a branching of the program, the nested (multi-level) condition statements (if-else, switch-case) are used and often the operators of the unconditional goto transition. Embedded cycles may also be present in conditions and in other cycles. Here is an example of a possible variant of the code of the program.

```
if (Menu)
 {
 if (ff_kl_buton_star) goto endMenu;
 if (menu==1)
 {
 ...
 if (ff_kl_buton_star) goto endMenu;
...
//- - - - - - - - - - - - - - - - - - -
  if (submenu==1)
   {
   …
   do
   {
   …
   if (!ff_kl_buton_star)
    {
    …
     if (Condition_1)
      {
      while (1)
       {
       ...
       if (Condition_2)
        {
        if (Condition_3)
         {
         ...
         }
wait:
        if (Condition_3) break;
        if (!ff_KeyRead) goto wait;
        if (Condition_4)
         {
         ...
         }
         else
         {
         ...
         }
        …
        }
```

```
      else
      {
      ...
      break;
      }
     }
    }
    else
    {
    ...
    break;
    }
   }
  }
  while (!ff_kl_buton_star);
  break;
  }
//- - - - - - - - - - - - - - - - - - -
 if (submenu==2)
  {
  …
  }
//- - - - - - - - - - - - - - - - - - -
 if (menu==2)
 {
 …
 }
}
…
endMenu:
…
```

This design can be observed when organizing complex multi-level menus. To exit the menu item or the menu at all, you need to insert it in the checking program for a certain condition (highlighted in bold). The output is complicated by the presence of cyclic constructions.

When you exit the submenus of the menu sometimes there is a need to restore certain settings. If the transition after the recovery is always at the same point of the program, then you can use the goto unconditional transfer operator to part of the recovery code. From this place go to the given point. If at different points - it will have to organize a separate subroutine.

This approach leads to an increase in the number of transfer marks, the allocation of the program code block with curly braces ({}). The number of errors during the writing of the program increases. This increases the time it is written. It also complicates the process paralleling and interrupting, the program's response to interrupt from the peripheral modules of the microcontroller. For such an approach is inherent in the redundancy of the code, correspondingly, the volume of the program increases.

III. Processing Action Processor

It is suggested to apply a slightly different approach to building branched and parallel processes as a simplified RTOS replacement.

In the program, enter a block (or procedure) that will track signals from peripheral modules, interrupts, internal program processes, signs of execution of program blocks, prioritize, assign the required code of action. Let's name the block of program PROCESSING ACTION PROCESSOR (PAP). An example of building a program is given below.

```
while (1)
{
//PAP
…
//Actions
switch (Action)
      {
case 1:// Action 1.1
      {
      …
      break;
      }
case 2:// Action 1.2
      {
      …
      break;
      }
case 3:// Action 2
      {
      …
      break;
      }
…
default: break;
}
…
}
```

Actions are divided into more elementary. They should be through-cross, it is desirable to avoid cyclic structures inside the action. The PAP block and actions are performed in an infinite loop. You can delay one action and give permission to others, repeat the same action the required number of times.

IV. Conclusion

Using the processor to process operations and split actions into elementary operations simplifies the writing of programs and reduces the program code volume after compiling approximately 1.1-1.5 times (depending on the optimization of the software code).

References

[1] "8-Bit MCUs | Microchip Technology", *Microchip.com*, 2019. [Online]. Available: https://www.microchip.com/design-centers/8-bit. [Accessed: 18- Jun- 2019].

[2] "8051 Family - Nuvoton Direct", *Nuvoton Direct*, 2019. [Online]. Available: https://direct.nuvoton.com/en/8051-family/. [Accessed: 18- Jun- 2019].

[3] "Microcontrollers - STM32 Arm Cortex MCUs - STMicroelectronics", *St.com*, 2019. [Online]. Available: https://www.st.com/en/microcontrollers-microprocessors/stm32-32-bit-arm-cortex-mcus.html. [Accessed: 18- Jun- 2019].

[4] "Free RTOS for ST STM32 ARM Cortex-M3 microcontroller", *Freertos.org*, 2019. [Online]. Available: https://www.freertos.org/portstm32iar.html. [Accessed: 18- Jun- 2019].

[5] "FreeRTOS Kernel - The FreeRTOS kernel is an open source real time operating system and the de-facto standard solution for microcontrollers and small microprocessors - STMicroelectronics", *St.com*, 2019. [Online]. Available: https://www.st.com/en/embedded-software/freertos-kernel.html. [Accessed: 18- Jun- 2019].

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How to Use Equipment to Measure the Analog Signal by Means of FPGA System

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***Abstract*—This article is devoted to design of a measurement system based on specialized FPGA. A balance of ACD and DAC channels through output from one side and computation power of FPGA from another side is considered. Possibilities for obtaining one more tool for screening the signal processing is proposed**

Keywords—FPGA, analog signal, digital signal processing, measurement system

I. INTRODUCTION

A modern developer should be able to create modern devices. Their scope can be very wide. This measurement and intelligent devices, and medical equipment, and even telecommunications with multimedia. Constantly something new appears and you need to be ready for it.

Specialists in this field are required in firms engaged in research and design (R & D) of equipment and embedded solutions of computing and measuring equipment, telecommunications, medicine, automotive, environmental protection, and so on.

Great opportunities for the developer provides software company Xilinx, specialized for chips manufactured by the same company. Through the efforts of the company, the software is constantly being improved in terms of efficiency and flexibility. For the FPGA of the 7th generation, the Vivado software package [1] is recommended for use. The possibilities are expanding at the expense of working at different logical levels: in addition to the traditional level of register transfers, the new version has the opportunity to work at the system level. The list of valid programming languages was updated accordingly: if at the level of register transfers it is VHDL or Verilog, then at the system level it is SystemC, C or Python [1,2].

The Vivado software package refers to end-to-end software systems. It allows you to design modern devices on chips manufactured by Xilinx.

This company today produces PLM (CPLD), FPGA (FPGA), FPGA with pre-installed processor cores (SoC), as well as custom integrated circuits (ASIC). These types of microcircuits are related to microcircuits of different degree of integration, differ in the homogeneity of the internal structure, internal resources and purpose.

So, the main structural unit of the PLM is a 4 or 6 input configurable logic unit (CLB) with the ability to buffer outputs, allowing to implement all sorts of logical functions.

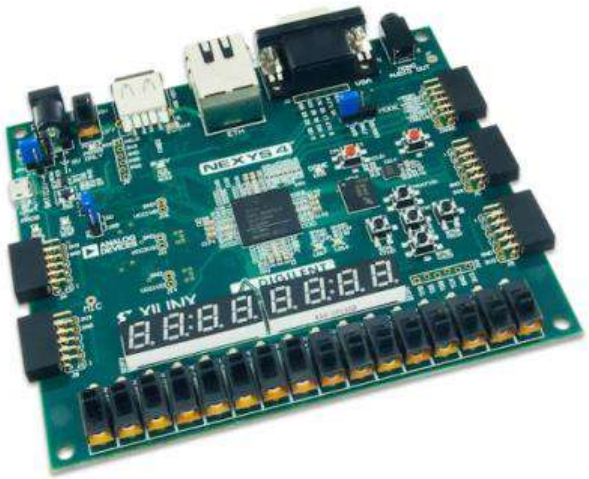

Fig. 1. Nexys 4 DDR with Artix-7 FPGA

FPGA 7 series differs from PLM not only in the fact that they have more such units on board, but also in the presence of specialized subsystems located in separate zones. For digital signal processing, this is a 12-bit ADC and a DSP48E1 digital processing unit (layer). If there is additional memory on the chip and the ability to connect via a wide high-speed channel of external memory, the capabilities of the PLM and FPGA differ significantly. The company produces a FPGA line optimized in terms of cost, price / quality ratio, efficiency (energy-performance ratio and speed) [3].

To implement algorithms that are demanding of computational resources, the company offers FPGAs with processors located on the same chip, which, from many points of view, simplifies system design.

All these innovations pose a task for software developers to maintain very diverse products. So, for PLA, apparently, is enough support for languages, such as VHDL or Verilog. Of course, a modeling module will be required taking into account time constraints and a modeling module for the implemented structure. Only now, to work with FPGAs, it will be necessary to work with a more complex system, with much larger amounts of memory and logical connections, with a large number of dedicated hardware adders and multipliers on board. And to work with multiple processors on board, you will need a language that allows you to operate

with a higher level of abstractions than Verilog and VHDL allows.

In such conditions, we are faced with an exciting, but not an easy task to study the Xilinx product range and software, their capabilities, application features for creating equipment for various purposes.

II. How to make a measurement studio out of this

Suppose we are going to measure an analog signal, using all the powers of new platform. We will need some analog inlet into digital system and maybe analog outlet for utilizing the result.

And here we go to work. We use FPGA when creating digital equipment for various purposes. And we implement some algorithm. What analog interfaces do manufacturers offer for use?

For the input analog signal onboard the Artix-7 platform, there is a 12-bit ADC with a conversion frequency of 1 MHz. Even for the youngest platform, this is not very much. PWM is proposed from the output channels for the analog signal, there is no DAC. Although the platform has enough ports to connect an external 12 or 16 bit D / A converter [5].

When performing various studies, it may be convenient to use the VGA monitor output as a graphical output device. This will require learning to perform the following operations.

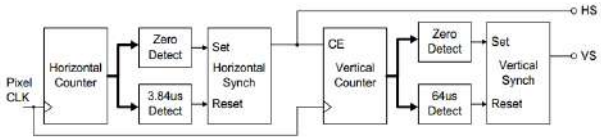

Fig. 2. VGA display controller block diagram

1. Display a digital stream (picture) on a monitor with given physical parameters: screen size in pixels and frequencies in rows and frames

2. Using the previous item as a standard procedure, display static graphic information (borders of graphic areas, scales, division prices, titles and labels on axes) and dynamic information (data displayed on charts)

3. The capabilities of the measuring complex will increase if you add the ability to interrogate hot keys that allow you to measure parameters and maintain cursor measurements

4. The data displayed on such a monitor can be of various types. The first thing that comes to mind is the dependence of the signal on time in real time, its spectral or correlation function.

The main problem is that the system should be balanced in its part to meet requirements for the task given. It is understood that a board like Nexys 4 DDR is designed as universal product for a broad circles of tasks and needs. It contains quite a lot of up-to-date digital interfaces like PCI-E 10 GbE to name a few. Maybe, it is a case when one wants something special?

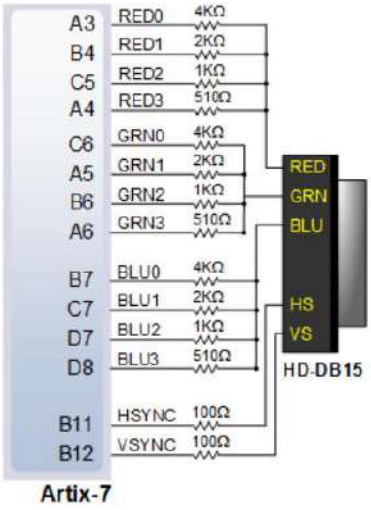

Fig. 3. VGA interface on Nexys 4 DDR

III. Perspectives of the nearest steps

If the aim is to design a DSP system with one or two analog inputs and one or two analog outputs, and suppose we try to process analog data with 12 bit ADC on moderate frequency, then all the power of Artix 7 platform with 100 MHz clock frequency and a little bit more will be quite handy. And maybe attaching couple of standalone ADCs and DACs with clock frequency close to 100 MHz can improve the characteristics of our system.

Besides, VGA channel utilization can establish monitoring of the signal in different forms – temporal, spectral, correlation, wavelet.

References

[1] Moiseev N.N. Mathematical problems of system analysis: [Proc. manual for universities on spec. “Apply Mathematics ”] / N. N. Moiseev. - M .: Science, 1981. - 487.

[2] Digital signal processing and MATLAB: proc. manual / A.I. Solonina, D.M. Klionsky, T.V. Merkucheva, S.N. Perov. - SPb .: BHV-Petersburg, 2013. – 512 pp., Ill . – (Educational literature for universities).

[3] V. Semenets. Designing digital systems using the VHDL language: studies. manual / V.V. Semenets, I.V. Khakhanova, V.I. Khakhanov; MES of Ukraine, KNURE. - Kharkov: KNURE, 2003. - 492 p.

[4] Semenets V. V. Technology of electronic equipment interconnections: studies. for universities / V. V. Semenets, John Kratz, I. Sh. Nevludov, V. A. Palagin. – H.: ed. SMITH, 2005. – 432 p. [Semenets V. V., Kratts J., Nevlyudov I. Sh., Palagin V. A].

[5] Nexys4™ FPGA Board Reference Manual.

[6] S. Sakalo, V. Semenets and O. Azarhov, *High frequencies in medicine (therapy and diagnostics): Teaching manual*. Kharkov: KNURE; Collegium, 2005, p. 264.

[7] V. Semenets, "Technical aspects for development laboratory base for learning FPGA and microcontroller systems," *2009 10th International Conference - The Experience of Designing and Application of CAD Systems in Microelectronics*, Lviv-Polyana, 2009, pp. 145-145.

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Approaches to Designing a Wireless Sensor Network Node

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***Abstract*—The object of the research is the hardware component for building a test platform for wireless sensor networks. The aim of the work is to develop a software and hardware test platform for wireless sensor networks. As a result of the analysis, the node structures, wireless sensor network modules, CC2530 peripherals were analyzed. A module based on the CC2530 PA was chosen as the hardware. Given to optimize the structure of the node for as one of approach to designing a wireless sensor network node. Also given report about difference in approach to designing nodes and uses areas.**

Keywords—approach, CC2530, software and hardware test platform, node, wireless sensor network

I. INTRODUCTION

This Wireless sensor networks (WSN) systems have a lot of problems like security, energy consumption, heterogeneity and other disadvantages that need be solved [1]. Therefore, it is quite difficult to design a sensor network node so that it satisfies the necessary criteria for optimality. If such a node is also used for testing and training, then additional requirements for the construction will be propose to, for example, as in articles of designing microprocessor systems [2] or embedded control systems [3]. Energy monitoring [4] is a key factor for the successful prolongation of life times each nodes in wireless sensor network, for examples reducing the power consumption of nodes [5]. Therefore, can set the task to optimize the structure of the node for as one of approach to designing a wireless sensor network node.

In conventional two-tiered WSN, sensors in each cluster transmit observed data to a fusion center via an intermediate supernode. This structure is vulnerable to supernode failure. A double supernode system model with a new coding scheme is proposed to monitor a binary data source [6]. One of design method of WSN node and gateway node for monitoring of data presented in article [7]. Each of the sensing nodes was composed of an ATmega128L micro-processor and a CC2420 transceiver module. Micro controller S3C2410X was used as the kernel of hardware platform in the gateway node [7].

Next good example of design node of WSN for aim at the problems existing in the information monitoring of the farmland environment such as the limited energy, low system stability and large monitoring area, a WSN node for rice field based on hybrid antenna is designed to realize the real-time on-line monitoring for the environmental parameters of rice fields in the network. As for the hardware, the node uses a STM32F103VET6 as a processing core, and a WLK01L39 RF chip is used in wireless communication module, while the sensor module is composed of the air temperature and humidity sensor, light intensity sensor and soil moisture sensor. As for the software, uC/OS-II is applied as an operational system to realize multitask scheduling running. The sensor node applies a mechanism as sleeping and waking up work modes to reduce power consumption. The current consumption of sensor nodes is 0.024mA under the sleeping mode, 32.32mA under the data collection, 26.25mA under data transmission and 21.95mA under the operating mode. The results of a long time networking experiment indicate that the average PLR (Packet Loss Rate) of network is 0.76%. In conclusion, the design of sensor node system is suitable for the real-time and stable monitoring of rice field [8]. The paper [9] introduces the basic structure of wireless sensor network node based on ARM, and it delivers a detailed analysis on the operating features and the CC2480 hardware interface of the ZigBee processor, what's more, it specifically talks about the implementation of the Linux driver of WSN nodes. The paper [10] propose a microcontroller based anti poaching system employing WSN technology, which is capable of detecting theft by monitoring the vibrations produced by the cutting of trees/branches using a 3 axis MEMS accelerometer. A low power MSP430F5529 microcontroller is used along with Xbee RF modules based on IEEE 802.15.4 Zigbee standards to communicate to a central server from a remote place. The embedded system architecture and the hardware/software designs are described in detail. Vibration data collected by various tests on wood and simulated using Labview.

In order to solve the problem of inflexible location, dead angle and large measurement error of the network node of the wire monitoring system for factory toxic gas leakage, a toxic gas monitoring and alarm system based on CC2530 wireless sensor network is designed [11]. Therefore, after analyzing the developed and designed nodes, can define several research tasks:

- optimize the structure of the node;
- selection of chip for WSN node;
- peripheral requirements development.

II. Optimization of Structure Nodes

At the moment, there are two basic solutions for constructing ZigBee nodes for wireless sensor networks. In the first case, the developer is encouraged to construct the hardware unit independently, using different microprocessors supporting the IEEE 802.15.4 radio interface.

The radio transceiver in IEEE 802.15.4 complies only with the functions of receiving and transmitting information over a radio channel and does not contain software that implements the ZigBee protocol stack. The software implementation of the ZigBee stack relies on an external microcontroller to which the transceiver chip connects to one of the standard interfaces, such as a serial peripheral interface (SPI) or a parallel interface. Additionally, the transceiver requires a bunch, which includes an antenna, a quartz resonator, as well as a small number of passive components. The use of such SoC (Systems on the crystal) or SiP (Integrated hybrid chips) performs all the functions for working with ZigBee as WSN node and a microcontroller to perform a user program, though it will be less energy efficient, but in turn will be able to provide greater flexibility to execute this program in terms of Input/Output, external interfaces, or have any specific functions. This option is not the most economical in terms of the cost of chips, but it does not require much effort in design development. In the case of using a platform in a single body (PiP), the design task in general consists only in the organization of the binding of this chip. The digamma of structure chip is shown on Fig. 1

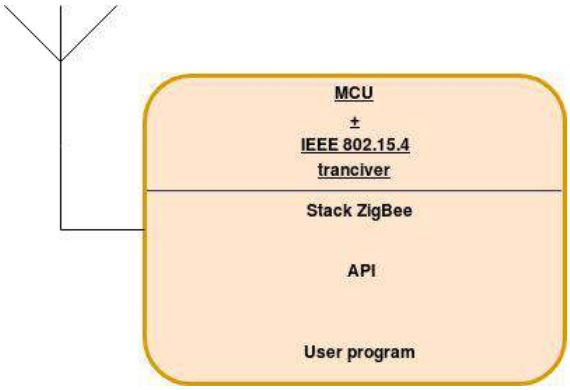

Fig. 1. Digamma of structure WSN node in one SoC

Another version with separate microcontroller with user program and radio transceiver. In this case the microcontroller has enough resources not only for realization the main functions of the program, but also the ZigBee stack. In this case, the chip The IEEE 802.15.4 radio transceiver interfaces with the base processor per means SPI interface. This structure is shown on Fig. 2.

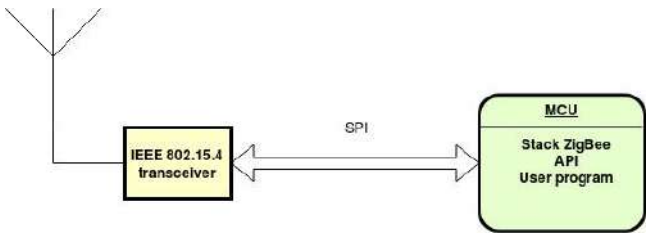

Fig. 2. Digamma of structure WSN node with separate radio transceiver and microcontroller with user program

The structure on Fig. 3 differs only in that there two microcontrollers are used: the first to implement the ZigBee stack, and the other to execute the user program, the data exchange is also carried out through the SPI. This option increases the overall power consumption.

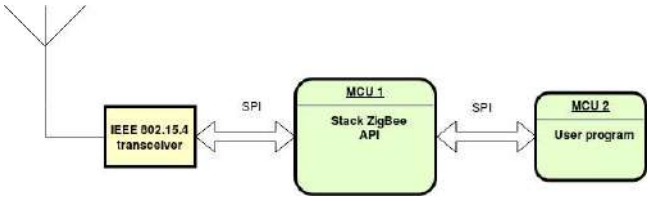

Fig. 3. Digamma of structure WSN node with two MCU and one transceiver

The closest case to the implementation of the one system on a chip is the system shown in Fig. 4, where separate microcontroller is used for user program.

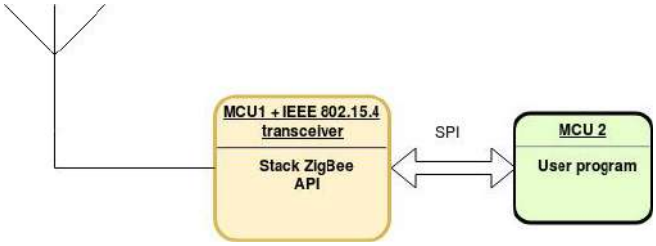

Fig. 4. Digamma of structure WSN node with one MCU for user program and one MCU with transceiver

After considering the peculiarities of the structure the node of wireless sensor networks, it should be noted difference between SiP and SoC approaches. Integrated hybrid chips, which combine in one case crystals of the "classic" radio transmitter and general purpose microcontroller. This solution allows you to place the ZigBee software stack directly in the built-in microcontroller memory and thereby significantly reduce load on an external microcontroller, which provides solution to the tasks of a particular application. These microcircuits require a minimum strap, including an antenna. Systems on the crystal - this type of chip actually replicate the capabilities of SiP, but unlike them and the transmitter receiver, and built-in the microcontroller is executed on one crystal. Some firms, such as Texas Instruments, called such crystals ZigBee processors. They interact with the external controller of the application in one of the standard interfaces (SPI, Universal Asynchronous Receiver (UART)) and allow loading in memory of network protocols of different complexity depending on the predicted the complexity and structure of the implemented network.

Therefore, we can conclude that WSN node in one SoC it is first step for optimization energy consumption of node and consequently, longer life time all network.

III. Prepare Selection of Chip for Wireless Sensor Network

There are many different modules to implement ZigBee networks. Each of them has its own features, both in terms of the hardware part and in terms of software in the form of various environments for working with these modules [12].

There are various modules based on the SoC CC2530 [13], in essence they are a board that hosts the CC2530 itself, an external quartz resonator, several passive components, an antenna connector (or built-in antenna) and outputs for connecting to other devices. The typical node of wireless sensor network can be constructed using a chip CC2530. This transceiver can be ready for prototyping by PCB board-module (Fig. 5).

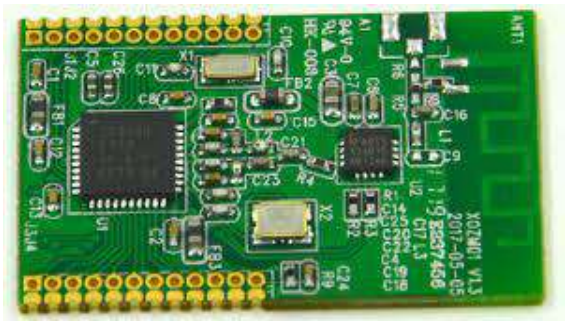

Fig. 5. PCB board-module base on chip CC2530

The use of ready-made modules is the easiest way to start working with ZigBee [14], since it does not require its own development, you only need to select the module with the required number of ports, the required data interfaces and related parameters. Such modules are often installed directly on the board with the necessary operating equipment, sensors or simply with port output. Company developers of these modules usually also make additional modules with different input / output devices, sensors and other related equipment. In addition, there are additional expansion cards (shield) designed to power the module itself, output ports on connectors, containing LEDs reflect the state of the module and additional buttons.

As an example of a debugging board for the ZigBee module can consider the CC2530 PCB base (Fig. 6) on ZigBee CC2530 Sensor (Fig. 7) from the company Texas Instruments which is designed for the modules CC2530EM.

Problems in the design of embedded systems were also considered earlier [15-17].

Fig. 6. Module base on chip CC2530

The ZigBee CC2530 Sensor debugging board contains:

- Full USB 2.0 interface;
- UART interface;
- LEDs and buttons;
- serial flash memory.

Fig. 7. ZigBee CC2530 Sensor

The CC2530 is a true system-on chip (SoC) solution for IEEE802.15.4, Zigbee and RF4CE applications [13].

IV. Using the Template Peripheral Requirements Development

The CC2530 contains many peripherals that provide everything to develop various applications [14]. The debugging interface uses I / O ports P21 (data) and P22 (synchronization) in debug mode. In this case, in the debug mode, the other 19 ports pins can be active, which gives a great opportunity to debug the module, while at the same time it can be connected to quite a few different devices. In other cases, the ports for debugging can work in the normal GPIO mode. In general, the debugging interface allows you to track all processes that occur in the module when it is in an active state (user program execution), and also to change the parameters of these processes (for example, values in registers) and in real time to observe changes in the work of the module.

The wiring diagram of the CC2530 is shown in Fig. 8. As can be seen in the figure, the CC2530 chip requires a very small number of external components, which greatly simplifies the development of a new product. The microcircuit is suitable for use in a variety of applications. For this, it is integrated as standard microcontroller peripherals: 8/16 bit timers; watchdog; ADC two USART modules with support for SPI and UART protocols; I / O ports (21 lines: 19x4 + 2x20 mA) and specialized: MAC timer (defined by the IEEE 802.15.4 standard), hardware support unit for the network protocol CSMA / CA, as well as random number generator and data encryption / decryption accelerator AES algorithm using a 128-bit key.

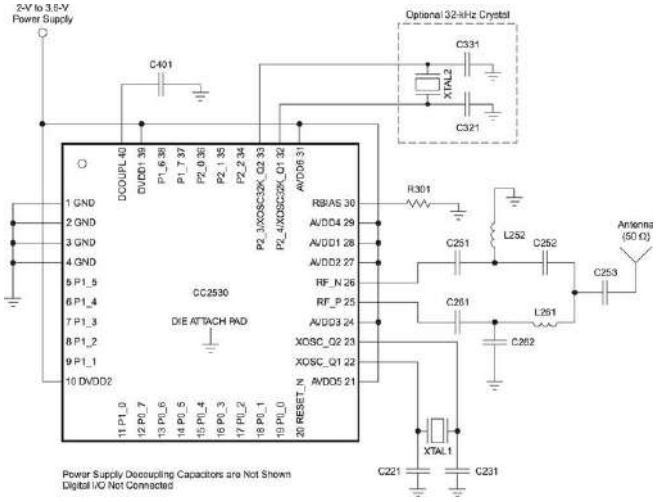

Fig. 8. Wiring diagram of the CC2530

V. CONCLUSION

The during of research, it was considered optimize the structure of the node, selection of chip for wireless sensor network node and discussion about peripheral requirements development. A module based on the CC2530 PA was chosen as the hardware. In article was noted that optimize of structure the wireless sensor network node as one of approach to designing a wireless sensor network with long life cycle.

REFERENCES

[1] C. Alvarado, F. Bosquez, Palacios and L. Córdoba, "Low-energy Adaptive Clustering Hierarchy protocol and optimal number of cluster head algorithm in a randomized wireless sensor network deployment," 2017 International Conference on Electrical, Electronics, Communication, Computer, and Optimization Techniques (ICEECCOT), Mysuru, 2017, pp. 1-4. oi: 10.1109/ICEECCOT.2017.8284632.

[2] V. Semenets, "Technical aspects for development laboratory base for learning FPGA and microcontroller systems," 2009 10th International Conference - The Experience of Designing and Application of CAD Systems in Microelectronics, Lviv-Polyana, 2009, pp. 145-145.

[3] P. Galkin, “Razrabotka laboratornogo kompleksa po izucheniyu vstraivaemyih sistem upravleniya i promyishlennoy avtomatizatsii [Development of a laboratory complex for the study of embedded control systems and industrial automation],” Materials of the 21st International Youth Forum "Radio Electronics and Youth in the 21st Century", April 25-27, 2017 Conference "Automated systems and computerized technologies of radio-electronic instrument-making", Kharkiv, KNURE, vol. 2, P.94-95. (In Russian).

[4] P. Galkin. “Analiz energopotrebleniya uzlov besprovodnih sensornih setei [Analysis of power consumption of nodes of wireless sensor networks],“ ScienceRise, no.2 pp 55-61, 2014. (In Russian).

[5] P. Galkin, "Model of Reducing the Power Consumption for Node of Wireless Sensor Network in Embedded Control Systems," 2018 International Scientific-Practical Conference Problems of Infocommunications. Science and Technology (PIC S&T), Kharkiv, Ukraine, 2018, pp. 252-256. doi: 10.1109/INFOCOMMST.2018.8631891.

[6] A. Razi, F. Afghah and A. Abedi, "Power Optimized DSTBC Assisted DMF Relaying in Wireless Sensor Networks with Redundant Super Nodes," in IEEE Transactions on Wireless Communications, vol. 12, no. 2, pp. 636-645, February 2013. doi: 10.1109/TWC.2012.121712.111968.

[7] Daozong Sun, Weixing Wang, Jianqing Lu and Zuanhui Lin, "Design of WSN nodes and network performance analysis in a tea plantation," IET International Conference on Wireless Sensor Network 2010 (IET-WSN 2010), Beijing, 2010, pp. 144-147. doi: 10.1049/cp.2010.1043.

[8] H. Chen, W. Wang, B. Sun, J. Weng and F. Tie, "Design of a WSN Node for Rice Field Based on Hybrid Antenna," 2017 International Conference on Computer Network, Electronic and Automation (ICCNEA), Xi'an, 2017, pp. 276-280. doi: 10.1109/ICCNEA.2017.101.

[9] J. Jinwu, C. Lecai and L. Renjia, "The Design of Linux Driver of WSN Nodes Based on ARM," 2011 Fourth International Conference on Intelligent Computation Technology and Automation, Shenzhen, Guangdong, 2011, pp. 761-764. doi: 10.1109/ICICTA.2011.477.

[10] S. Gaikwad, R. Patil, A. Khandare and A. Rai, "Design WSN node for protection of forest trees against poaching based on ZigBee," 2015 IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT), Bangalore, 2015, pp. 1-4. doi: 10.1109/CONECCT.2015.7383911.

[11] C. Ma, N. Li, X. Pang, S. Wang and Y. Yang, "Hardware Design of Factory Toxic Gas Leakage Monitoring System Based on CC2530," 2018 10th International Conference on Intelligent Human-Machine Systems and Cybernetics (IHMSC), Hangzhou, 2018, pp. 243-245. doi: 10.1109/IHMSC.2018.10162.

[12] M. Khanafer, M. Guennoun and H. T. Mouftah, "A Survey of Beacon-Enabled IEEE 802.15.4 MAC Protocols in Wireless Sensor Networks," in IEEE Communications Surveys & Tutorials, vol. 16, no. 2, pp. 856-876, Second Quarter 2014. doi: 10.1109/SURV.2013.112613.00094.

[13] Second Generation System-on-Chip Solution for 2.4 GHz IEEE 802.15.4 / RF4CE / ZigBee [Electronic resource] / Texas Instruments.– Available at: www/ URL: http://www.ti.com/lit/ds/symlink/cc2530.pdf.

[14] F. Knutti, N. Tobler and H. Mathis, "Low-power voting device for use in education and polls employing TI's CC2530 RF CHIP," 2014 6th European Embedded Design in Education and Research Conference (EDERC), Milano, 2014, pp. 221-224. doi: 10.1109/EDERC.2014.6924392.

[15] P. Galkin, L. Golovkina and I. Klyuchnyk, "Analysis of Single-Board Computers for IoT and IIoT Solutions in Embedded Control Systems," 2018 International Scientific-Practical Conference Problems of Infocommunications. Science and Technology (PIC S&T), Kharkiv, Ukraine, 2018, pp. 297-302. doi: 10.1109/INFOCOMMST.2018.8632069.

[16] T. Nimi and P. Samundiswary, "Comparative analysis of ZigBee network with tree and mesh topology for different range of frequencies," 2017 2nd International Conference on Communication and Electronics Systems (ICCES), Coimbatore, 2017, pp. 560-564. doi: 10.1109/CESYS.2017.8321140.

[17] P. Galkin, "Analysis models of collection data in wireless sensor networks," 2016 Third International Scientific-Practical Conference Problems of Infocommunications Science and Technology (PIC S&T), Kharkiv, 2016, pp. 233-236. doi: 10.1109/INFOCOMMST.2016.7905392.

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Review of Seventh Series FPGA Xilinx

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***Abstract*—The work of the Xilinx FPGA of the 7th series was reviewed, as well as a comparative description of its families.**

Keywords—FPGA, DSP, XADC, Xilinx, Spartan-7, Artix-7, Kintex-7, Virtex-7.

I. INTRODUCTION

Xilinx FPGAs are widely used today to solve problems of varying complexity. The FPGA of the 7th series of the Xilinx company combines four families [1]-[5]:

- Spartan-7,
- Artix-7,
- Kintex-7,
- Virtex-7.

These FPGA Series 7 series cover a wide range of system requirements, from low cost chips to mass production devices to ultra-high integration for high performance digital signal processing systems with high bandwidth. FPGA data has high-speed bandwidth, a large number of logical elements, the ability to process signals for a variety of digital devices [5]-[9].

II. THE MAIN FEATURES OF THE SERIES

The main features of the FPGA series of the 7th series of the firm Xilinx, by families [1]-[5]:

- FPGA Spartan-7 family: well-optimized for its low cost, low power consumption and high performance, I/O, has a compact placement on the board, making this type of FPGA small size;
- Artix-7 FPGA family: optimized and flexible to create low-power devices; are used to create devices that require serial-type external peripherals with high DSP bandwidth. This type of FPGA provides the lowest cost of manufacturing (total cost of materials for manufacturing) to create high-performance, sensitive to the cost of materials of digital devices;
- Kintex-7 FPGA family: Designed and optimized for the best performance of the developed digital devices, with a 2-fold improvement in performance compared to previous generations at a low price;
- Virtex-7 FPGA family: Designed and optimized for the best performance of developed digital devices, with a 2-fold improvement in performance compared to previous generations at a low price.

Comparative FPGA Performance of the 7th Series of Xilinx by Family:

- the number of a logical elements: Spartan-7 - 102000; Artix-7 - 215000; Kintex-7 - 478000; Virtex-7 - 1955000;
- the size of the RAM unit: Spartan-7 - 4.2 MB; Artix-7 - 13 MB; Kintex-7 -34 MB; Virtex-7 -68 MB;
- 3) the number of DSP Slices: Spartan-7 - 160; Artix-7 - 740; Kintex-7 - 1,920; Virtex-7 - 3600;
- DSP performance. Measured in GMAC per unit time, where GMAC - Giga multiply - accumulate operations, the number of operations per second: Spartan-7 - 176 GMAC / s; Artix-7 - 929 GMAC / s; Kintex-7 - 2845 GMAC / s; Virtex-7 - 5335 GMAC / s;
- MicroBlaze processor. Measured in DMIPs, where Dhrystone Million Instructions Per second, or there are millions of operations per time unit: Spartan-7 - 260 DMIPs; Artix-7 - 303 DMIPs; Kintex-7 - 438 DMIPs; Virtex-7 - 441DMIPs;
- number of transceivers (devices for transmission and reception of signals): Spartan-7 - absent; Artix-7 - 16 pcs .; Kintex-7 - 32 pcs .; Virtex-7 -96 pcs .;
- transceiver speed: Spartan-7 is absent; Artix-7 - 6.6 Gb / s; Kintex-7 - 12.5 GB / s; Virtex-7 - 28.05 Gb / s;

- Serial bandwidth: Spartan-7 is absent; Artix-7 - 221Gb / s; Kintex-7 - 800 Gb / s; Virtex-7 -2 784 GB / s;
- programmable logic controller (PLC) interface: Spartan-7 is absent; Artix-7 - x4 Gen2; Kintex-7 - x8 Gen2; Virtex-7 - x8 Gen3;
- memory interface: Spartan-7 - 800 Mb / s; Artix-7 - 1,066 Mb / s; Kintex-7 - 1,866 Mbps; Virtex-7 -1 866 Mb / s;
- number of input / output elements: Spartan-7 - 400 units; Artix-7 - 500pcs .; Kintex-7 -500 pcs .; Virtex-7 -1200;
- the voltage consumption of input / output elements: Spartan-7 - 1.2-3.3 V; Artix-7 - 1.2-3.3V; Kintex-7 - 1.2-3.3V; Virtex-7 - 1.2-3.3 V.

The Xilinx Series 7 FPGA family is based on the high-k metal gate (HKMG), a modern, high-performance, low-power 28nm technology.

The Xilinx Series 7 FPGA family provides a significant increase in system performance with up to 2.9 TB / s throughput, about two million logical elements, as well as 5.3 TMAC / s DSPs, while consuming 50% less power than digital devices built on the basis of the previous generation of the FPGA family, which offers a real alternative to the use of ASSP and ASIC. Xilinx's 7th Series FPGA family has: Dual 12-Bit Analog / Digital Converters (XADC) for general purpose, with a productivity of 1 million samples per second; built-in sensors for temperature and voltage control; DSP blocks with a 25x18 multiplier, 48-bit battery and a promisor for high-performance filtering, including the possibility of optimally constructing filters with symmetric coefficients; control and synchronization units for synchronization signals, which provide high signal accuracy and low jitter level; A wide set of configuration modes, including the ability to encrypt the configuration sequence using the AES (256 bit) algorithm with HMAC / SHA-256 authentication; built-in module for detecting and correcting a one-time error. All types of cases of the 7th series are available in "lead-free" performance (Pb-free), and some types are also available in "lead" performance.

III. Conclusions

All Xilinx Series 7 FPGA chips have a common architecture that is organized in the form of columns of function blocks of the same type. Such an architecture is called an optimized silicon modular block. In addition, the Xilinx stack silicon interconnect technology used on some Virtex-7 chipsets allows the FPGA architecture to be introduced at the next structural level, making it possible to create a very high density and performance FPGA.

According to the representatives of the Xilinx company in FPGA, the 7th series embodies all the world's achievements in the field of FPGA architecture development.

References

[1] "Spartan-7 FPGAs Data Sheet:DC and AC Switching Characteristics. Product Specification. DS189 (v1.9) March 13, 2019", Xilinx.com, 2019. [Online]. Available: https://www.xilinx.com/support/documentation/data_sheets/ds189-spartan-7-data-sheet.pdf. [Accessed: 15- Jun- 2019].

[2] "Artix-7 FPGAs Data Sheet:DC and AC Switching Characteristics. Product Specification. DS181 (v1.25) June 18, 2018", *Xilinx.com*, 2018. [Online]. Available: https://www.xilinx.com/support/documentation/data_sheets/ds181_Artix_7_Data_Sheet.pdf. [Accessed: 15- Jun- 2019].

[3] "Kintex-7 FPGAs Data Sheet:DC and AC Switching Characteristics. Product Specification. DS182 (v2.18) June 28, 2019", *Xilinx.com*, 2019. [Online]. Available: https://www.xilinx.com/support/documentation/data_sheets/ds182_Kintex_7_Data_Sheet.pdf. [Accessed: 15- Jun- 2019].

[4] "Virtex-7 T and XT FPGAs Data Sheet:DC and AC Switching Characteristics. Product Specification. DS183 (v1.28) March 13, 2019", *Xilinx.com*, 2019. [Online]. Available: https://www.xilinx.com/support/documentation/data_sheets/ds183_Virtex_7_Data_Sheet.pdf. [Accessed: 15- Jun- 2019].

[5] "7 Series FPGAs Data Sheet: Overview. Product Specification. DS180 (v2.6) February 27, 2018", *Xilinx.com*, 2018. [Online]. Available: https://www.xilinx.com/support/documentation/data_sheets/ds180_7Series_Overview.pdf. [Accessed: 15- Jun- 2019].

[6] "7 Series Product Tables and Product Selection Guide", *Xilinx.com*, 2019. [Online]. Available: https://www.xilinx.com/support/documentation/selection-guides/7-series-product-selection-guide.pdf. [Accessed: 15- Jun- 2019].

[7] "7 Series DSP48E1 Slice. User Guide. UG479 (v1.10) March 27, 2018", *Xilinx.com*, 2018. [Online]. Available: https://www.xilinx.com/support/documentation/user_guides/ug479_7Series_DSP48E1.pdf. [Accessed: 15- Jun- 2019].

[8] "7 Series FPGAsConfiguration. User Guide. UG470 (v1.13.1) August 20, 2018", *Xilinx.com*, 2018. [Online]. Available: https://www.xilinx.com/support/documentation/user_guides/ug470_7Series_Config.pdf. [Accessed: 15- Jun- 2019].

[9] V. Soloviev, *Architecture of the FILM of the firm XILINX: CPLD and FPGA of the 7th series*. Moscow: Hotline - Telecom, 2016, p. 392.

[10] Svyd I.V., Litvinenko O.V., Bilotserkivets O.G. Features of designing digital devices based on Xilinx FPGA in CAD Vivado HLx Design Suite. // *Specialized Exhibition «KharkivProm Days. Production and efficiency ". Collection of materials of the forum section "Automation, electronics and robotics. Development Strategies and Innovative Technologies »*. - Kharkiv, KNURE, Exhibition Company ADT, 2019. - P. 43-44.

[11] Semenets V.V. *Technology of interconnection of electronic equipment: a university textbook* / V.V. Semenets, John Kratz, I.Sh. Nevlyudov, V.A. Palagin. - X.: ed. SMIT, 2005 - 432 p.

[12] V. Semenets, "Technical aspects for development laboratory base for learning FPGA and microcontroller systems," *2009 10th International Conference - The Experience of Designing and Application of CAD Systems in Microelectronics*, Lviv-Polyana, 2009, pp. 145-145.

[13] S. Sakalo, V. Semenets and O. Azarhov, *High frequencies in medicine (therapy and diagnostics): Teaching manual*. Kharkov: KNURE; Collegium, 2005, p. 264.

[14] O. Avrunin, S. Sakalo and V. Semenetc, "Development of up-to-date laboratory base for microprocessor systems investigation," *2009 19th International Crimean Conference Microwave & Telecommunication Technology*, Sevastopol, 2009, pp. 301-302.

[15] V. Semenets, V. Kauk, O. Avrunin. "The advanced technology of remote training at the initial process" ["Vprovadjennya tehnologiy dystantsiynogo navchannya u navchalnii protses"], High School, 2009. – No. 5 .– P. 40– 45.

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Intelligent Lighting Control and Management System

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***Abstract*—This paper discusses the features of building an automated lighting control system. The architecture of the automated system is given. The block diagram is considered and its components are described. The principle of interaction of intelligent devices with the server is given. Presented the rationale and benefits from the introduction of such a system.**

Keywords—light control, intelligent, led, network module, monitoring, server, IIoT

I. Introduction

At the moment, there are many organizations with no control system and electricity accounting. Installation of this automated lighting control system does not require global interference with the interior of the room. Automated lighting control systems is a complex product with a modular structure and a versatile control program for any task. Implementation of this solution helps to save energy by:

- control of level of external illumination and presence of people in the room;
- automatic maintenance of the required level of illumination in the workplace, regardless of time of day or weather conditions;
- the use of smart next lighting to increase the safety of workers at the expense of.

The peculiarity of this system is the possibility of phased and economic modernization of the obsolete lighting system through the commissioning of separate lighting devices of the structural divisions of the enterprise. Due to the connection of special control modules you can use conventional light bulbs as part of the intelligent lighting control system.

The financial costs of installing and implementing the system will be paid back in 3 to 8 years, depending on the type of organization. The enterprise will be able to save up to 60% on electricity costs.

II. Structure and Principle of the Automated Lighting Control System

The system consists of: intelligent lighting modules with built-in current and lighting sensors, with the possibility of wired or wireless control; modular light sensors for controlling light levels in the workplace; network module; local or cloud server; a control program for managing the operation of the system and viewing statistics.

Fig. 1 shows the architecture of the automated system.

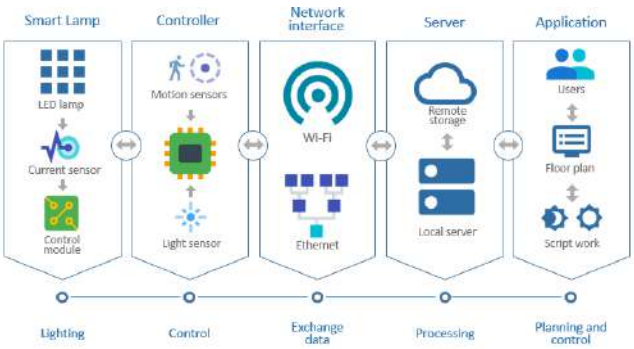

Fig. 1. Architecture of the automated system

Fig. 2 shows a schematic diagram of an automated lighting control system.

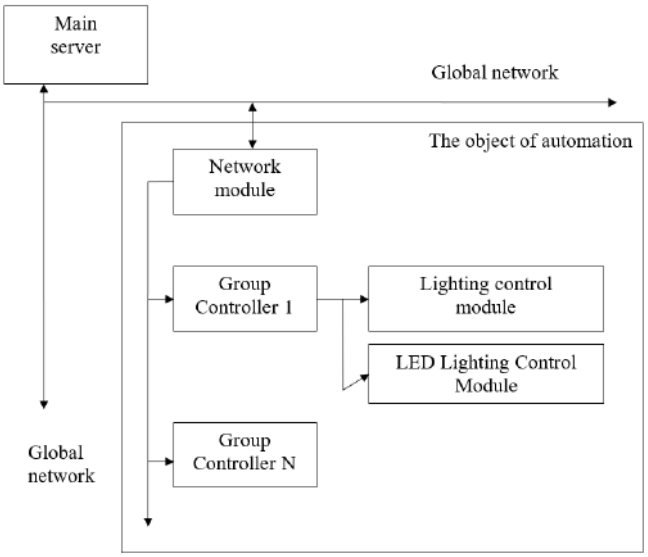

Fig. 2. The block diagram of an automated lighting control system

The structure of the automated system includes:

- intelligent lighting control modules of different power and operating principle (LED lamps, fluorescent lamps, incandescent lamps);
- controlling controller for the management of a group of fixtures;
- network controller, which is the gateway between local lighting devices and the global network;
- emergency lighting control module and integration into automated security system.

Intelligent light control modules are separate hardware devices based on microcontrollers with built-in transceiver (with wired or wireless transmission of information).

The network module is designed to control an automated lighting control system. This module is an intermediate link between the main server and directly the lighting control modules on the object.

Fig. 3 shows the principle of the interaction of the transmitter with the server.

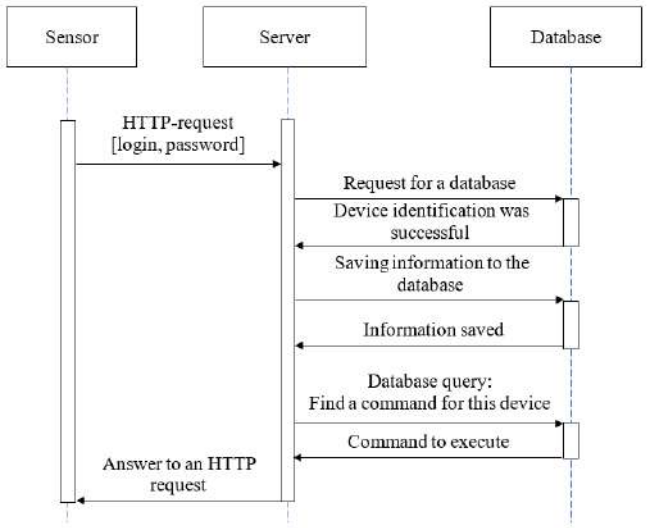

Fig. 3. The principle of the interaction of the transmitting device with the server

The network module is a gateway between the group controller that is installed on the automation object and the Internet.

Network module features:

- receiving requests from the server;
- processing received information;
- formation of packages and broadcasting of requests to the industrial network of the object of automation of lighting control;
- receive a response from the controllers of automation of lighting control;
- build response and broadcast it to the main server.

Intelligent devices send statistics to the server and expect reciprocal commands from it. In standby, the server waits for requests from controllers to read their status and save them to the database. When the device accesses the server, the latter disassembles the received message, decodes it, and records the received information to the database.

The software part of the server consists of the interface and controllers. The interface allows you to get information about the state of sensors and other devices, and manage them. The interface also allows you to change these parameters.

III. Conclusions

The proposed intelligent lighting control system provides the opportunity to save on the company's financial costs due to a significant reduction in electricity consumption while improving working conditions for employees.

Differences of this system from similar:

- universal solution for an object of any complexity due to;
- use of modular scalable software on the basis of micro-services;
- reducing the range of hardware to several units, which simplifies the configuration, configuration and support;
- automatic reconfiguration of the smart device network.

The use of intelligent control makes it possible to quickly detect malfunctions of lighting devices and increase the speed of response to it. Centralized control, accounting and control of the state of lighting devices, as well as control and accounting of the consumption of electricity by the lighting system, can significantly reduce the level of energy consumption.

References

[1] O. Hersent, The Internet of Things: Key Applications and Protocols. D. Boswarthick, O. Elloumi. - Wiley, 2012. - 370 p.

[2] Gong, Y.; Han, P. Research on energy-saving scheme based on LED street lamp management-system. Appl. Mech. Mater. 2014, pp. 448–453, 2850–2855.

[3] F. Behmann, Collaborative Internet of Things (C-IoT): for Future Smart Connected Life and Business. Kwok Wu K. - Wiley, 2015. - 304 p.

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Matlab Use in Design of Digital Systems on the FPGA in CAD Xilinx VIVADO

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***Abstract*—Matlab is a high-level language and an interactive environment that can help to analyze data, develop algorithms, create models and applications. There are many extensions for Matlab. One of these extensions is the Xilinx System Generator for DSP, a key component of the Xilinx specialized digital signal processing platform, that allows to implement DSP algorithms with less time costs than traditional RTL design.**

Keywords—MATLAB, VHDL, XILINX, VIVADO.

I. INTRODUCTION

Matlab is a high-level language and an interactive environment for programming, numerical calculations, visualization of results, technical calculations. Has a large number of packages of application extensions. With Matlab you can analyze data, develop algorithms, create models and applications.

Matlab is widely used in the following areas:

- working of signals and communications;
- image and video processing;
- system of management;
- automation of testing and measurements, and so on.

The Matlab system consists of the following main parts:

MATLAB matrix (matrix and array language);

- MATLAB environment;
- controlling graphics (high-level teams for visualizing two- and three-dimensional data, etc.);
- built libraries and numerous extensions packages (including Simulink);
- program interface (a library that allows you to use programs in C and Fortran that interact with MATLAB).

For Matlab there are many extensions (Toolboxes and Blocksets) for different industries. One of these extensions is the Xilinx System Generator for DSP, a key component of the Xilinx specialized digital signal processing platform (DSP).

II. MATLAB XILINX DSP SYSTEM GENERATOR

System Generator for DSP is the industry-leading tool for developing high-performance digital signal processing systems built by Xilinx's FPGA and SoC. System Generator for DSP allows you to implement DSP algorithms with less time costs than traditional RTL design.

System Generator for DSP provides:

- the development of high-performance parallel systems on the most advanced FPGA;
- system simulation and automatic code generation from Simulink and MATLAB;
- integration of RTL code, IP modules, MATLAB codes and hardware components into the DSP system.

System Generator for DSP is included in the Vivado System Edition. Using System Generator for DSP developers with small design experience allows to quickly create high-quality DSP projects at a lower cost compared to traditional RTL design.

Simulink System Generator for DSP allows the developer to access the set of Xilinx FPGA hardware components and, at the same time, can use standard Simulink units such as signal sources and receivers, logic and math operations, subsystem blocks, and more. And System Generator libraries contain blocks that represent elements of communication, logic management, signal processing, memory work, and built-in microprocessor devices, and more.

III. Features and Benefits of System Generator for DSP

Key Features and Benefits of System Generator for DSP:

A. DSP simulation

DSP-simulation. Creating and debugging high-performance DSP systems using optimized RTL IP addresses of Xilinx as blocks in Simulink for signal processing (eg FIR, FFT filters), error correction (for example, Viterbi decoder, Reed-Solomon encoder / decoder), arithmetic, memory such as FIFO, RAM, ROM, and digital logic. Allows access to Simulink's DSP48 primitives for high frequencies.

B. Bit and cyclic realization with floating and fixed-point

Bit and cyclic implementation with floating and fixed-point. The system generator supports bitwise and cyclic precision with fixed point and bit and clock accuracy with single, dual and user-defined floating-point accuracy.

C. Automatic generation of code VHDL or Verilog, or Packaged IP from Simulink

Automatic generation of VHDL or Verilog code, or Packaged IP from Simulink. Implementation of behavioral (RTL) generation and targeting to specific Xilinx IP cores with Xilinx Blockset. Pack the project as an IP kernel, which can be added to the Vivado IP directory for use in another project, allowing you to reuse the design and share the developed model.

D. Hardware co-simulation

Hardware common simulation. The code generation option, which allows validation and acceleration of simulation by compiling projects into FPGA hardware, which can be used in a Simulink simulation loop to test the running equipment and simulink simulation acceleration. System Generator supports Ethernet (10/100 / Gigabit) and JTAG communications between the hardware platform and Simulink for supported platforms and platforms.

E. Strings and resource analysis

Track and analysis of resources. Checking the synchronization closure and use of resources of your projects (after synthesis or after implementation) and mapping the results with the Model Generator system into Simulink through cross-sensing speeds up the process of project refinement, which increases productivity or detects synchronization failures.

Integrated with Kintex®-7, Virtex®-7, Zynq®-7000, Artix®-7, Kintex UltraScale ™, Kintex UltraScale +, Virtex UltraScale, Virtex UltraScale +, Zynq UltraScale + RFSoC.

IV. Conclusions

Using System Generator, that included in the Vivado System Edition for DSP, allows for developers with small design experience, to quickly create high-quality DSP projects at a lower cost compared to traditional RTL design.

References

[1] V. Soloviev, *Architecture of the FILM of the firm XILINX: CPLD and FPGA of the 7th series*. Moscow: Hotline - Telecom, 2016, p. 392.

[2] Semenets V.V. *Technology of interconnection of electronic equipment: a university textbook* / V.V. Semenets, John Kratz, I.Sh. Nevlyudov, V.A. Palagin. - X.: ed. SMIT, 2005 - 432 p.

[3] V. Semenets, "Technical aspects for development laboratory base for learning FPGA and microcontroller systems," *2009 10th International Conference - The Experience of Designing and Application of CAD Systems in Microelectronics*, Lviv-Polyana, 2009, pp. 145-145.

[4] S. Sakalo, V. Semenets and O. Azarhov, *High frequencies in medicine (therapy and diagnostics): Teaching manual*. Kharkov: KNURE; Collegium, 2005, p. 264.

[5] O. Avrunin, S. Sakalo and V. Semenetc, "Development of up-to-date laboratory base for microprocessor systems investigation," *2009 19th International Crimean Conference Microwave & Telecommunication Technology*, Sevastopol, 2009, pp. 301-302.

[6] V. Semenets, V. Kauk, O. Avrunin. "The advanced technology of remote training at the initial process" ["Vprovadjennya tehnologiy dystantsiynogo navchannya u navchalnii protses"], High School, 2009. – No. 5 .– P. 40– 45.

[7] Svyd I.V., Litvinenko O.V., Bilotserkivets O.G. Features of designing digital devices based on Xilinx FPGA in CAD Vivado HLx Design Suite. // *Specialized Exhibition «KharkivProm Days. Production and efficiency ". Collection of materials of the forum section "Automation, electronics and robotics. Development Strategies and Innovative Technologies »*. - Kharkiv, KNURE, Exhibition Company ADT, 2019. - P. 43-44.

[8] O.Avrunin, T. Nosova, V. Semenets. *Fundamentals of VHDL language for the design of digital devices in the FPGA: tutorial* ./ Ministry of Education and Science of Ukraine, Kharkiv National University of Radio Electronics. - Kharkiv: KNURE, 2018. - 196 p.

[9] "Spartan-7 FPGAs Data Sheet:DC and AC Switching Characteristics. Product Specification. DS189 (v1.9) March 13, 2019", Xilinx.com, 2019. [Online]. Available: https://www.xilinx.com/support/documentation/data_sheets/ds189-spartan-7-data-sheet.pdf. [Accessed: 17- Jun- 2019].

[10] "Artix-7 FPGAs Data Sheet:DC and AC Switching Characteristics. Product Specification. DS181 (v1.25) June 18, 2018", *Xilinx.com*, 2018. [Online]. Available: https://www.xilinx.com/support/documentation/data_sheets/ds181_Artix_7_Data_Sheet.pdf. [Accessed: 17- Jun- 2019].

[11] "Kintex-7 FPGAs Data Sheet:DC and AC Switching Characteristics. Product Specification. DS182 (v2.18) June 28, 2019", *Xilinx.com*, 2019. [Online]. Available: https://www.xilinx.com/support/documentation/data_sheets/ds182_Kintex_7_Data_Sheet.pdf. [Accessed: 17- Jun- 2019].

[12] "Virtex-7 T and XT FPGAs Data Sheet:DC and AC Switching Characteristics. Product Specification. DS183 (v1.28) March 13, 2019", *Xilinx.com*, 2019. [Online]. Available: https://www.xilinx.com/support/documentation/data_sheets/ds183_Virtex_7_Data_Sheet.pdf. [Accessed: 17- Jun- 2019].

[13] "7 Series FPGAs Data Sheet: Overview. Product Specification. DS180 (v2.6) February 27, 2018", *Xilinx.com*, 2018. [Online]. Available: https://www.xilinx.com/support/documentation/data_sheets/ds180_7Series_Overview.pdf. [Accessed: 17- Jun- 2019].

[14] "7 Series Product Tables and Product Selection Guide", *Xilinx.com*, 2019. [Online]. Available: https://www.xilinx.com/support/documentation/selection-guides/7-series-product-selection-guide.pdf. [Accessed: 17- Jun- 2019].

[15] "7 Series DSP48E1 Slice. User Guide. UG479 (v1.10) March 27, 2018", *Xilinx.com*, 2018. [Online]. Available: https://www.xilinx.com/support/documentation/user_guides/ug479_7Series_DSP48E1.pdf. [Accessed: 17- Jun- 2019].

[16] "7 Series FPGAsConfiguration. User Guide. UG470 (v1.13.1) August 20, 2018", *Xilinx.com*, 2018. [Online]. Available: https://www.xilinx.com/support/documentation/user_guides/ug470_7Series_Config.pdf. [Accessed: 17- Jun- 2019].

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Application of Xilinx Series 7 on FPGA (XADC)

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***Abstract*—FPGA systems development has long ceased to be limited to simply writing code in hardware description languages (HDL); and as the number of logical resources and the complexity of projects increase, approaches to designing systems on FPGAs have been repeatedly revised. One of the turns of development was the introduction of soft processors into projects — essentially ordinary microprocessors but assembled on FPGA resources. Unfortunately, despite the relative difficulty of developing software-processor systems, many trying to "raise" this topic face difficulties in mastering, because they do not know where to find the necessary information.**

Keywords—programming environment, VIVADO, FPGA, VHDL, XADC, boards, Basys 3

I. Introduction

The purpose of the article is to give a general idea of the stages of assembly of the processor system based on the Microblaze soft processor, using the Xilinx Vivado environment. Unfortunately, within the framework of a single article, it is difficult to describe all the diversity of the process of building soft-processor systems on an FPGA and to describe in detail all the "subtle" moments accompanying it, but it is necessary to start with something. In the article, we will look at connecting XADC, various memory controllers, external interfaces, analyze the operation of components connecting MicroBlaze with peripherals, and much more. But it will be a little later, but for starters.

Today, there is an acute problem of the development of technologies in different spheres of human life. And one of the most developed is the service sector of people. But the goal of the project is to develop a method for implementing the analog-to-digital signal conversion. This topic is relevant because a person needs to convert signals into one form or another. And to realize a very easy way was our goal.

Therefore, we propose using Basys 3 with the use of MicroBlaze. A tutorial for university students with a detailed explanation of each step in the work of VIVADO (programming environment) or in the creation of the simplest schemes is attached to this project.

Using this programming environment, it is possible to implement various schemes for measuring temperature, voltage, alarms (if you connect a speaker to the board) or a normal flashing LED.

II. Goals And Results

The development of any processor system built on FPGA resources consists of two fundamental parts: the assembly of the hardware platform HW - hardware, and the development of the SW - software executable program.

The HW part is developed in the Xilinx Vivado environment in the IP Integrator module (Vivado IPI) and is the creation of the actual instance (or several for a multiprocessor system) of the MicroBlaze core, connecting it with the necessary peripherals and address space allocation. Code development for MicroBlaze is performed in Xilinx SDK in assembly language or C / C ++.

The assembly process of the HW part in Vivado IPI is in many ways similar to that in the previous Xilinx environments — ISE and PlanAhead (where the XPS utility, Xilinx Platform Studio, was used for this), but has a number of differences from it. General principles have been preserved, the differences are found, for the most part, in the representation of the system. There are no differences from the software (SW-part) side: the Xilinx SDK is also used to work with the software part.

The development of a hardware platform begins with the launch of Vivado and the creation of a project.

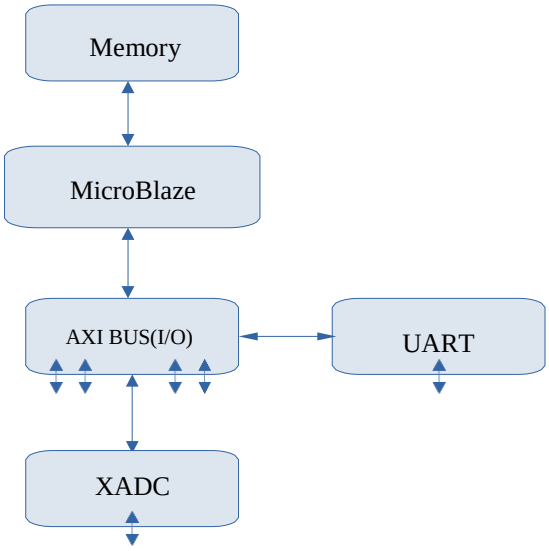

Fig. 1. Block Diagram of Final Scheme of The Project.

Full components in the scheme:

- *clk_wiz_1* – (Clocking wizard) - helps us to manage the clocker frequency and connect it to the other elements which requires;
- *xlconstant_0* – (Constant) applied a constant value (1) to make a trick with the block "rst_clk-wiz_100m";

- *rst_clk-wiz_10Om* – (Processing System Reset) using to reset the entire Microblaze system. This block is required to use Microblaze, but we are not using any "Reset" function;
- *MicroBlaze* – functional block of Microblaze processor;
- *Microblaze_0_axi_periph* – (AXI Interconnect) helps the system to configure the AXI hub, to process the input values;
- *microblaze_0_local memory* – (Local Memory) provides processor to save the data;
- *xadc_wiz_0* – (XADC Wizard) special functional block which provides us the ADC data;
- *axi-gpio_0* – (AXI GPIO) AXI bus module, which getting data from digital inputs (16 switches);
- *axi_uarllite_0* – (AXI uarllite) AXI bus module, provides a connection to PC using UART interface;
- *axi_gpio_1* – (AXI GPIO) AXI bus module, which putting data to digital outputs (16 LEDs);
- *reverse_v1_0* – (Reverse_0) an example of VHDL module to invers the output signal.

The final section of the code involved reading the ADC values and converting to voltages as well as reading the digital input. All of these inputs that were read in were then printed to the serial port in a form such that the raw ADC, voltage value, and digital value could all be read and continuously updated.This was all done in an infinite loop so that measurements were always being made and then reported.

As achievements using GPIO we understood and organized the abilities of AXI hub. How to control and use a digital I/O in C code (via Microblaze). We can read/write the state of digital inputs/outputs like 7-segment dispay, switches, digital I/O, keys, leds, etc. Using special IP-Blocks like UART-LITE helps us to configure the UART port. Also to turn on the XADC, we should use a special block XADC Wizard. It provides the input voltage stage and temperature of microprocessor (FPGA). In our reality, because of the differences between Zynq and Microblaze architectures, Vivado can't provide us same libraries for both of components, and that is the problem what we met. We could get the voltage value of the components, but it should be correctly plugged because we use positive and negative signal in XADC port.

NOTE: The coupled routing and the anti-alias filters might limit the data speeds when used for digital signals. The XADC core within the Artix-7 is a dual channel 12-bit analog-to-digital converter capable of operating at 1 MSPS. Either channel can be driven by any of the auxiliary analog input pairs connected to the JXADC header. The XADC core is controlled and accessed from a user design via the Dynamic Reconfiguration Port (DRP). The DRP also provides access to voltage monitors that are present on each of the FPGA's power rails, and a temperature sensor that is internal to the FPGA.

III. Conclusion

In conclusion, XADC and AXI GPIO modules were implemented on an Arty board along with the MicroBlaze soft processor. The steps for setting both modules in the Vivado software were described. After the modules were set up and the hardware exported for working with the SDK, the code was written to set up channels, initialize the hardware, take measurements and report values from both the XADC and the AXI GPIO modules.

The project examined the work of the microprocessor in the FPGA in the VHDL language in the Vivado programming environment, this expands the field of activity when development and make VHDL programming more flexible, for example, allowing you to work with floating point numbers. With the help of this project, it is possible to carry out various types of work, which in the future will be used for studying by students.

In consequence of this, a tutorial was made, where it is shown how and at what speed an elementary project can be created and then complicate it using different tools of the software environment. The main part of our project is the implementation of the ADC. The paper presents the main scheme of work and its applications in the applications. The results of measurements of the signal at the output of the Basys 3 board were obtained and presented in the SDK (Software development kit).

The signal is the differential voltage on some components of the circuit and the temperature of the processor, as well as the voltage of the analog signal. Results attached to the app. The main objective of the project is to provide students with high-quality material for learning. With the help of FPGA, you can easily integrate different areas of work, both software, and hardware of the project. From this, we can conclude that time is reduced to separate stages of development. Therefore, this project is successful and ready to use.

References

[1] "MicroBlaze Processor Reference Guide. UG984 (v2016.4) November 30, 2016", *Xilinx.com*, 2016. [Online]. Available: https://www.xilinx.com/support/documentation/sw_manuals/xilinx2016_4/ug984-vivado-microblaze-ref.pdf. [Accessed: 20- Jun- 2019].

[2] "Using the MicroBlaze Processor to Accelerate Cost-Sensitive Embedded System Development. WP469 (v1.0.1) June 6, 2016", *Xilinx.com*, 2016. [Online]. Available: https://www.xilinx.com/support/documentation/white_papers/wp469-microblaze-for-cost-sensitive-apps.pdf. [Accessed: 20- Jun- 2019].

[3] "Vivado Design Suite", *Xilinx.com*, 2019. [Online]. Available: https://www.xilinx.com/products/design-tools/vivado.html. [Accessed: 19- Jun- 2019].

[4] "7 Series FPGAs Data Sheet: Overview. Product Specification. DS180 (v2.6) February 27, 2018", *Xilinx.com*, 2018. [Online]. Available: https://www.xilinx.com/support/documentation/data_sheets/ds180_7Series_Overview.pdf. [Accessed: 19- Jun- 2019].

[5] "Vivado Design Suite Tutorial. Designing IP Subsystems UsingIP Integrator. UG995 (v2016.4) November 30, 2016", *Xilinx.com*, 2016. [Online]. Available: https://www.xilinx.com/support/documentation/sw_manuals/xilinx2016_4/ug995-vivado-ip-subsystems-tutorial.pdf. [Accessed: 20- Jun- 2019].

[6] "Using Xilinx SDK", *Xilinx.com*, 2016. [Online]. Available: https://www.xilinx.com/html_docs/xilinx2016_4/SDK_Doc/index.html. [Accessed: 20- Jun- 2019].

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Features of the Use of Microprocessors in the Systems of Ovojectors in their Adaptation to the Conditions of the Former CIS

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***Abstract*—This electronic document describes the use of microcontrollers in the regulations of automatic sorting of eggs with a live (dead) embryo with further automatic vaccination of live embryos. These installations are produced only in 3 countries and are called Ovojectors.**

Keywords—microcontroller system, light sensor, mechanical extraction, computer control

I. INTRODUCTION

These devices (Ovojectors) are widely used by modern poultry farms. In Russia, they are leased to 5-7 poultry farms Fig.1. However, although they are produced in three to five countries, including in France, the monopoly right belongs to the company Embrex (USA). Renting these installations costs at least $ 220,000. These plants increase productivity by 8-10 times. The introduction of the proposed device will allow [1-5]: to reduce human costs by 8-10 times; to increase lab our productivity by 3-5 times; to reduce the percentage of defective products to the total volume by 1.5-2 times in poultry factories with a throughput of 5,000-50,000 eggs per shift.

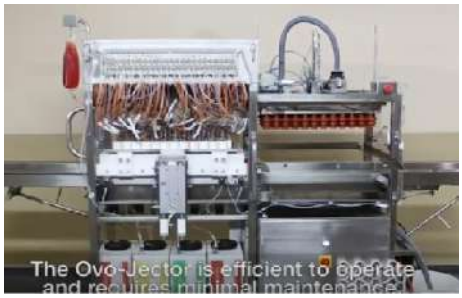

Fig. 1. Ovojector.

In ovo vaccination has been revolutionizing the avian vaccination process worldwide [6]. This is already happening in the hatcheries in Brazil and offers many technical advantages. Built with American technology and using spare parts from global suppliers fig. 2-3: OMRON photoelectricts E3F2-LS10 fig. 3; Innovation in Miniature the Lee Company Fig. 2.

Fig. 2. Miniature the Lee Company.

The ovojectors is Boehringer inteheim's answers to in ovo vaccination. It is backed by globally structured vaccination audits, technical support, and hatchery expertise. The ovojector is efficcent to operate and requires minimal maintenance. The ovojector vaccinater is very easy to operate. The control panel is available for multi-languages. The ovojectors has a touch screen that is capable of performing self-diagnosis.

All commands can easily be performed manually, through maintename screens. Ovojectors: Efficient and simple vaccination process. Using the control panel, the operator can adjust for 3 different egg size during the transfer. Ovojectors: capable of vaccionating 35 thousand eggs per hour; the Ovojectors relies the innovative EggCheck System (Selective vaccination).

This system consist of sensors with identify the absence of eggs in egg trays during injection there by avoiding waste of vaccine.

Fig. 3. Omron-electric, microcontrollers.

II. MAIN PARTS

These installations consist of two parts (carry out two operations): separation of a batch of eggs into parts with "live", "dead" embryos in terms of a conveyor with

automated, appropriate consideration of the number of sorted eggs in real time Fig 2; automatic, precision dosed introduction of a vaccine into selected eggs with live embryos with the corresponding computer accounting in real time.

This report is devoted to the description of the features of the use of microcontroller equipment in tasks that are solved by the first part of installations (Ovojectors) in the CIS market, for example Fig 4 .

Fig. 4. Fragment of installation of Inovoject (automatic removal of eggs with dead embryos).

This section is devoted to the features of the use of microcontroller technology to the tasks of creating the first part of the installation (OVOJECTORS). This installation includes a diagnostic part (sensor block of 30 or 150 pieces), a microcontroller control unit (a multi-output microcontroller with a block of electromagnetic relays for 30 or 150 pieces), a block of mechanical extraction of eggs, which includes installation of pneumatic pick-up of objects of extraction. The latter is a device for moving a gripper block -30 of a vacuum gripper using an air supply unit for 30 chambers connected to an electromagnetic relay controlled by a microcontroller unit. The kind of working finished device is shown in Fig.1. In branded installations, a diagnostic unit with optical sensors working on the through-clearance of eggs in the supplied tray is usually integrated with an extraction device. This certainly speeds up the operation of the device, although it introduces technological difficulties in the production of this product. As it imposes additional conditions on the parameters of the sensors, but it saves money on the absence of the need to create a separate panel on which the sensors are placed and there is no need to position it.

III. Devises for CIS Proposition

When the positioning of the tray with eggs is completed, the microcontroller automatically, in a cycle, starts polling infrared sensors that see through all 30 (150) eggs [4.5]. In the case of a signal level below the threshold value (which corresponds to an egg and a dead embryo), the number of the activated sensor is recorded in the corresponding EEPROM (memory) cell of the microcontroller's memory. At the end of the survey, the signals from the inputs of the microcontroller connected to the electromagnetic relay with optical decoupling include pneumatic devices that extract eggs with a dead embryo.

This happens as follows. Upon completion of recording the result of polling the sensors in the EEPROM memory of the microcontroller, a delay is set, after which the process of polling the EEPROM memory begins. Starting from a known starting address, for example, 00001H, the contents of the cells in the loop are read to the address, for example, 00029H. Each cell is programmed to correspond to a device for pneumatic extraction of eggs with dead embryos. Totally there are 30 or 150 pieces, as well as the number of infrared sensors. With 150 sensors for their control, in addition to the microcontroller, decryption devices are used, since the number of digital outputs of a typical inexpensive microcontroller is limited. When receiving information from the EEPROM memory cell corresponding to the object to be retrieved, the microcontroller through the terminals connected to the actuators through the relay brings the pneumatic gripping device to the corresponding object. This happens until the reading cycle of the EERROM memory cells ends. General view of the working installation is shown in Fig. 4.

This process is also controlled by a computer connected to the microcontroller via standard interfaces (USB, etc.) It is possible to modify the wireless interface to transmit information to a computer using the GSM-sim800 module, as well as Wi-fi, Blootuze modules. Installing a local server will make it possible to monitor the results of sorting eggs with live and dead embryos in On-line mode in the local network of the enterprise. It is also possible to transfer data to the Internet.

Features of the development and use of the installation in the conditions of the CIS and Ukraine. Despite the economic feasibility from the point of view of increasing labour productivity in poultry enterprises, the production of a full complex (Ovojectors) is not always appropriate. The reason for this is the high cost of maintenance, as well as the inevitable dependence on imported components.

IV. Conclusions

Work on the development of devices for the automation of processes for the removal of eggs with dead embryos and in ovo vaccination abroad are closed and publications do not exist. Thus, Embrex (USA) is offering a vaccination system for rent in more than 30 countries in Europe, Latin and North America, Australia, and Asia. Embrex does not sell machines and licenses for its production. Based on the experimental and design work carried out in Ukraine, it is quite possible to create industrial devices for the automatic removal of eggs from inert living embryos and to further in ovo vaccinate live embryos, which will be completed domestic poultry enterprises. In the world, there is an analogue, which was created by Embrex (USA), which only leases its products for 220 thousand dollars a year for one device. Domestic automatic devices for the removal of inanimate embryos and subsequent injecting of living will be cheaper by 3-4 times for US denials. It is most expedient in domestic to produce plants separating eggs with living and dead embryos separately from the ovo vaccination block.

References

[1] V. Breslavets and A. Stegniy, "On the Question to Development of Automatic Methods of Biocontrol in the Incubation", *Veterinarna medicina*, vol. 99, pp. 186-189, 2014.

[2] V. Rolnik, *Biology of embryonic development of birds*. Leningrad: Science, 1968, p. 425.

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Trends in Training Modern Technicians

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***Abstract*—The paper considered procedural aspects affecting the quality of modern technicians training as well as practical examples of the implementation of procedures that affect it.**

Keywords—technical training, cooperation, employers, VHDL, FPGA, MATLAB

I. Introduction

In the modern world, the university seeks to keep up with the times, to follow the trends of scientific and technological progress. Therefore, much attention is paid to the quality of technical specialists graduated from higher educational institutions. The current situation in the labor market also dictates its own conditions and requirements for the quality of technical graduated specialists.

More and more engineers are working at the hardware and software level. Therefore, more in demand are specialists who are fluent in hardware and software. Therefore, technical institutions of higher education need to constantly monitor progressive methods of designing and developing electronic devices and use modern equipment and software in the educational process.

II. Procedural Aspects Affecting the Quality of Training

The content of education is dictated by business. Since, they are potential employers. The quality of education depends on the level of cooperation of the university with commercial enterprises.

To improve the quality of technical training, it is useful, starting from junior courses for students, to organize informational meetings with representatives of enterprises, to hold training seminars, trainings, etc. There, students will learn more about the chosen specialty, the requirements of employers, possible areas of study and future professional activities.

One of the ways to improve the quality of technical training is to create specialized laboratories at universities that are equipped with modern equipment. Cooperation with leading specialized enterprises greatly simplifies this process.

Commercial enterprises and companies together with universities create specialized modern laboratories that are equipped in accordance with the requirements of the labor market. Then the company and the university agree on the areas of study, curriculum, structure of practical and laboratory classes. Next, together with the curator of the company and the university teacher develops teaching materials. If the university has ready teaching materials, they are adapted to the requirements put forward by the employer. The cycles of laboratory and practical work should be logically grouped, have a practical orientation, and correspond to the conditions of a modern employer.

The type of hardware platform is dictated by the employer, as it comes with a complete set of training laboratories. On the plus side, in the modern world, the hardware platforms in the bundle have free software environments for developing and designing devices. It provides universities with licensed software.

Improving the quality of technical training is ensured by coordinating with the employer topics of coursework and certification work. For the acquisition of practical skills - students are directed to the Company or to specialized laboratories to carry out the course and certification works.

Important is the organization of production practices in enterprises. That allows students to get practical experience that will ensure their effective work in the future and a decent salary.

The level of practical training of the teaching staff is important. The teacher must comply with current trends, learn the latest equipment, master new software. This is ensured by regular advanced training through internships at leading enterprises in the country and in foreign universities. In this way, the university receives a certified specialist teacher.

III. Practical Examples of Procedures Implementation

To improve the quality of technical specialists, a new fundamental technical department of microprocessor technologies and systems (MTS) was created at the Kharkov National University of Radio Electronics.

The Department of MTS carries out educational, methodological, organizational and scientific activities in the field of microprocessor technologies and systems. Teachers of the department for students of technical specialties of

bachelor level in the cycle of general and specialized vocational training teach the normative discipline “Designing devices on microcontrollers and programmable logic integrated circuits (FPGAs)” with a volume of 10 credits ECTS with such modules:

- “Simulation of digital signals using MATLAB and VHDL” (2 ECTS credits);
- “Microcontrollers” (4 ECTS credits);
- FPGA (4 ECTS credits).

Given the experience of European partner universities, the focus is on practical training. Therefore, for laboratory work allocated 75% of the total classroom hours.

The department develops the following research areas: designing devices on microcontrollers and programmable logic integrated circuits; digital signal modeling.

For classes at the department, a specialized training laboratory “Designing devices on microcontrollers and FPGAs” was created. The laboratory is equipped with modern hardware and software equipment: personal computers, sets of STM32 DISCOVERY, FPGAs from Xilinx Artix 7, measuring equipment (Fig. 1). As part of the existing university program of Xilinx (Xilinx University Program, XUP), the Vivado Design Suite software and methodological materials on its use were received for the department. The provided software is used to teach students in laboratory work and in scientific research.

Fig. 1. Laboratory boards.

Regular, staff of the Department of MTS in cooperation with the university administration, the Department of International Cooperation and leading enterprises held informational meetings for students of second and third year students and teachers. It discusses issues of professional competence, requirements of employers for an employee, training courses of companies, opportunities for participation in joint projects, mobile international programs, conditions for advanced training abroad, participation in Erasmus +, Horizon 2020, and others.

IV. Conclusion

Improving the quality of technical training of specialists is an urgent task not only in Ukraine, but also in the world. This is possible with the close cooperation of universities with leading companies - potential employers.

References

[1] V. Semenets, I. Svyd and L. Saikivska, "Methods of improving the quality of preparation of technical specialists", in *Engineering education: challendes and developments : materials of the IX International Scientific and Methodological Conference*, Minsk, Belarus, 2018, pp. 415-416.

[2] P. Sauh, *Innovation in higher education: problems, experience, perspectives: monograph*. Edited by Sauh P. Zhytomyr: ZHDU them. I. Franco, 2011, p. 444.

[3] V. Semenets, "Technical aspects for development laboratory base for learning FPGA and microcontroller systems.", in *10th International Conference The Experience of Designing and Application of CAD Systems in Microelectronics*, Lviv-Polyana, Ukraine, 2009, p. 145.

[4] O. Avrunin, S. Sakalo and V. Semenetc, "Development of up-to-date laboratory base for microprocessor systems investigation", in *19th International Crimean Conference Microwave and Telecommunication Technology CriMiCo - 2009*, Sevastopol, Ukraine, 2019, pp. 301-302.

[5] I. Tarasov. Organization of the educational process in the design of digital devices using an initial level based boards FPGA Spartan-6 company Xilinx. *Components and Technologies*, 2011,12, pp.10-14.

[6] V. Semenets, V. Kauk, O. Avrunin. "The advanced technology of remote training at the initial process" ["Vprovadjennya tehnologiy dystantsiynogo navchannya u navchalnii protses"], High School, 2009. – No. 5 .– P. 40– 45.

[7] S. Sakalo, V. Semenets and O. Azarhov, *High frequencies in medicine (therapy and diagnostics): Teaching manual*. Kharkov: KNURE; Collegium, 2005, p. 264.

[8] Semenets V.V. *Technology of interconnection of electronic equipment: a university textbook* / V.V. Semenets, John Kratz, I.Sh. Nevlyudov, V.A. Palagin. - X.: ed. SMIT, 2005 - 432 p.

[9] Svyd I.V., Litvinenko O.V., Bilotserkivets O.G. Features of designing digital devices based on Xilinx FPGA in CAD Vivado HLx Design Suite. // *Specialized Exhibition «KharkivProm Days. Production and efficiency ". Collection of materials of the forum section "Automation, electronics and robotics. Development Strategies and Innovative Technologies ».* - Kharkiv, KNURE, Exhibition Company ADT, 2019. - P. 43-44.

[10] V. Semenets, V. Levikin and V. Sayenko, "Research and analysis of the didactic policy of the university in the training of specialists in information technology", *Automated control systems and devices*, vol. 175, pp. 4-14, 2018.

[11] O. Avrunin, O. Kruk, T. Nosova and V. Semenets, "Technical aspects of the development of virtual laboratory works on technical educational disciplines", *Open Education*, vol. 3, pp. 11-17, 2008.

[12] V. Kobzev, V. Semenets and V. Filatov, "Components of the information system for monitoring the quality of education in Kharkov National University of Radio Electronics", in *7th Int. scientific and technical conf. Information systems and technologies (IST-2018)*, Kharkiv-Koblevo, 2018, pp. 51-54.

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A VHDL Implemetation of the Advanced Encryption Standard

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***Abstract*—A new original approach to realization of AES algorithm on FPGA is proposed. Problems of VHDL modeling of AES ciphering and deciphering are considered.**

Keywords—AES, triple DES, encryption, decryption, FPGA, VHDL

I. INTRODUCTION

Modern cryptography is the cornerstone of computer and communications security. Its foundation is based on various concepts of mathematics such as number theory, computational-complexity theory, and probability theory.

It came out on top among several competitors and was officially announced in 2001 by the new AES encryption standard. The algorithm is based on several substitutions, permutations and linear transformations, each of which is performed on data blocks of 16 bytes, hence it takes its term “blockcipher”. These operations are repeated several times, called "rounds." During each round, a unique round key is calculated from the encryption key and is included in the calculation. Based on the AES block structure, modifying a single bit, either in the key or in the plaintext block, results in a completely different block of ciphertext - a clear advantage over traditional stream cipher methods. Finally, the difference between AES-128, AES-192, and AES-256 is the key length: 128, 192, or 256 bits — all radical improvements over the 56-bit DES key. And cracking a 128-bit AES key using a modern supercomputer will take longer than the estimated age of the universe. [1]

II. AES STANDARD

The more popular and widely adopted symmetric encryption algorithm likely to be encountered nowadays is the Advanced Encryption Standard (AES). It is found at least six time faster than triple DES. [1]

A replacement for DES was needed as its key size was too small. With increasing computing power, it was considered vulnerable against exhaustive key search attack. Triple DES was designed to overcome this drawback but it was found slow.[1,2]

The features of AES are as follows:

- symmetric key and symmetric block cipher;
- 128-bit data, 128/192/256-bit keys;
- stronger and faster than Triple-DES;
- provide full specification and design details;
- software implementable in C and Java.

The Advanced Encryption Standard can be programmed in software or built with pure hardware. However Field Programmable Gate Arrays (FPGAs) offer a quicker, more customizable solution. This research investigates the AES algorithm with regard to FPGA and the Very High Speed Integrated Circuit Hardware Description language (VHDL). Altera Max+plus II software is used for simulation and optimization of the synthesizable VHDL code. All the transformations of both Encryptions and Decryption are simulated using an iterative design approach in order to minimize the hardware consumption. Altera ACEX1K Family devices are utilized for hardware evaluation.

III. THE ALGORITHM

A. Encryption

The AES algorithm represents a data block in the form of a two-dimensional byte array of 4x4. All operations are performed on individual bytes of the array, as well as on independent columns and rows. In each round of the algorithm, the following transformations are performed:

1. SubBytes operation, which is a tabular replacement of each byte of the data array

2. The ShiftRows operation, which performs a cyclic left shift of all rows of the data array, with the exception of zero. Shift i-th row of the array (for i = 1,2,3) is performed on i byte.

3. MixColumns operation. Performs multiplication of each data array column by a fixed polynomial a(x):

$$a(x) = 3x^3 + x^2 + x + 2.$$

Multiplication is performed by modulo $x^4 + 1$

4. The AddRoundKey operation imposes a key material on the data array. Namely, on i -th column of the data array (i = 0 ... 3), a bit-by-bit logical exclusive or XOR operation,

superimposes a specific extended key word W_{4r+i}, where r is the number of the current round of the algorithm, starting with 1. Before the first round of the algorithm, a preliminary key material is superimposed using the AddRoundKey operation, which overlays the clear four words of the extended key W_0 ... W_3 on the plaintext.

The last round is different from the previous ones in that it does not perform the operation MixColumns.

B. Decryption

Decryption is performed using reverse operations in reverse order. Accordingly, before the first round of decryption, an AddRoundKey operation (which is the reverse of itself) is performed, performing overlay on the ciphertext of the last four words of the extended key, i.e. W_{4r} ... W_{4r+3}. Then r decryption rounds, each of which performs the following transformations:

1. The InvShiftRows operation performs a cyclic right shift of the last three rows of the data array by the same number of bytes that the ShiftRows operation was shifted during encryption.

2. The InvSubBytes operation performs a table-by-byte reverse tabular replacement.

3. The AddRoundKey operation, as well as when encrypting, imposes four words of the extended key W_{4r} ... W_{4r+3} on the processed data. However, the numbering of rounds r when decrypting is performed in the opposite direction - from $r-1$ to 0.

4. The InvMixColumns operation multiplies each column of the data array in the same way as the direct MixColumns operation, however, the multiplication is performed by the polynomial $a^{-1}(x)$, defined as follows:

$$a^{-1}(x) = Bx^3 + Dx^2 + 9x + E.$$

Similar to encryption, the last decryption round does not include the InvMixColumns operation.

C. Key extension

AES uses encryption keys of three fixed sizes: 128, 192, and 256 bits. Depending on the key size, a specific variant of the AES algorithm may be referred to as AES-128, AES-192 and AES-256, respectively.

The task of the key expansion procedure is to form the necessary number of words of the extended key for their use in the AddRoundKey operation. As mentioned above, the "word" here means a 4-byte fragment of the extended key, one of which is used in the primary imposition of the key material and one by one in each round of the algorithm. Thus, in the process of key expansion, $4 * (r + 1)$ is formed of words.

Key expansion is performed in two stages, the first of which is the initialization of the words of the extended key (denoted as W_i): the first N_k (N_k is the size of the original encryption key K in words, that is, 4, 6 or 8) words W_i (t. e. i = 0 ... N_{k-1}) are formed by their successive filling with key bytes.

The following figure 1 represents complete hardware implementation of the both encryption and decryption with key generation modules.

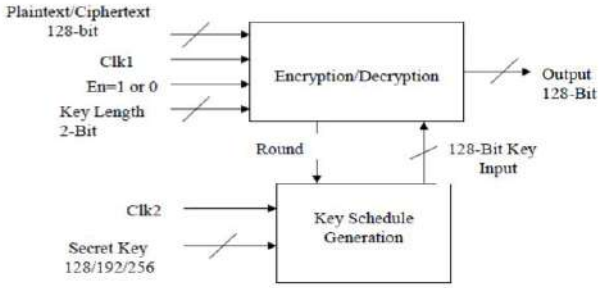

Fig. 1. Block Diagram of AES Hardware Implementation.

Key Schedule Generation block can generate the required keys for the process with secret key and Clk2 as inputs; these generated keys are stored in internal ROM and read by Encryption/Decryption block for each round to obtain a distinct 128-bit key with Round counter, where Encryption/Decryption module takes 128-bit plaintext or ciphertext as input with respective to the Clk1 (If En=1 or 0 process is encryption or decryption respectively). In order to distinguish the number of rounds, a 2-bit Key Length input is given to this module where 00, 01, 10 represents 10(128-bit key), 12(192- bit key), 14(256-bit key) rounds respectively, generates the final output of 128-bit cipher or plaintext.

IV. CONCLUSION

Optimized and Synthesizable VHDL code is developed for the implementation of both encryption and decryption process. Each program is tested with some of the sample vectors provided by NIST and output results are perfect with minimal delay. Therefore, AES can indeed be implemented with reasonable efficiency on an FPGA, with the encryption and decryption taking an average of 320 and 340 ns respectively (for every 128 bits). The time varies from chip to chip and the calculated delay time can only be regarded as approximate. Adding data pipelines and some parallel combinational logic in the key scheduler and round calculator can further optimize this design.

REFERENCES

[1] Tilborg, Henk C. A. van. "Fundamentals of Cryptology: A Professional Reference and Interactive Tutorial", New York Kluwer Academic Publishers, 2002.

[2] Peter J. Ashenden, "The Designer's Guide to VHDL", 2nd Edition, San Francisco, CA, Morgan Kaufmann, 2002.

[3] Joan Daemen and Vincent Rijmen, The Design of Rijndael, AES - The Advanced Encryption Standard, Springer-Verlag 2002 (238 pp.).

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Approaches Half Band Filter Realization for Means FPGA

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***Abstract*—Approaches to half band filter realization are considered. Ways of implementation are discussed. Possibilities for obtaining FIR or IIR realizations are mentioned.**

Keywords—FPGA, half band filter, digital signal processing, analytical signal

I. INTRODUCTION

When solving problems of synthesis and analysis of systems of different purposes, imitative modeling plays an increasingly important role. The current level of development of hardware and software allows you to perform modeling work at different levels of equipment - from the idea of the system, expressed in mathematical form to its implementation. In itself, the simulation in this case is not the ultimate goal of this work, but is an instrument in the course of designing and allows us to conveniently evaluate the quality of the system from different points of view [1].

The object of the study is a half-band filter, which is being developed in digital form. Such a filter is extremely useful for the developer, since it is the basic element for performing many operations on a signal – frequency transfer, modulation, demodulation, to name a few. It is also convenient because it allows you to perform quality control work both in frequency and time characteristics, as well as in key parameters that are relevant to the researcher's current task, such as the number of valves, the value of the delay, etc.

Since the filter is digital, using the Matlab and Simulink software, you can perform simulations, from the task of filter parameters to its implementation, which is very convenient, cheap and really consumes a minimum of time.

Matlab allows you to get the filter structure of the given kind, its coefficients taking into account or without rounding off, as well as in a convenient form to present a complete set of filter characteristics in the shortest possible time and qualitatively [2]. Unfortunately, for an analog filter the task is more difficult to solve.

But to implement the filter in the FPGA, you need a convenient transition to the chosen environment of the description of digital equipment - VHDL, Verilog, System Verilog. Thus, the design is already in the specialized program (Quartus II or Vivado) and is close to the apparatus synthesis [3,4]. This transition allows Matlab to be executed in semi-automatic mode. This adds flexibility to the design process and allows you to reduce the cost of design.

A bit of technical characteristics. Bit length - no less than 16 bits. What element base was available for research?

1. Spartan 6. 45 nm. The limit on the digit is rather vague. On the crystal, high-speed hardware multipliers 18x18 bits and a 48-bit battery are implemented, which significantly but not completely limits the bit. In principle, you can increase the digit. The charge on the crystal, of course, increases, but can be used for educational purposes.

2. Artix 7. Compared to it, Spartan looks simple. In addition to offering Xilinx on the Spartan 6 example for the initial level of familiarity with the capabilities of modern FPGAs, it is possible to master the interfaces that are widely used at present. Actually, for work with interfaces Artix 6 and optimized. These include interfaces such as PCI Express Base Spec 2.1 Gen1 (2.5 Gb / s) and Gen2 (5 Gb / s). Maximum speed up to 6.25 Gb / s. It is possible to convert the serial code into parallel words in the length of 16, 20, 32, or 40 bits in the receiver and perform a reverse operation by the transmitter.

II. CALCULATION OF THE COEFFICIENTS

Half-band filters are lowpass FIR filters with cut-off frequency of one-quarter of sampling frequency f_s and odd symmetry about $f_s/4$ [5]. And it so happens that almost half of the coefficients are zero. The passband and stopband bandwiths are equal, making these filters useful for decimation-by-2 and interpolation-by-2. Since the zero coefficients make them computationally efficient, these filters are ubiquitous in DSP systems.

Here we will compute half-band coefficients using the window method. While the window method typically does not yield the fewest taps for a given performance, it is useful for learning about half-band filters. Efficient equiripple half-band filters can be designed using the Matlab function firhalfband [5].

III. COEFFICIENTS BY THE WINDOW METHOD

The impulse response of an ideal lowpass filter with cut-off frequency $\omega_c = 2\pi f_c/f_s$ is [5]:

$$h(n)=\sin(\omega_c n)/\pi n, -\infty<n<\infty.$$

This is the familiar sinx/x or sinc function (scaled by ω_c/π). To create a filter using the window method, we truncate h(n) to N+1 samples and then apply a window. For a halfband filter, $\omega_c = 2\pi*1/4 = \pi/2$. So the truncated version of h(n) is:

$$h(n)=\sin(n\pi/2)/n\pi,-N/2<n<N/2.$$

Now apply a window function w(n) of length N+1 to obtain the filter coefficients b:

$$b(n)=h(n)w(n),-N/2<n<N/2,$$

$$b(n)=\sin(n\pi/2)/(n\pi) * w(n),-N/2<n<N/2. \quad (1)$$

Choice of a particular window function w(n) is based on a compromise between transition bandwidth and stopband attenuation. As a simple example, the Hamming window function of length N+1 is:

$$w(n)=0.54+0.46\cos(2\pi nN),-N/2<n<N/2$$

And this way you can obtain the coefficients. Note that N is even and the filter length is N+1 (odd length).

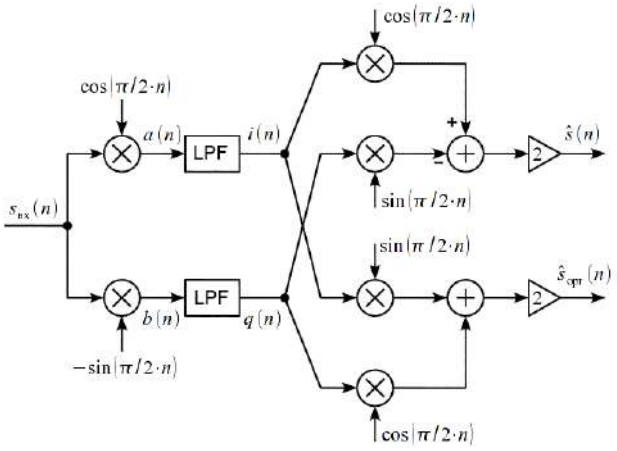

Fig. 1. Analytical signal shaper based on quadrature converter.

IV. Brief Results of Work

The half band filter is supposed to implement for analytical signal forming. The main task in the formation of the analytical signal is the suppression of the spectral components in the negative frequency range falls on the half-band low-pass filter. One can use either FIR or IIR filters. When using IIR filters, one can save computational resources, and calculate the filter based on the required frequency response corridor. However, the use of a physically realized low-pass filter will lead to signal distortion in the low and high frequencies

Real low-pass filter has non-uniformity in the passband (in the positive frequency range), possesses finite suppression in the negative-frequency range, and some transition band, with the result that the signal in the low and high frequencies is distorted. But for practical use of such a shaper for SSB modulation during voice transmission, distortions in the low and high frequency areas do not play a significant role, while the use of, for example, elliptical IIR filters allows you to adjust the level of sideband suppression and uneven frequency response.

Thus, all multiplications can be replaced by re-indexing the samples and changing their sign. This structure requires only multiplication for filtering, which makes it attractive both for software implementation and for hardware based on FPGA.

The concepts of a bandpass signal and a complex radio signal envelope are used, and the concept of a vector representation of a complex envelope makes possible to realize modulation and demodulation under general schemes. The complex envelope can be represented by the in-phase and quadrature components and the modulation can be performed by a quadrature modulator. In order to specify the modulation method, it is necessary to choose the method of forming the complex signal envelope by changing the amplitude and phase.

The project in Matlab is a half band filter of the 32nd and 128th order. When switching to Vivado, we have the opportunity to quickly obtain a filter structure and the ability to explore the characteristics of the digital system. Considering such a simple example, we demonstrate the possibilities of interacting with different products. The power of crystals is enough to implement even an optimized algorithm: about 1100 instances and 320 nodes (DFlops) require an algorithm where the weakest version of Spartan has 3840 elements (Logic Cells), as well as Artix 7. More detailed results are given in the work.

References

[1] Moiseev N.N. Mathematical problems of system analysis: [Proc. manual for universities on spec. “Apply Mathematics ”] / N. N. Moiseev. - M .: Science, 1981. - 487 p.

[2] Digital signal processing and MATLAB: proc. manual / A.I. Solonina, D.M. Klionsky, T.V. Merkucheva, S.N. Perov. - SPb .: BHV-Petersburg, 2013. - 512 pp., Ill .— (Educational literature for universities)

[3] Semenets V. V. Designing digital systems using the VHDL language: studies. manual / V.V. Semenets, I.V. Khakhanova, V.I. Khakhanov; MES of Ukraine, KNURE. - Kharkov: KNURE, 2003. - 492 p.

[4] Semenets V. Century Technology of interconnection of electronic equipment: studies. for universities / V. V. Semenets, John Kratz, I. Sh. Nevludov, V. A. Palagin. — H.: ed. SMITH, 2005. — 432 p. [Semenets V. V., Kratts J., Nevlyudov I. Sh., Palagin V. A].

[5] Neil Robertson. Simplest Calculation of Half-band Filter Coefficients. https://www.dsprelated.com/blogs.php

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