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Realisation of Iterative Algorithm of Six-Port Reflectometer on FPGA Using Logarithm Function

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***Abstract*—The six-port reflectometer is an universal measurement device of microwave range for signal power and tract termination reflection coefficient definition. The definition of such tract and termination parameters is made by sensor signal processing. As processing algorithm can be used least squares estimation. The advantages of least squares estimation is accuracy. The condition of its use is redundandant sensor number. The least squares estimation feature is invers matrix computation. As to FPGA realisation of algorithm there are problems connected to matrix inversion. So the report is devoted to attempt to simplify six-port reflectometer sensor signal processing and to avoid inverse matrix computation.**

Keywords—six-port reflectometer, processing algorithm, least squares estimation, logarithm

I. INTRODUCTION

The six-port reflectometer [1, 4, 5] consists of waveguide section and processing and indication block. The processing and indication block can be realized on FPGA.

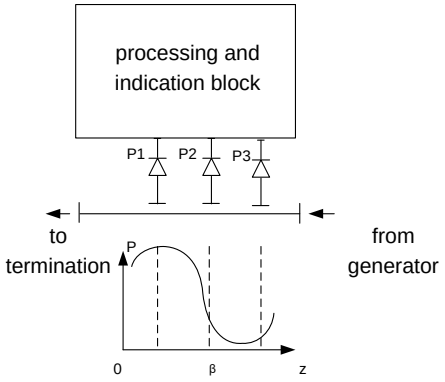

Fig. 1. The six-port reflectometer with three sensors.

The waveguide section located between generator and termination. Due to electromagnetic wave reflection from termination inside waveguide section is standing wave. There are sensors along standing wave in the waveguide. The sensors signals proportional to intensity of electromagnetic wave in their position. To extract information about signal power and reflection coefficient modulus ana phase it is necessary process sensor signals by definite algorithm. As mathematical model of ideal six-port reflectometer is system of linear equation, where each equation corresponds to one sensor, to get algorithm is necessary to solve the system of linear equation through inverse matrix, unlike non ideal sensor processing. Processing of non ideal sensors demand more complicated algorithm, for example, least squares estimation.

The problem of this research is contradiction between accounting an uncertainity of measurement by mean of complication processing methods and realization of computation methods on FPGA, using hardware description language VHDL, where computation mathematics should be implemented by hardware units.

II. ITERATIVE ALGORITHM OF SIX-PORT REFLECTOMETER

Lets sensor number exceed unknown intermediate variable number. As mathematical model we have redundant system of linear equation [1]. The solution of such system through the least squares estimation is

$$[b] = \left([A]^T [A] \right)^{-1} [P]. \qquad (1)$$

To avoide inverse matrix calculation lets apply iterative Seidel algorithm

$$\begin{aligned} b_0 &= \frac{1}{f_{11}} \{ a_{11} p_1 + a_{21} p_2 + a_{31} p_3 + a_{41} p_4 - (f_{12} b_1 + f_{13} b_2) \} \\ b_1 &= \frac{1}{f_{22}} \{ a_{12} p_1 + a_{22} p_2 + a_{32} p_3 + a_{42} p_4 - (f_{21} b_0 + f_{23} b_2) \} \\ b_2 &= \frac{1}{f_{33}} \{ a_{13} p_1 + a_{23} p_2 + a_{33} p_3 + a_{43} p_4 - (f_{13} b_0 + f_{32} b_1) \} \end{aligned} \qquad (2)$$

where system matrix is

$$[A]=\begin{pmatrix} 1 & \cos\phi & \sin\phi \\ 1 & 1 & 0 \\ 1 & \cos\phi & -\sin\phi \\ \dots & \dots & \dots \\ 1 & \cos n\phi & -\sin n\phi \end{pmatrix}, \quad (3)$$

matrix column of sensor signals is

$$[P]=(P_1\ P_2 \dots P_n)^T. \quad (4)$$

Intermediate variable is

$$[b]=(b_1 b_2 \dots b_n)^T. \quad (5)$$

Definition for intermediate variables is

$$\begin{aligned} b_0 &= P_{inc}(1+\Gamma^2), \\ b_1 &= \Gamma P_{inc}\cos\phi, \\ b_2 &= \Gamma P_{inc}\sin\phi, \end{aligned} \quad (6)$$

where Γ is reflection coefficient modulus, φ is reflection coefficient phase, θ is phase distance between neighbouring sensors, P_{inc} is incident power. For expression (2) also necessary expression. They are calculated from information Fisher matrix

$$\begin{aligned} f_{11} &= a_{11}^2 + a_{21}^2 + a_{31}^2 + a_{41}^2 \\ f_{12} &= a_{11}a_{12} + a_{21}a_{22} + a_{31}a_{32} + a_{41}a_{42} \\ f_{13} &= a_{11}a_{13} + a_{21}a_{23} + a_{31}a_{33} + a_{41}a_{43} \\ f_{21} &= a_{11}a_{12} + a_{21}a_{22} + a_{31}a_{32} + a_{41}a_{42} \\ f_{22} &= a_{12}^2 + a_{22}^2 + a_{32}^2 + a_{42}^2 \\ f_{23} &= a_{12}a_{13} + a_{22}a_{23} + a_{32}a_{33} + a_{42}a_{43} \\ f_{31} &= a_{11}a_{13} + a_{21}a_{23} + a_{31}a_{33} + a_{41}a_{43} \\ f_{32} &= a_{12}a_{13} + a_{22}a_{23} + a_{32}a_{33} + a_{42}a_{43} \\ f_{33} &= a_{13}^2 + a_{23}^2 + a_{33}^2 + a_{43}^2 \end{aligned}$$

Analysis of expression shows that on VHDL should be realised summation, multiplication and exponentiation.

III. HARDWARE IMPLEMENTATION

In the paper [2],an FPGA-based single precision floating point hybrid iterative architecture for solving a linear system of equations is proposed. The whole design has been implemented in Verilog HDL, having Virtex 7 XCV2000T as targeted device. The design optimizations include using modified high-speed radix 4 multiplier and optimized high-speed 2's complementer. The Radix-4 Booth Encoded multiplier is the most speed efficient and area efficient among other higher radix Booth Encoded multipliers. The partial products required for computation are significantly reduced compared to the traditional multipliers. These partial products are added using a Dadda tree structure and the final summation is carried out using a Koggestone adder.

This approach has many advantage and it is verified, but we propose an idea of alternative solution. The idea is borrow from operational amplifier. The idea is instead of calculation of product there is made calcultion of sum of multipicant logarithm.

The logariphm calculation is performed by such methods as: 1) recursive algorithm for calculating the logarithm; 2) the comparison method to 2; 3) discrete logarithm; 4) logariphm ruler, 5) lookup table. The elements of this approach are contained in [3].

The second method, comparison to 2 method algorithm is: 1. The number is compared to 2; 2. If greater than 2: then divide it by 2 and go to 1 step; 3. if less than 2, but more than 1: then remember the number of divisions by 2 (this there will be an integer part of the logarithm); 4. output the result. Advantages: 1) Possibility of implementation on logic elements; 2) Speed of calculations. Disadvantages:1) Calculates only an integer, without a remainder.

IV. CONCLUSION

There was proposed new iterative method of six-port reflectometer sensor signal processing. It is based on least squares estimation iterative calculation by Seidel method for example. It allows to avoid inverse matrix calculation and leaves only calculation of sum and product. There was worked out procedura for computation.

Implementation of such algorithm on FPGA is considered from hardware point of view. The inherited from operational amplifiers logarithmic transformation, i.e. instead of calculation of product there is made calcultion of sum of multipicant logarithm lays in its foundation.

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