

II International Scientific and Practical Conference

Theoretical and Applied Aspects of Device Development on Microcontrollers and FPGAs

MC&FPGA-2020

Conference Proceedings

Kharkiv, Ukraine June 25-26, 2020 II International Scientific and Practical Conference «Theoretical and Applied Aspects of Device Development on Microcontrollers and FPGAs» MC&FPGA-2020, Kharkiv, Ukraine, June 25-26, 2020. – Kharkiv, NURE. – 60 pp.

There proceedings depict: mathematical modeling of information signals and systems; hardware description languages; systems of computer aided design of devices on microcontrollers, microprocessors and FPGAs; features of device development on microcontrollers and microprocessors; aspects of the development of devices in the FPGA; architecture and microprocessor technology; the problem of improving the quality of training specialists.

Papers are presented in authors' edition.

Edition prepared of the Department of Microprocessor Technologies and Systems Faculty of Information Radio Technology and Technical Information Protection of the Kharkov National University of Radio Electronics with the support of the State Scientific Institution "Institute of Education Content Modernization" of the Ministry of Education and Science of Ukraine.

Head of the Department of Microprocessor Technologies and Systems Phone: +38 (050) 4061-220 E-mail: mcfpga@nure.ua , iryna.svyd@nure.ua Conference on Web: mcfpga.nure.ua

Committees

Valerii Semenets	Chair of the program committee, chair of the organizing committee, doctor of technical sciences, professor, rector of KhNURE (Kharkiv, Ukraine).
Igor Ruban	Vice Chair of the Program Committee, Member of the Organizing Committee, Doctor of Technical Sciences, Professor, First Vice-Rector of Kharkiv National University of Radio Electronics (Kharkiv, Ukraine).
Murad Anver oglu Omarov	Vice Chair of the Program Committee, Member of the Organizing Committee, Doctor of Technical Sciences, Professor, Vice-Rector on International Cooperation of Kharkiv National University of Radio Electronics (Kharkiv, Ukraine).
Iryna Svyd	Vice Chair of the Program Committee, Member of the Organizing Committee, Candidate of Technical Sciences, Associate Professor, Head of Department of Microprocessor Technologies and Systems of Kharkiv National University of Radio Electronics (Kharkiv, Ukraine).
Paweł Komada	Member of the Program Committee, Ph.D. Eng. assistant professor, Deputy Director of the Institute for General Affairs Lublin University of Technology, Institute of Electronics and Information Technology, (Lublin, Poland).
Nikolai Listopad	Member of the Program Committee, doctor of technical sciences, professor, Head of Department of Information Radio Technologies Belarusian State University of Informatics and Radioelectronics (Minsk, Republic of Belarus).
Vahid Meghdadi	Member of the Program Committee, professor, professor the University of Limoges (Limog, France).
Serhat Şeker	Member of the Program Committee, Prof. Dr., Dean of Faculty of Elecrical – Electronis Engineering the Istanbul Technical University (Istanbul, Turkey).
Sergey Sakalo	Vice Chair of the Organizing Committee, Member of the Program Committee, Candidate of Technical Sciences, Associate professor, Senior Researcher, Dean of Faculty of Information Radio Technologies and Technical Information Security of Kharkiv National University of Radio Electronics (Kharkiv, Ukraine).
Aleksandr Korotkevich	Member of the Organizing Committee, Candidate of Technical Sciences, Associate Professor, Dean of Faculty Radio Engineering and Electronics Belarusian State University of Informatics and Radioelectronics (Minsk, Republic of Belarus).
Vladimir Kartashov	Member of the Program Committee, Member of the Organizing Committee, doctor of technical sciences, professor, Head of Department of the Media Engineering and Information Radio Electronic Systems of Kharkiv National University of Radio Electronics (Kharkiv, Ukraine).
Ivan Antipov	Member of the Program Committee, Member of the Organizing Committee, doctor of technical sciences, professor, Head of Department of Computer Radio Engineering and Technical Information Security Systems of Kharkiv National University of Radio Electronics (Kharkiv, Ukraine).
Olena Voloshchuk	Member of the Organizing Committee, Ph.D, Assistant Rector of Kharkiv National University of Radio Electronics (Kharkiv, Ukraine).
Tetiana Tkachova	Member of the Organizing Committee, Candidate of Technical Sciences, Associate Professor, Chief of Department of International Relations of Kharkiv National University of Radio Electronics (Kharkiv, Ukraine)

Volodymyr Kobziev	Member of the Program Committee, Member of the Organizing Committee, Candidate of Technical Sciences, Senior Researcher, Associate Professor of the Department of Applied Mathematics of Kharkiv National University of Radio Electronics (Kharkiv, Ukraine).
Oleg Sharpan	Member of the Program Committee, Doctor of Technical Sciences, Professor, Professor of the Department of Theoretical Foundations of Radio Engineering at the National Technical University of Ukraine "Igor Sikorsky Kyiv Polytechnic Institute (Kyiv, Ukraine).
Ganna Zavolodko	Member of the Program Committee, Candidate of Technical Sciences, Associate Professor of the Department "Information" of National Technical University "Kharkiv Polytechnic Institute" (Kharkiv, Ukraine).
Ivan Obod	Member of the Program Committee, Member of the Organizing Committee, Doctor of Technical Sciences, Professor, Professor of Department of Microprocessor Technologies and Systems of Kharkiv National University of Radio Electronics (Kharkiv, Ukraine).
Oleksandr Vorgul	Member of the Program Committee, Member of the Organizing Committee, Ph. D. of Technical Sciences, Assosiate Professor, Assosiate Professor of Department of Microprocessor Technologies and Systems of Kharkiv National University of Radio Electronics (Kharkiv, Ukraine)
Oleg Zubkov	Member of the Program Committee, Member of the Organizing Committee, Ph.D., Associate Professor, Assosiate Professor of Department of Microprocessor Technologies and Systems of Kharkiv National University of Radio Electronics (Kharkiv, Ukraine)
Liliia Saikivska	Member of the Program Committee, Member of the Organizing Committee, Candidate of Technical Sciences, Assosiate Professor, Assosiate Professor of Department of Microprocessor Technologies and Systems of Kharkiv National University of Radio Electronics (Kharkiv, Ukraine)
Pavlo Galkin	Member of the Program Committee, Senior Lecturer of Design and Operation of Electronic Devices Department of Kharkiv National University of Radio Electronics (Kharkiv, Ukraine)

Table of Contents

No.	Paper Title	Page No.
1.	Features of the use of PID controllers when controlling evaporators	6
2	Oleg Zubkov, Iryna Svyd, Oleksandr Maltsev	0
2.	Realisation of Iterative Algorithm of Six-Port Reflectometer on FPGA Using Logarithm Function	8
	Olga Zaichenko, Pavlo Galkin, Nataliia Zaichenko, Lydmila Golovkina	
3.	Approaches to Designing a Wireless Sensor Network Node for IoT Solution	10
	Anton Sukov, Alexey Zayanchukovsky, Vyacheslav Olizarenko, Pavlo Galkin	
4.	Intelligent Control and Monitoring Module for Uninterruptible Power Supply System <i>Andriy Palamar</i>	12
5.	Teaching microcontrollers and FPGAs in Quarantine from Coronavirus: Challenges	14
0.	and Prospects	
	Oleksandr Vorgul, Iryna Svyd, Oleg Zubkov, Valerii Semenets	
6.	Creation Features of Devices for Testing Nasal Breathing	18
	Yana Nosova, Maksym Tymkovych, Sofia Khudaieva, Ibrahim Younouss Abdelhamid, Oleg	
	Avrunin, Birgit Glasmacher	
7.	Remote Debugging of Embedded Systems in STM32CubeMonitor	22
	Oleksandr Velihorskyi, Ihor Nesterov, Maksym Khomenko	
8.	The Use of Percepio Tracealyzer for the Development of FreeRTOS-based	26
	Applications	
0	Maksym Khomenko, Oleksandr Velihorskyi Mathada of Organizing Communication Potwar Microsontucllors in the System of	20
9.	Methods of Organizing Communication Between Microcontrollers in the System of Monitoring Energy Consumption	30
	Sergiy Novoselov, Oksana Sychova	
10.	Using Remote Hardware Education Kit to Study Electronics Courses	34
101	Sergii V. Afanasiev, Nikita S. Poberezkyi, Sergey A. Ivanets	0.
11.	Fuzzy Logic Custom Instruction Set for NIOS II Processor	36
	Sergey A. Ivanets, Artem P. Fesenko, Oleksandr M. Fesiuk	
12.	Application of Software Signal Filtering in an Ultrasonic Rangefinder	39
	Artem Khromenko, Liliia Saikivska	
13.	Processes Analysis of Networks Management Systems	41
	Lubomyr Petryshyn, Wioleta Cieslik, Mykhailo Petryshyn	
14.	Visualization Modeling of Networks Management Systems	45
15	Lubomyr Petryshyn, Wioleta Cieslik, Mykhailo Petryshyn Dictores Training of Higher Education Specialists Using Virtual Presence	50
15.	Distance Training of Higher Education Specialists Using Virtual Presence Technologies	50
	Valerii Semenets, Oleg Avrunin, Tatyana Nosova, Evgen Chuguy, Yana Nosova,	
	Oleksandr Gryshkov	
16.	3D Printing in Online Education	53
	Hanna Zavolodko, Nataliia Haidar	
17.	Special Features of the Educational Component "Design of Devices on	55
	Microcontrollers and FPGA"	
	Iryna Svyd, Oleksandr Vorgul, Valerii Semenets, Oleg Zubkov, Valeriia Chumak,	
10	Natalia Boiko	F 0
18.	Literacy is an Important Factor in Professional Training of Modern Specialist <i>Viktoriia Tsyhanenko, Alla Serhiieva, Nataliia Ochkurova</i>	58

Features of the use of PID controllers when controlling evaporators

Oleg Zubkov ORCID 0000-0002-8528-6540 Department of Microprocessor Technologies and Systems Kharkiv National University of Radio Electronics Kharkiv, Ukraine oleh.zubkov@nure.ua Iryna Svyd ORCID 0000-0002-4635-6542 Department of Microprocessor Technologies and Systems Kharkiv National University of Radio Electronics Kharkiv, Ukraine iryna.svyd@nure.ua

Abstract—In the work, the features of the use of PID regulators for controlling evaporators are theoretically and experimentally analyzed, an algorithm for controlling the heating element of the evaporator is developed, and practical recommendations are given for choosing the parameters of the PID controller.

Keywords—PID controller, evaporator, microcontroller, algorithm, vapor

I. INTRODUCTION

In many automated control systems for technological processes in production, boiler equipment, electric motor control systems, proportional-integral-differential controllers (PIDs) are used. With their help, a constant value of any technological parameter is maintained. For example, a constant value of the temperature of the heat carrier in heating or cooling systems. The regulation problem in modern control systems is solved by microcontrollers in combination with measuring sensors and power modules. The theoretical foundations of the operation of classical PID controllers and their settings have been studied and described in many literature sources [1-4]. However, there is a specific group of control devices for which it is necessary to modernize the algorithms of the PID regulators and their mathematical description. These are vaporizers. In such devices, the process of liquid boiling takes place, in which all the energy transferred from the heating element to the evaporator is used not to increase the temperature of the liquid, but to transfer the liquid to vapor [5]. In evaporators, the PID regulator must maintain a fixed value of the volume of steam generated per unit of time. At the same time, when the PID controller is turned on, its reaching the operating mode is complicated by the fact that the thermodynamic processes in the evaporator before boiling and during boiling are different. These scientific studies were devoted to solving these problems, which are relevant for automated control systems. The solution of these main problems is inextricably linked with a number of aspects of an applied nature: the type of measurements - direct or indirect, the location of the measuring sensors, the choice of the measurement period and the correction period for the control action. Therefore, the purpose of the research was to develop an evaporator control algorithm and form recommendations for the selection of PID controller parameters.

Oleksandr Maltsev 42 ORCID 0000-0003-1520-9280 or Department of Microprocessor Technologies and Systems Radio Kharkiv National University of Radio Electronics Kharkiv, Ukraine aleksandr.maltsev@nure.ua

II. THEORETICAL PART

The principle of operation of the PID controller is that based on the measurement result of the main output parameter of the controlled system, the deviation of the current value from the required value is calculated and the value of the corrective action on the system is calculated [1, 3]

$$u(t) = P + I + D = K_p e(t) + K_i \int_{0}^{\tau} e(t) dt + K_d \frac{de}{dt}$$
(1)

where P is proportional component; I is integral component; D is differential component; e(t) is current error; Kp is proportional factor; Ki is integral coefficient; Kd is differential coefficient.

For evaporators with direct measurements, the main output parameter is the amount of steam generated. However, steam flow meters are very expensive devices with high measurement errors and specific measurements for various types of steam (water, alcohol, etc.). Therefore, when controlling the majority of modern evaporators, indirect measurements of vaporization are used through the temperature of the heating elements of the evaporator. Temperature is directly related to the amount of energy transferred to the evaporator and, accordingly, to the amount of steam generated.

Formula (1) is a continuous form of PID controller representation, which requires conversion to a discrete form for implementation on a microcontroller [2].

$$u(k) = K_p \left\{ \Delta x(k) + \frac{T_0}{T_{\text{int}}} \sum_{i=0}^k \Delta x(i-1) + \frac{T_d}{T_0} \left[\Delta x(k) - \Delta x(k-1) \right] \right\},$$
(2)

where k is discrete moment in time (kT_0) ; T_{int} is constant of integration; T_d is differentiation constant; T_0 is sampling period.

III. EQUIPMENT OF THE EXPERIMENTAL SYSTEM

As heating elements of the evaporation system, 2 kW electric heaters with triac control were used. Therefore, the PID regulator provided control of the electrical power transmitted to the load. Thermal resistances of the Pt1000 type were used to measure the temperature. In the board of the controller for controlling the triac, a circuit for detecting the zeros of the mains voltage is implemented, which made it possible to implement two main methods of controlling the triac during research: passing a part of the half-cycle of the mains voltage into the load or passing one of the set of half-periods. The controllers of the STM32F1 and STM32F4 series were chosen as control controllers.

IV. STUDY RESULTS AND PRACTICE RECOMMENDATIONS FOR EVAPORATOR CONTROL SYSTEMS

The software implementation of the standard PID controller operation algorithm according to (2) showed that the process of turning on the system is significantly extended in time in comparison with the calculation results, and overshoot is also observed in the control system. This is due to the transition from heating to boiling. To eliminate these effects at the initial stage of inclusion in the algorithm, a forced mode is introduced. In this mode, the power of the heating elements is maintained at a maximum until a predetermined temperature threshold is reached, the value of which can be either less than the operating value or higher. After that, the PID controller is turned on. However, at this moment the value of the integral component is equal to 0, since the integration is not performed from the moment the system is turned on. Therefore, the parameter of the initial value of the integral component is introduced, which makes it possible to compensate the accumulated value from the moment the system is turned on. The use of the forced mode ensured a quick activation of the system and the absence of fluctuations in the control system. Experimental studies have also shown that when the user gives commands to reduce the amount of steam per unit of time, the response value of the PID controller can drop to 0. This can lead to the termination of boiling, which is unacceptable for the evaporator. Therefore, a limitation was introduced on the minimum value of the control action of the PID controller.

Taking into account the proposed improvements, expression (2) was transformed to the form

$$u(k) = \begin{cases} u_{\max}, \ i < k_{START} \\ u_{\min}, \ u(k) < u_{\min}, \ i > = k_{START} \\ K_p \left(\Delta x(k) + I_{START} + \frac{T_0}{T_{\inf}} \sum_{i = k_{START}}^k \Delta x(i-1) + , \\ + \frac{T_d}{T_0} [\Delta x(k) - \Delta x(k-1)] \right) \end{cases}$$
(3)

where u_{max} the maximum power value of the evaporator heating elements; u_{min} the minimum value of the power supplied to the heating element in the operating mode of the evaporator; k_{START} moment of time from switching on to switching off the forced mode; I_{START} the initial value of the integral component at the moment of switching off the forced mode.

The optimal location for the temperature sensor is the outer surface of the heating element, since this provides a wide dynamic range of temperature measurements for the heating element. In the research stand, it reached 60°C.

Since the developed control algorithm was implemented on modern 32-bit microcontrollers with an ARM core, all calculations in the PID controller were performed with floating point. For STM32F1 microcontrollers, the calculation time does not exceed 80 μ s, and for STM32F4 microcontrollers, no more than 1 μ s due to the hardware DSP block. Thus, even the cheap STM32 microcontroller series can implement one or more PID controllers.

V. CONCLUSION

According to the classical theory of PID controllers, the differential component is influenced by noise, which manifests itself as fluctuations in the temperature measurements of the heating elements over time. With a normal distribution of measurement errors, the standard deviation decreases in proportion to the square root of the number of measurements. Experimental studies have shown that in order to achieve temperature fluctuations of no more than $\pm 0,07^{\circ}C$ smoothing should be implemented over a time interval of 1 s for 100 measurements. Such a time interval was chosen based on the provision of 100 discrete power levels of the evaporator heating elements, which correspond to 100 half-periods of the mains voltage for 1 s. A further increase in the value of this parameter is impractical, since a delay in the response of the PID controller to a change in the temperature of the heating elements begins to appear.

Experimental verification of the developed algorithm on a test bench has shown its efficiency and stability.

REFERENCES

- C.B. Kadua, C.Y. Patil. Design and Implementation of Stable PID Controller for Interacting Level Control System. Procedia Computer Science. Vol. 79, 2016, Pages 737-746.
- [2] J. Farshad Merrikh-Bayat, Nafiseh Mirebrahimi, and Mohammad Reza Khalil. Discrete-time fractional-order PID controller: Definition, tuning, digital realization and some applications International Journal of Control, Automation, and Systems, 2015 Vol. 13(1), pp. 81-90.
- [3] V. Chopra, S. K. Singla, and L. Dewan, "Comparative analysis of tuning a PID controller using intelligent methods," Acta Polytechnica Hungarica, vol. 11, no. 8, pp. 235–249, 2014.
- [4] Semenets V. V., Kratts Dzh., Nevlyudov I. Sh., Palagin V. A. Tekhnologiya mezhsoedinenii elektronnoi apparatury. Ucheb. dlya vuzov. Khar'kov: «SMIT», 2005.
- [5] Bambang Dwi Argo, Yusuf Hendrawan, Dimas Firmanda Al Riza, Anung Nugroho Jaya Laksono. Optimization of PID Controller Parameters on Flow Rate Control System Using Multiple Effect Evaporator Particle Swarm Optimization. International journal on advanced science engineering information technologies. Vol.5 (2015) No. 2. pp. 6-12.

MC&FPGA-2020

Realisation of Iterative Algorithm of Six-Port Reflectometer on FPGA Using Logarithm Function

Olga Zaichenko ORCID 0000-0003-4936-2785 dept. Design and Operation of Electronic Devices Kharkiv National University of Radioelectronics Kharkov, Ukraine olha.zaichenko@nure.ua

Nataliia Zaichenko ORCID 0000-0001-9798-7136 dept. Design and Operation of Electronic Devices Kharkiv National University of Radioelectronics Kharkov, Ukraine nataliia.zaichenko@nure.ua

Abstract—The six-port reflectometer is an universal measurement device of microwave range for signal power and tract termination reflection coefficient definition. The definition of such tract and termination parameters is made by sensor signal processing. As processing algorithm can be used least squares estimation. The advantages of least squares estimation is accuracy. The condition of its use is redundandant sensor number. The least squares estimation feature is invers matrix computation. As to FPGA realisation of algorithm there are problems connected to matrix inversion. So the report is devoted to attempt to simplify six-port reflectometer sensor signal processing and to avoid inverse matrix computation.

Keywords—six-port reflectometer, processing algorithm, least squares estimation, logarithm

I. INTRODUCTION

The six-port reflectometer [1, 4, 5] consists of waveguide section and processing and indication block. The processing and indication block can be realized on FPGA.

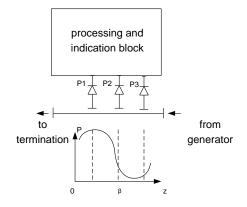


Fig. 1. The six-port reflectometer with three sensors.

The waveguide section located between generator and termination. Due to electromagnetic wave reflection from termination inside waveguide section is standing wave. There are sensors along standing wave in the waveguide. The Pavlo Galkin ORCID 0000-0002-0558-6448 dept. Design and Operation of Electronic Devices Kharkiv National University of Radioelectronics Kharkov, Ukraine pavlo.halkin@nure.ua

Lydmila Golovkina ORCID 0000-0001-5929-3256 dept. Design and Operation of Electronic Devices Kharkiv National University of Radioelectronics Kharkov, Ukraine liudmyla.holovkina@nure.ua

sensors signals proportional to intensity of electromagnetic wave in their position. To extract information about signal power and reflection coefficient modulus ana phase it is necessary process sensor signals by definite algorithm. As mathematical model of ideal six-port reflectometer is system of linear equation, where each equation corresponds to one sensor, to get algorithm is necessary to solve the system of linear equation through inverse matrix, unlike non ideal sensor processing. Processing of non ideal sensors demand more complicated algorithm, for example, least squares estimation.

The problem of this research is contradiction between accounting an uncertainity of measurement by mean of complication processing methods and realization of computation methods on FPGA, using hardware description language VHDL, where computation mathematics should be implemented by hardware units.

II. ITERATIVE ALGORITHM OF SIX-PORT REFLECTOMETER

Lets sensor number exceed unknown intermediate variable number. As mathematical model we have redundant system of linear equation [1]. The solution of such system through the least squares estimation is

$$\begin{bmatrix} b \end{bmatrix} = \left(\begin{bmatrix} A \end{bmatrix}^T \begin{bmatrix} A \end{bmatrix} \right)^{-1} \begin{bmatrix} P \end{bmatrix}.$$
(1)

To avoide inverse matrix calculation lets apply iterative Seidel algorithm

$$b_{0} = \frac{1}{f_{11}} \{ a_{11}p_{1} + a_{21}p_{2} + a_{31}p_{3} + a_{41}p_{4} - (f_{12}b_{1} + f_{13}b_{2}) \}$$

$$b_{1} = \frac{1}{f_{22}} \{ a_{12}p_{1} + a_{22}p_{2} + a_{32}p_{3} + a_{42}p_{4} - (f_{21}b_{0} + f_{23}b_{2}) \} (2)$$

$$b_{2} = \frac{1}{f_{33}} \{ a_{13}p_{1} + a_{23}p_{2} + a_{33}p_{3} + a_{43}p_{4} - (f_{13}b_{0} + f_{32}b_{1}) \}$$

where system matrix is

$$[A] = \begin{pmatrix} 1 & \cos\phi & \sin\phi \\ 1 & 1 & 0 \\ 1 & \cos\phi & -\sin\phi \\ \dots & \dots & \dots \\ 1 & \cos n\phi & -\sin n\phi \end{pmatrix},$$
 (3)

matrix column of sensor signals is

$$[P] = (P_1 \ P_2 ... P_n)^T.$$
(4)

Intermediate variable is

$$\begin{bmatrix} b \end{bmatrix} = \begin{pmatrix} b_1 b_2 \dots b_n \end{pmatrix}^T.$$

Definition for intermediate variables is

$$b_0 = P_{inc} (1 + \Gamma^2),$$

$$b_1 = \Gamma P_{inc} \cos \phi,$$

$$b_2 = \Gamma P_{inc} \sin \phi,$$
(6)

where Γ is reflection coefficient modulus, φ is reflection coefficient phase, θ is phase distance between neighbouring sensors, P_{inc} is incident power. For expression (2) also necessary expression. They are calculated from information Fisher matrix

$$\begin{split} f_{11} &= a_{11}^2 + a_{21}^2 + a_{31}^2 + a_{41}^2 \\ f_{12} &= a_{11}a_{12} + a_{21}a_{22} + a_{31}a_{32} + a_{41}a_{42} \\ f_{13} &= a_{11}a_{13} + a_{21}a_{23} + a_{31}a_{33} + a_{41}a_{43} \\ f_{21} &= a_{11}a_{12} + a_{21}a_{22} + a_{31}a_{32} + a_{41}a_{42} \\ f_{22} &= a_{12}^2 + a_{22}^2 + a_{32}^2 + a_{42}^2 \\ f_{23} &= a_{12}a_{13} + a_{22}a_{23} + a_{32}a_{33} + a_{42}a_{43} \\ f_{31} &= a_{11}a_{13} + a_{21}a_{23} + a_{31}a_{33} + a_{41}a_{43} \\ f_{32} &= a_{12}a_{13} + a_{22}a_{23} + a_{32}a_{33} + a_{42}a_{43} \\ f_{33} &= a_{13}^2 + a_{23}^2 + a_{33}^2 + a_{43}^2 \end{split}$$

Analysis of expression shows that on VHDL should be realised summation, multiplication and exponentiation.

III. HARDWARE IMPLEMENTATION

In the paper [2],an FPGA-based single precision floating point hybrid iterative architecture for solving a linear system of equations is proposed. The whole design has been implemented in Verilog HDL, having Virtex 7 XCV2000T as targeted device. The design optimizations include using modified high-speed radix 4 multiplier and optimized highspeed 2's complementer. The Radix-4 Booth Encoded multiplier is the most speed efficient and area efficient among other higher radix Booth Encoded multipliers. The partial products required for computation are significantly reduced compared to the traditional multipliers. These partial products are added using a Dadda tree structure and the final summation is carried out using a Koggestone adder.

This approach has many advantage and it is verified, but we propose an idea of alternative solution. The idea is borrow from operational amplifier. The idea is instead of calculation of product there is made calcultion of sum of multipicant logarithm.

The logariphm calculation is performed by such methods as: 1) recursive algorithm for calculating the logarithm; 2) the comparison method to 2; 3) discrete logarithm; 4) logariphm ruler, 5) lookup table. The elements of this approach are contained in [3].

The second method, comparison to 2 method algorithm is: 1. The number is compared to 2; 2. If greater than 2: then divide it by 2 and go to 1 step; 3. if less than 2, but more than 1: then remember the number of divisions by 2 (this there will be an integer part of the logarithm); 4. output the result. Advantages: 1) Possibility of implementation on logic elements; 2) Speed of calculations. Disadvantages:1) Calculates only an integer, without a remainder.

IV. CONCLUSION

There was proposed new iterative method of six-port reflectometer sensor signal processing. It is based on least squares estimation iterative calculation by Seidel method for example. It allows to avoid inverse matrix calculation and leaves only calculation of sum and product. There was worked out procedura for computation.

Implementation of such algorithm on FPGA is considered from hardware point of view. The inherited from operational amplifiers logarithmic transformation, i.e. instead of calculation of product there is made calcultion of sum of multipicant logarithm lays in its foundation.

REFERENCES

- O. Zaichenko, P.Galkin, N. Zaichenko, and M. Miroshnyk, "Six-port Reflectometer with Kalman Filter Processing of Sensor Signals,". IEEE 15th International Conference on Advanced Trends in Radioelectronics, Telecommunications and Computer Engineering (TCSET), pp. 55-58, February2020.
- [2] R. Joshi, A. Raghuvanshi, Y. Gilhotra, S. Sharma, S. Sharma, P. Dalmia, and N. Pandey, "An FPGA based floating point Gauss-Seidel iterative solver," 14th IEEE India Council International Conference (INDICON), pp. 1-6, December2017.
- [3] Usirkov K. V. "Analysis of mathematical operation realization on FPGA," Master dissertation, South-Ural state university, 2016, 48 p.
- [4] O. Zaichenko, M. Miroshnyk and P. Galkin, "Signal Flow Graph for Optimizing of Mutual Sensors Reflection in the Multiprobe Microwave Multimeter," 2019 IEEE 2nd Ukraine Conference on Electrical and Computer Engineering (UKRCON), Lviv, Ukraine, 2019, pp. 200-203, doi: 10.1109/UKRCON.2019.8879925.
- [5] O. Zaichenko, P. Galkin and M. Miroshnyk, "Model and Algorithms for Microwave Mutiport Receiver," 2019 IEEE International Scientific-Practical Conference Problems of Infocommunications, Science and Technology (PIC S&T), Kyiv, Ukraine, 2019, pp. 1-4, doi: 10.1109/PICST47496.2019.9061275.

Approaches to Designing a Wireless Sensor Network Node for IoT Solution

Anton Sukov

dept. Design and Operation of Electronic Devices Kharkiv National University of Radioelectronics Kharkov, Ukraine anton.sukov@nure.ua

Vyacheslav Olizarenko

dept. Design and Operation of Electronic Devices Kharkiv National University of Radioelectronics Kharkov, Ukraine viacheslav.olizarenko@nure.ua

Abstract—The object of the research is the hardware component for building a test platform for wireless sensor networks. The aim of the work is to develop a software and hardware test platform for wireless sensor networks. As a result of the analysis, the node structures, wireless sensor network modules, CC2530 peripherals were analyzed. A module based on the CC2530 PA was chosen as the hardware. Given to optimize the structure of the node for as one of approach to designing a wireless sensor network node. Also given report about difference in approach to designing nodes and uses areas. All developments will receive life in the educational process of the department. Sample production is already underway.

Keywords—approach, CC2530, software and hardware test platform, node, wireless sensor network

I. INTRODUCTION

The Wireless sensor networks (WSN) systems have a lot of problems like security, energy consumption, heterogeneity and other disadvantages that need be solved [1]. Therefore, it is quite difficult to design a sensor network node so that it satisfies the necessary criteria for optimality. If such a node is also used for testing and training, then additional requirements for the construction will be propose to, for example, as in articles of designing microprocessor systems [2] or embedded control systems [3]. Energy monitoring [4] is a key factor for the successful prolongation of life times each nodes in wireless sensor network, for examples reducing the power consumption of nodes [5]. Therefore, can set the task to optimize the structure of the node for as one of approach to designing a wireless sensor network node.

The purpose of the work is to develop a software and hardware test platform for the Internet of Things.

The first part the development of a test IoT layout, namely, a communication module based on the CC2538 radio transceiver.

The second part development of a test IoT layout. Communication module based on the CC2530 radio transceiver.

Alexey Zayanchukovsky

dept. Design and Operation of Electronic Devices Kharkiv National University of Radioelectronics Kharkov, Ukraine oleksii.zaianchukovskyi@nure.ua

Pavlo Galkin ORCID 0000-0002-0558-6448 dept. Design and Operation of Electronic Devices Kharkiv National University of Radioelectronics Kharkov, Ukraine pavlo.halkin@nure.ua

The third part is development of a test IoT layout, namely, a communication module based on the ESP8266 radio transceiver.

II. CC2530 NODE FOR IOT

The CC2530 contains many peripherals that provide everything to develop various applications. The debugging interface uses I/O ports P21 (data) and P22 (synchronization) in debug mode. In this case, in the debug mode, the other 19 ports pins can be active, which gives a great opportunity to debug the module, while at the same time it can be connected to quite a few different devices. In other cases, the ports for debugging can work in the normal GPIO mode. In general, the debugging interface allows you to track all processes that occur in the module when it is in an active state (user program execution), and also to change the parameters of these processes (for example, values in registers) and in real time to observe changes in the work of the module.

As a result of the analysis, the node structures, wireless sensor network modules, peripherals CC2530 were analyzed. A module based on CC2530 PA was chosen as the hardware. Elements such as:

- LEDs ;
- push buttons;
- photoresistor;
- humidity sensor;
- ultrasonic sensor;
- exits to the outer periphery.

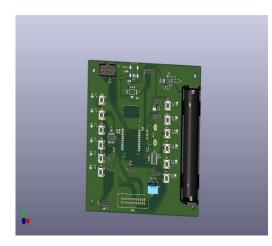


Fig. 1. Developed PCB board base on CC2530.

III. CC2538 NODE FOR IOT

The CC2538xFnn is the ideal wireless microcontroller System-on-Chip (SoC) for high-performance ZigBee applications. The device combines a powerful ARM Cortex-M3-based MCU system with up to 32KB onchip RAM and up to 512KB on-chip flash with a robust IEEE 802.15.4 radio. This enables the device to handle complex network stacks with security, demanding applications, and over-theair download.

As a result of the analysis, the node structures, wireless sensor network modules, CC2538 peripherals were analyzed. A module based on the CC2538 was chosen as the hardware. As elements of the periphery, the following elements were chosen:

- LEDs;
- push buttons;
- Temperature, humidity and pressure sensor in the one case;
- Buzzer;
- hall sensor;
- lighting sensor;
- voltage divider with adjustable resistor.

A contact switch is selected to switch between the peripheral elements, and electrical switch for switching between external and internal peripheral (Fig. 2).

IV. ESP8266 NODE FOR IOT

The ESP8266 is a low-cost Wi-Fi microchip, with a full TCP/IP stack and microcontroller capability, produced by Espressif Systems in Shanghai, China.

Proposed developed PCB board base on ESP8266 shown on Fig.3.

V. CONCLUSION

The topic of the modern concept of IoT and the possibilities of the ZigBee protocol were considered. Similar devices were considered. The selected module and its

capabilities were considered. The model is developed, its separate possibilities and components are considered.



Fig. 2. Developed PCB board base on CC2538.



Fig. 3. Developed PCB board base on ESP8266.

REFERENCES

- [1] C. Alvarado, F. Bosquez, Palacios and L. Córdoba, "Low-energy Adaptive Clustering Hierarchy protocol and optimal number of cluster head algorithm in a randomized wireless sensor network deployment," 2017 International Conference on Electrical, Electronics, Communication, Computer, and Optimization Techniques (ICEECCOT), Mysuru, 2017, pp. 1-4. doi: 10.1109/ICEECCOT.2017.8284632.
- [2] V. Semenets, "Technical aspects for development laboratory base for learning FPGA and microcontroller systems," 2009 10th International Conference - The Experience of Designing and Application of CAD Systems in Microelectronics, Lviv-Polyana, 2009, pp. 145-145.
- [3] P. Galkin, "Razrabotka laboratornogo kompleksa po izucheniyu vstraivaemyih sistem upravleniya i promyishlennoy avtomatizatsii [Development of a laboratory complex for the study of embedded control systems and industrial automation]," Materials of the 21st International Youth Forum "Radio Electronics and Youth in the 21st Century", April 25-27, 2017 Conference "Automated systems and computerized technologies of radio-electronic instrument-making", Kharkiv, KNURE, vol. 2, P.94-95. (In Russian).
- [4] P.V. Galkin. "Analiz energopotrebleniya uzlov besprovodnih sensornih setei [Analysis of power consumption of nodes of wireless sensor networks]," ScienceRise, no.2 pp 55-61, 2014. (In Russian).
- [5] P. Galkin, "Model of Reducing the Power Consumption for Node of Wireless Sensor Network in Embedded Control Systems," 2018 International Scientific-Practical Conference Problems of Infocommunications. Science and Technology (PIC S&T), Kharkiv, Ukraine, 2018, pp. 252-256. doi: 10.1109/INFOCOMMST.2018.8631891.

II International Scientific and Practical Conference Theoretical and Applied Aspects of Device Development on Microcontrollers and FPGAs

MC&FPGA-2020

11

Intelligent Control and Monitoring Module for Uninterruptible Power Supply System

Andriy Palamar ORCID 0000-0003-2162-9011 Computer Systems and Networks Department Ternopil Ivan Puluj National Technical University Ternopil, Ukraine palamar.andrij@gmail.com

Abstract—This paper proposes an intelligent control and monitoring module for industrial uninterruptible power supply systems. The structure scheme of the module based on the parallel connected of two microcontrollers with ARM architecture is designed. The software for the module is developed and implemented.

Keywords—control system, monitoring, microcontroller, uninterruptible power supply.

I. INTRODUCTION

Industrial uninterruptible power supply (UPS) systems are widely used in order to ensure high quality power supply and protection of electronic equipment from failure. One of the most important components of modern UPS is a computer information and measurement system [1].

In most UPS, the core of such system is a microprocessor or microcontroller that performs all of the monitoring and control functions. Quite often, UPS is used to provide guaranteed power to remote objects to which the operator does not have constant access, so there is a requirement for remote monitoring of the device and its electrical parameters.

In the software and hardware complex, which was developed by the author [2, 3], the process of data transfer to a PC for remote monitoring is implemented using the Ethernet protocol, which requires significant hardware and software resources of the microcontroller. On the other hand, the process of battery charge management also requires significant computing power, as it requires operations of analog-to-digital conversion of electrical signals, and rapid response to changes in measured data depending on the control mode.

The combination of these tasks creates a significant load on the computing power of the microcontroller, which in turn reduces the response rate to changes in the electrical parameters of the battery, which is critical during transients during battery charging. To solve this problem, this paper proposes design and implementation of a two-core information and measurement control system for an uninterruptible power supply system, which implements the principle of parallelization of tasks.

The purpose of the work is to increase the reliability and efficiency of the industrial UPS control module by using parallel operation of two 32-bit microcontrollers.

II. THE STRUCTURE OF THE MODULE

The UPS control module implements functions of electric parameters measurement and battery charge management process, check a condition of alarm signals, provides an opportunity of archiving of the measured data, carries out transfer of the received information to the personal computer.

The schematic block diagram of the control and monitoring module for uninterruptible power supply system is shown in Fig. 1. The structure of the module contains:

- two microcontrollers (STM32F103 and AT91SAM7X512);
- conversion and amplification circuit for receiving input analog signals;
- circuit that is responsible for receiving digital input signals;
- non-volatile memory chip for storing received data;
- USB and Ethernet controllers for PC connection;
- keyboard and LCD for user interaction.

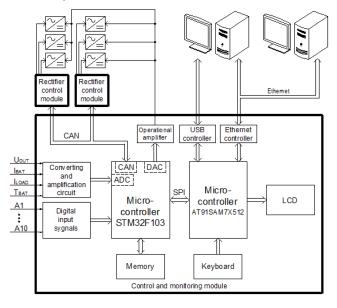


Fig. 1. Block diagram of the control and monitoring module for uninterruptible power supply system.

Two 32-bit microcontrollers based on the ARM architecture provide basic control and monitoring functions of the UPS. The STM32F103 microcontroller contains builtin 16-channel 12-bit analog-to-digital converter (ADC) and two-channel digital-to-analog converter (DAC). It is responsible for performing tasks that require frequent checking of the system status and measuring its electrical parameters by using ADC. This microcontroller provides fast response to their change by generating an analog control signal for UPS rectifier modules using DAC. In addition, this microcontroller performs the function of controlling the operating modes of the USP such as battery charge process, residual capacity testing, etc.

The AT91SAM7X512 microcontroller with integrated Ethernet, CAN and USB interfaces is responsible to perform tasks that are not time-critical. For example, displaying of the measured data on the LCD display, reading the keyboard, transferring the information to the server for its storage in database and further processing. Serial peripheral interface (SPI) is used to provide fast and reliable data exchange process between these microcontrollers.

After the conversion and amplification, voltage, currents, and temperature signals are measured by using inner analogto-digital converter of the STM32F103 microcontroller. All deviations of the measured data from the normal values, alarms as well as time of an event are stored in a non-volatile memory.

The received data are visualized on the LCD on the front of the module. Electrical parameters of the system can be set or changed using the keyboard with four buttons. Digital signals of the UPS status are being read periodically by using the input output ports of the microcontroller. Real time clock is used to keep track of the current time.

A prototype of the designed control and monitoring module is illustrated in Fig. 2.



Fig. 2. A prototype of the control and monitoring module for an uninterruptible power supply.

III. THE SOFTWARE OF THE MODULE

The software of the control and monitoring system comprises of two parts. The first one is firmware for the microcontrollers. It is written by using C programming language. The second part of the software is a computer monitoring application – graphical user interface (Fig. 3).

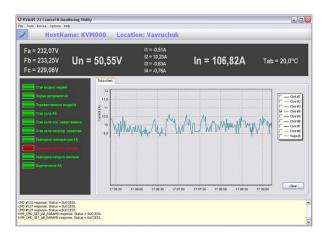


Fig. 3. Graphical user interface of UPS monitoring system for PC.

The main program of the microcontrollers includes the following subroutines: system initialization; data collection and processing; monitoring and display unit; control unit; data transfer unit.

The function of data collection and processing unit is to provide digitizing of the measured data and their previous processing. Information required to be collected includes: output voltage; battery current; load current; battery temperature. These data are used for management purposes of the control system.

The monitoring and display unit is designed to visualize the measured information on the LCD in a real-time and to provide access to archived data. Furthermore, it allows one to set and to modify parameters of the system.

Data transfer unit is responsible for transmitting the information to the computer through the Ethernet or USB interface. The amount of data to be transferred includes: the measured information, electrical parameters of the system, and the archived data from the memory of the module.

IV. CONCLUSIONS

In this paper an intelligent control and monitoring module for UPS system was designed and implemented. The results of experimental tests of the developed module shows that the technology of parallelization of tasks by using two microcontroller allows to increase the reliability and efficiency of the control system for an uninterruptible power supply.

REFERENCES

- T. Addabbo, A. Fort, M. Mugnaini, V. Vignoli. "Distributed UPS control systems reliability analysis," Measurement, 2017, Vol. 110, pp. 275–283. doi: 10.1016/j.measurement.2017.06.021
- [2] A. Palamar, M. Karpinskyy. "Control of an uninterruptible power supply in a DC microgrid system," 10th International Symposium Symposium "Topical Problems in the Field of Electrical and Power Engineering" and "Doctoral School of Energy and Geotechnology II", Pärnu, Estonia. 2011, pp. 80–84.
- [3] A. Palamar, M. Karpinskyy, V. Vodovozov. "Design and implementation of a digital control and monitoring system for an AC/DC UPS," 7th International Conference-Workshop "Compatibility and Power Electronics" CPE 2011, Tallinn, Estonia. 2011, pp. 173–177. doi: 10.1109/CPE.2011.5942227



Teaching microcontrollers and FPGAs in Quarantine from Coronavirus: Challenges and Prospects

Oleksandr Vorgul ORCID 0000-0002-7659-8796 Department of Microprocessor Technologies and Systems Kharkiv National University of Radio Electronics Kharkiv, Ukraine oleksandr.vorgul@nure.ua

Oleg Zubkov ORCID 0000-0002-8528-6540 Department of Microprocessor Technologies and Systems Kharkiv National University of Radio Electronics Kharkiv, Ukraine oleh.zubkov@nure.ua

Abstract—Modern equipment is becoming more and more complex and education establishment must keep up with it and offer its contribution to the overall progress. The goal of this work is to find the way how to survive on self-isolation and teach microcontrollers and FPGAs. What challenges need to be overcome and what prospects may open up.

Keywords—digital signal processing; microprocessor; STM32; programmable logic integrated circuits; learning online

I. INTRODUCTION

We were studying and teaching microcontrollers and FPGA. And suddenly a corona virus, quarantine and self-isolation. So we are self-isolated together. The bosses continued to lead the educational process in isolation from teachers, teachers teach in isolation from students, students should have an opportunity and a feedback channel.

Man is a social being, and non-verbal communication methods appeared earlier than speech. What is my point? Work in self-isolation in a trivial form can be reduced to the distribution of teaching materials, which excludes contact in the "teacher-student" system. And the channels, verbal and non-verbal, are closed. Therefore, the upbringing process is actually terminated. Furthermore, for hardware specialties, it is also important that students have, let's say, less opportunities to explore equipment on their own and gain practical experience with real equipment, not its simulation model or with just a theory. And this is not seems to be good.

Despite the fact that the teaching load during selfisolation, according to subjective feelings, is much greater than with the contact form of training, quarantine is something new, while exploring it one can get a new quality and finally improve.

II. WHAT EXPIRIENCE CAN WE FIND IN THE INTERNET

Along with self-isolation, it became possible to visit the Coursera platform [1], to participate on the student's part in

Iryna Svyd ORCID 0000-0002-4635-6542 Department of Microprocessor Technologies and Systems Kharkiv National University of Radio Electronics Kharkiv, Ukraine iryna.svyd@nure.ua

Valerii Semenets ORCID 0000-0001-8969-2143 Department of Microprocessor Technologies and Systems Kharkiv National University of Radio Electronics Kharkiv, Ukraine valery.semenets@nure.ua

courses on our interests, to imagine what the creation of such a course in our disciplines will mean, in which direction it can be continued and for fun.

The following were selected as experimental courses:

- Digital Signal Processing from École Polytechnique Fédérale de Lausanne;
- Digital signal processing (in Russian) from the Polytechnic University, St. Petersburg;
- Hardware Description Languages for FPGA;
- Embedded Hadrware and Operation system from the University of Turku.

In each course, the platform offers:

- *A. Presentation of the course. Like video annotations and self-promotion.*
- B. The course being structurized on the weekly blocks with summing up the final results and issuing certificates.
- C. Each block contains:
 - Video lectures with video text. Basically, courses on the platform are in English. The courses were not specially selected from universities in different countries, it happened unintentionally. In terms of pronunciation and understanding, the French course is distinguished by perhaps excellent English with a good writing style and the use of Python to illustrate the use of digital processing. Russian course contain a serious theoretical approach and emphasis on MATLAB. Colorado Course – in American English, contrasting with English from Lausanne – has a well-thought-out system of practice. Tasks for modeling HDL nodes are made in the ModelSim program. The simulation result is an HDL file in one of the modeling languages. The course consists of

two parts, which are the same in structure, but with slightly different presentation styles due to the fact that it is taught by different teachers. The highlight of the Colorado course is the use of a proprietary testbench file format (the student cannot make changes to this file) to validate the assignment. As a result, the verification of the correctness of the scheme is performed on the website of the course compiler using the data file generated by the testbench file.

- There is text below the video lecture. It is synced to the video if the video is running or paused using an underline. The platform provides a translation button for other languages, but it seems that this will appear in the next version.
- During video playback, it is possible to insert small questions for the listener, which stimulates the listener to pay more attention to watching the video, and not to perceive it as background noise. However, correct or incorrect answers to simple questions do not affect the overall rating.
- In addition to video, it is possible to use text materials for classes (files with examples of solved problems, pdf format, scripts with programs illustrations in python).
- After studying the above material, the student is asked to take a test. The compiler of the course has the right to decide whether to allow passing the next item (practical task). Stating the pass level of rating, if there are several tests, the compiler of the course can prohibit the transition to the next part if the previous one has not been completed. So you can build different strategies.
- During the test, you need to complete the task and enter the answer in the form of one number in the whole format, with a fixed point or in the form of a formula. Formulas are introduced in an unusual way, but you can get used to it. As with any other minor problem, entering answers in the form of arrays of numbers can cause problems for listeners. They need to be promptly answered by the course compilers, so the work here requires patience and attention from both sides.

In terms of using a platform that is essentially paid, the interest of the listener is maintained. Apparently, the moderators stimulate the creators of the courses, or competition affects the fact that the course for the student is interesting and well received. The level of the student at the entrance to the course is not checked and in order to fulfill the interestingness and perceptibility one has to choose between the fundamental nature of the course and its popularity.

If the student does not fit into the work schedule, he is offered a transfer of dates of classes. A rather high volume of rhythmic work is required from the listener. The courses, in principle, indicate the time spent in hours and minutes, which, according to the authors, are required to complete a particular task, but, of course, this is very individual. Conclusion: good idea. Either theory or hardware modeling is proposed for study. Suitable for learning languages (foreign or programming) very well, but this is not our case. When studying electronic circuits, digital or analog, simulation is used. But we need a sound training on hardware issues and it is a completely different story.

III. HOW GOOD OUR ENVIREMENT WAS BEFORE THE CARANTINE

With an in-class, contact version of training, an educational institution has the opportunity to spend funds on the purchase of equipment and time for training personnel in order to confirm its relevance in the educational services market, where we are so amicably going. And with the interest of all parties to the process: students, teachers and employers, the listener at the exit should be ready for a smooth and comfortable transition from training to professional activity. Taking into account the realities existing before the quarantine, the experience of the teaching staff and the technical equipment of the staff makes it possible to train a technical specialist from a student [2]. However, an important component of the result is the listener's motivation, which there is still room for improvement.

IV. WHAT FUTURE DO WE DREAM ABOUT?

Our goal is to bring back full laboratory work. Apparently, mixed learning can be a good option - contact with support of the online version, this is possible if you provide layouts for use over the network. This will require changes to the educational process. There is complete certainty here only in one thing: it will not be easier than in the contact version.

After spending nearly four months in deep online, what are our is the general first impression? As for me, I don't like the situation as it is. Let me rename what exactly.

A. Motivation falls.

Both on the part of the student and on the part of the teachers. It needs to be somehow supported in terrible conditions (no prestige, no decent salary, few points of application of forces are visible, it is hard to see what will happen next).

B. Teacher load has increased.

Why? But because all the plans, the most individual ones, suggest a stationary regime. Usually we plan in July and we carry out our load the whole year, and the high authorities do not throw additional task as a pleasant surprise. And even there is enough time for scientific work. But we now have a transitional regime. We pass from one stationary state to another. And if the current stationary state can somehow be described, then what will happen in the future is not clear and there are prospects in this: you can try to change something. Let's hope for the best changes in the quality learning environment.

C. Platforms such as Coursera - it is payable, modern and it works.

For the instructor, this is an additional burden of mastering, course installation (both are once), update and support (both are all the time).

D. Conducting classes online for a theoretical or praktical course.

Conducting classes online for a theoretical course, from one side, and hardware like microprocessors and FPGAs, from another side are very different. It is necessary to come up with an active part of the assignment for the student so that it is feasible and not by copypasting or rewriting.

E. With software.

Three parts of the course. Digital processing is process modeling, STM32 microprocessors and FPGAs [5-11]:

- For digital processing, Matlab is actually the standard. In the installation of the student part of the course, especially online, you have to require students to install programs. There are free, trial, online versions of Matlab. Students balk and look for reasons to get out (here: low motivation!). Instead of Matlab, you can try Octava or Python with libraries that are free software or free. For such software, there are no fundamental problems to implement the same task as for Matlab, but the time (which is not) to enter the mode and develop a digital copy of the course increases.
- STM32. There are several options for proprietary software (free), for many platforms, for Windows, Linux and MAC OS. You can build a course based on paid software with the support of sponsors from production.
- There is no such diversity for FPGAs. Chip and evaluation board manufacturers offer large, complex software, often for a fee [3, 4]. Simulation options are available for HDL hardware description languages - VHDL and Verilog. So far we are only interested in VHDL. For this case, there exists a student version of ModelSim for Windows that also supports Verilog. As for Linux, GHDL and FreeHDL for Linux, but if you switch to Verilog, you will need to change the software. Mixed projects are problematic.

The university staff has developed a sufficient number of hardware platforms for laboratory workshops and proposed several approaches to solving the problems of remote access to laboratory equipment, presented in [5-15].

Conducting laboratory work on hardware online is a real challenge, which is currently at the stage of testing the optimal use cases.

V. CONCLUSIONS

In the days of offline learning, the main form of education was lecture. Its support was a book (textbook and study guide) and consultations. To obtain practical skills we could use practical classes and laboratory works, qualitatively wrapped in preparation for classes by students, preparation of class time material and homework by teachers and high-quality, albeit sometimes tedious, defense of laboratory work. But practical and laboratory ones are nevertheless carried out under the guidance of a teacher, although they contain some of the student's independent work.

In the case of online classes, the lecture in the form of a file is ineffective; lecture-video, with questions-tasks during playback is much better. Information can be dosed in small portions. And leave part of the material in the reference form. A good form of lecture is a presentation with sound, in which the lecturer has the opportunity to draw explanations and graphs on the finished material. The advantage of online learning is that it is quite easy to add multimedia illustrations - video clips or sound effects.



Fig. 1. Laboratory work place.



Fig. 2. Laboratory work place [5].

It is more difficult with practical tasks. They should not be long, mandatory for the student and with increasing difficulty from task to task. Laboratory work, like working in software (for a theoretical course) or with hardware (for microcontrollers and FPGAs), is more difficult in a remote implementation. And we really have little experience in conducting classes with hardware and providing students

II International Scientific and Practical Conference Theoretical and Applied Aspects of Device Development on Microcontrollers and FPGAs

MC&FPGA-2020

with access to the equipment of the department (Fig. 1 and Fig. 2).

Alternatively, in the software, the student writes a program on his remote computer. This will require the installation of specialized software on his computer. But then the student will have the opportunity to perform all operations up to loading the program into the board and incircuit debugging on a remote computer. Upon successful completion of this part, the student should be provided with remote access to the board physically located in the department. And to the measuring instruments correctly connected to the board. To implement such a regime, a sequence of problems arises.

Problem 1. It is necessary to organize the provision of remote access to the student's hardware by means of the operating system or third-party software. Distribute available computers, boards and measurement equipment to students and avoid conflicts.

Problem 2. At the first stage, it is likely that laboratory technicians are required to support such exercises. In addition to mechanical and logical connections, the staff must be able to complete laboratory work in full and be prepared for non-standard situations.

Problem 3. It is necessary to think about whether it is possible to compose and implement tasks for laboratory work with a board, automatically checked online. Or, nevertheless, without physical contact, everything will degenerate into a demonstration to the student on video how someone is doing laboratory work.

Today, there are many organizational and technical issues that have to be solved in the near future to improve the quality of distance education.

REFERENCES

- [1] Coursera. 100% online education Official website http://www.coursera.org/
- [2] F. Morgan et al., "Remote FPGA Lab with Interactive Control and Visualisation Interface," 2011 21st International Conference on Field Programmable Logic and Applications, Chania, 2011, pp. 496-499, doi: 10.1109/FPL.2011.98.
- [3] Nicole Hemsoth, Timothy Prickett Morgan FPGA Frontiers: New applications in reconfigurable computing. Xilinx, Published by Next Platform Press, 2017, 87 p.
- [4] Quartus® Prime Standard Edition Handbook. Intel Corp., 2017.

- [5] Valerii Semenets, Liliia Saikivska, Iryna Svyd, Oleksandr Maltsev. Trends in Training Modern Technicians. // First International Scientific and Practical Conference «Theoretical and Applied Aspects of Device Development on Microcontrollers and FPGAs» MC&FPGA-2019, Kharkiv, Ukraine, July 26-27, 2019, pp. 35-36. doi: 10.35598/mcfpga.2019.013
- [6] Iryna Svyd, Oleksandr Maltsev, Oleg Zubkov, Liliia Saikivska. Matlab Use in Design of Digital Systems on the FPGA in CAD Xilinx VIVADO. // First International Scientific and Practical Conference «Theoretical and Applied Aspects of Device Development on Microcontrollers and FPGAs» MC&FPGA-2019, Kharkiv, Ukraine, July 26-27, 2019, pp. 29-30. doi: 10.35598/mcfpga.2019.010
- [7] V. Semenets, I. Svyd and L. Saikivska, "Methods of improving the quality of preparation of technical specialists", inEngineering education: challendes and developments: materials of the IX International Scientific and Methodological Conference, Minsk, Belarus, 2018, pp. 415-416.
- [8] V.S. Chumak, I.V. Svyd. Testimonial Modern trends in the training of technical specialists. // Modern education - accessibility, quality, recognition: a collection of scientific papers of the XI International Scientific and Methodological Conference, November 13-14, 2019, Kramatorsk - Kramatorsk: DSEA, 2019. - pp. 245-247.
- [9] I.V. Svyd, O.V. Litvinenko, O.G. Bilotserkivets. Features of designing digital devices based on Xilinx FPGA in CAD Vivado HLx Design Suite. // Specialized Exhibition "KharkivProm Days. Production and efficiency". Collection of materials of the forum section "Automation, electronics and robotics. Development Strategies and Innovative Technologies". - Kharkiv, KNURE, Exhibition Company ADT, 2019, pp. 43-44.
- [10] V. Semenets, "Technical aspects for development laboratory base for learning FPGA and microcontroller systems.", in 10th International Conference The Experience of Designing and Application of CAD Systems in Microelectronics, Lviv-Polyana, Ukraine, 2009, p. 145.
- [11] Oleg Zubkov, Iryna Svyd, Oleksandr Maltsev, Liliia Saikivska. Incircuit Signal Analysis in the Development of Digital Devices in Vivado 2018. // First International Scientific and Practical Conference «Theoretical and Applied Aspects of Device Development on Microcontrollers and FPGAs» MC&FPGA-2019, Kharkiv, Ukraine, July 26-27, 2019. – Kharkiv: 2019. – P. 12-13. DOI: 10.35598/mcfpga.2019.003
- [12] V. Semenets, V. Levikin and V. Sayenko, "Research and analysis of the didactic policy of the university in the training of specialists in information technology", Automated control systems and devices, vol. 175, pp. 4-14, 2018.
- [13] O. Avrunin, O. Kruk, T. Nosova and V. Semenets, "Technical aspects of the development of virtual laboratory works on technical educational disciplines", Open Education, vol. 3, pp. 11-17, 2008.
- [14] V. Kobzev, V. Semenets and V. Filatov, "Components of the information system for monitoring the quality of education in Kharkov National University of Radio Electronics", in 7th Int. scientific and technical conf. Information systems and technologies (IST-2018), Kharkiv-Koblevo, 2018, pp. 51-54.
- [15] O. Avrunin, S. Sakalo and V. Semenetc, "Development of up-to-date laboratory base for microprocessor systems investigation", in 19th International Crimean Conference Microwave and Telecommunication Technology CriMiCo - 2009, Sevastopol, Ukraine, 2019, pp. 301-302.

Creation Features of Devices for Testing Nasal Breathing

Yana Nosova ORCID 0000-0003-4310-5833 Department of Biomedical Engineering Kharkiv National University of Radio Electronics Kharkiv, Ukraine yana.nosova@nure.ua

Ibrahim Younouss Abdelhamid ORCID 0000-0003-2611-2417 Department of Biomedical Engineering Kharkiv National University of Radio Electronics Kharkiv, Ukraine ibrahim.younouss.abdelhamid@nure.ua Maksym Tymkovych ORCID 0000-0001-5613-1104 Department of Biomedical Engineering Kharkiv National University of Radio Electronics Kharkiv, Ukraine oleh.avrunin@nure.ua

Oleg Avrunin ORCID 0000-0002-6312-687X Department of Biomedical Engineering Kharkiv National University of Radio Electronics Kharkiv, Ukraine maksymtymkovych@nure.ua

Abstract—The article is devoted to the questions of metrological certification of tests of the device of rhinomanometry type PRX. The main stages of the methodology of metrological certification, as well as design and technological aspects in the development of rhinomanometers with a measuring unit are described.

Keywords—respiratory, rhinomanometry, pressure drop, nasal breathing

I. INTRODUCTION

In Ukraine, protecting public health is one of the most important state tasks [1, 2] aimed at organizing and increasing the production of domestic medical equipment, improving the quality of medical care, and introducing standards for the provision of medical care based on the principles of evidence-based medicine.

However, the creation of an effective system of diagnostic and therapeutic measures in Ukrainian clinics is hampered by the insufficient provision of medical facilities with modern medical equipment, since up to 70% of the medical equipment used is physically worn out, morally obsolete and needs to be replaced [2].

At the same time, the needs for medical equipment are met at the expense of domestic manufacturers by no more than 30% [2]. It follows that the use of scientific and technological potential to increase the range of domestic medical equipment products, the ability to compete in both domestic and foreign markets, is a strategic task for Ukrainian medical instrument making.

Relevance and purpose of research.

Recently, there has been a significant increase in the prevalence of upper respiratory tract diseases [3]. However, in Ukraine, in clinical practice, instrumental methods for examining the respiratory function of the upper respiratory tract and the corresponding rhinomanometry devices are rarely used. The rhinomanometry method involves Sofia Khudaieva ORCID 0000-0002-1247-5279 Department of Biomedical Engineering Kharkiv National University of Radio Electronics Kharkiv, Ukraine sofia.khudaieva@nure.ua

Birgit Glasmacher ORCID 0000-0002-2452-1666 Institute for Multiphase Processes Leibniz University of Hannover Hannover, Germany secretariat@imp.uni-hannover.de

measuring the pressure drop across the nasal passages and the corresponding air flow during breathing to determine the value of the aerodynamic drag coefficient [4].

Currently, there are only a few rhinomanometer models on the market of medical respiratory equipment, the main of which are ATMOS 200 and ATMOS 300 (ATMOS Medical system GMB, Germany) [4, 5] and their analogues, for example, Rinolan rhinomanometer from Mitsar (RF, St. Petersburg). All of the above rhinomanometers are based on the method of anterior active rhinomanometry, which, according to the developers, is the least uncomfortable for the patient, but has limited diagnostic capabilities.

Therefore, it is relevant to create domestic rhinomanometric equipment that allows expanding diagnostic capabilities and increasing the reliability of the measured indices of nasal breathing, as well as the development of metrological certification and verification methods for both newly created and existing devices.

Formulation of the problem.

The object of the test is an experimental model of a device developed at KHNURE for determining the differential flow rate characteristics (PRX) in low pressure air ducts, which is part of the KRM computer rhinomanometry for testing nasal breathing of the TNDA of the PRX type. A detailed description of the structural diagram and design of the PRX device is given in [4, 6]. It consists of: a measuring unit containing pressure and air flow sensors, the signals from which are transmitted to the converter unit, in which the output signals of the sensors are digitized using an analog-to-digital converter and transferred via USB to a personal computer of the PC in which high-level signal processing, visualization, analysis and recording of measurement results.

The justification of the diagnostic indicators of the rhinomanometry method is given in [4], therefore, further we consider only the numerical values of the parameters of the measured quantities and the basic medical and technical requirements:

- the maximum pressure drop in the nasal passages can reach values up to 40 kPa;

- the maximum air flow during breathing in the inspiration cycle according to spirometry is up to 81/s [2];

- the measurement range of auxiliary sensors that determine the pressure drop in the submask space during inhalation and exhalation can be selected on the basis of the assumption that the aerodynamic resistance of the inlet breathing equipment (mask and connecting hoses) is not less than an order of magnitude lower than the aerodynamic resistance of the respiratory tract, which is confirmed experimentally [4, 6];

- when choosing analog sensors, it is necessary to take into account that the error of most standard primary transducers used in medical equipment for breathing diagnostics is about 5%, and the quantization step when digitizing an analog signal should be less than 10% of the measurement error. Therefore, the quantization step should not exceed 0.5% of the maximum signal value, which corresponds to 256 levels of an 8-bit ADC;

- given that the duration of the breathing cycle can be from 0.5 to 10 s [2, 4, 8], as well as the possibility of conducting examinations in dynamic mode when studying the relatively high-frequency components (up to tens of Hz) of the air flow signal in diagnosing the function of the nasal valve [8], it is necessary, accordingly with the sampling theorem, to select the sampling frequency of the measuring signals of the order of hundreds of Hz;

- also one of the main requirements for widespread use of the device in clinical practice is the simplicity of performing preparatory procedures by medical personnel (sterilization, adjustment, calibration) and the examination itself (selection of measurement modes, data analysis and visualization).

II. THE MAIN STAGES OF THE METHODOLOGY OF METROLOGICAL CERTIFICATION

The tests were carried out on a measuring installation, the combined circuit of which is shown in Fig. 1. Structurally, the PRX device consists of a RA flow meter, which is installed in the VT air duct, a BPD pressure transducer block, an ADC analog-to-digital converter module, a USB interface, and a personal computer.

In the body of the flowmeter there is an internal cylindrical diffuser with an expansion of diameters towards the source of air consumption (a Ventury nozzle is used as the basis of the principle of the flowmeter operation). An adapter with a KO non-return valve and a pressure test point for pressure transducer is attached to the flowmeter body. A mask with an inlet channel B for the passage of inhaled and exhaled air and a channel G in the form of a flexible sleeve RD2, which enters the inside of the mask and serves to communicate with the patient's mouth by holding the tip of the sleeve with lips, is mounted to the outlet of the adapter (it is advisable to use a rigid plastic mouthpiece to exclude the possibility of clamping lips or teeth of a flexible sleeve).

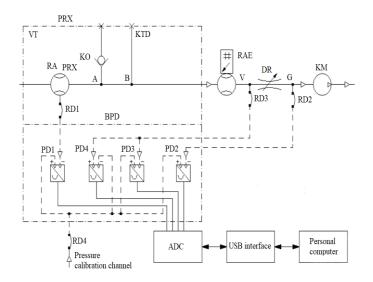


Fig. 1. Combined bench setup for metrological certification of PRX device.

The BPD unit contains pressure transducers PD1 – PD4 with electrical connectors and flexible hoses for communicating pressure transducers with a flowmeter RA (RD1) and an oral cavity G (RD2 and RD3). The flexible sleeve RD4 is used for simultaneous testing (verification) of pressure transducers PD1 – PD4. Pressure measurement is performed at the following points: PD1 – pressure (vacuum) in the flowmeter RA; PD2 – pressure (discharge) in the patient's oral cavity (at point G) behind the nasal passages (chokes DR1 and DR2); PD3 – pressure (vacuum) at the entrance to the mask (channel B); PD4 – overpressure at the outlet of the mask (channel B).

The KO non-return valve, connected at point A, serves to limit the excess pressure in the exhalation cycle in order to avoid damage to the PD1 – PD4 transducers and prevents the mask from detaching from the patient's face due to the high aerodynamic resistance of the Ventury nozzle. The pressure test point B of the CTD is used to connect an additional pressure transmitter (if necessary).

Thus, when testing a patient, the air flow inhaled through the nose and the pressure drop at the resistances DR1 and DR2 (simultaneously on two nasal passages or alternately) are determined. Processing of the test results is carried out by constructing a graphical dependence of the differential pressure on the flow rate and calculating the ratio of the differential pressure to flow rate and air flow rate. In the reverse flow of air (expiration), only overpressure (measured by the transducer) is subject to control PD4) to indicate the phase of expiration. It should be noted that when using a non-return valve, the readings of the PD4 sensor do not exceed 100 Pa.

The measurement setup diagram also shows: an air flow source (KM compressor), an adjustable choke DR to create resistance, and a RAE reference flowmeter with an electrical analog output signal. To create a stable airflow when purging a PRX device, a flow source with a power of about 1600 W is required.

The use of a calibration (reference) RAE flow meter makes it possible to assess the accuracy of the data measured by the PRX device and, if necessary, to adjust the value of the flow coefficient in order to minimize the error. During the tests, the standard of the Caliber unit of flow and the Artwik MC2-R pressure calibrator (ZAO Radian, RF) were used.

The PRX device performs the following functions:

- simultaneous control of pressure drop and flow in the test channel;

- processing the test results by constructing a graphical dependence of the differential pressure on the flow rate and calculating the ratio of the differential pressure to flow rate and air flow rate.

III. DESIGN AND TECHNOLOGICAL ASPECTS IN THE DEVELOPMENT OF RHINOMANOMETERS WITH A MEASURING UNIT LIKE PRX

The technical implementation of the KRM computer rhinomanometry provides for the selection and coordination of the hardware included in the measuring, converting and interface modules, the development of the device design, as well as the creation of the corresponding control software. The main technical requirements when choosing sensors for the TNDA PRX computer rhinomanometry are: high sensitivity, lack of hysteresis, linearity, stability, the least influence external factors; simplicity of and manufacturability of the design, the possibility of interchangeability and sanitization. Based on this, it is advisable to choose analog tensor-resistive differential sensors of Motorola Freescale Semiconductor MPX5010DP [6] as pressure sensors PD1 - PD4, designed to measure small pressure drops, including in medical applications, and having a built-in amplifier that allows connecting their conclusions, directly to the ADC signal inputs.

It is advisable to implement the converter unit on the basis of the L – Card E14–140 multichannel specialized measuring module, the main components of which are the 14-bit LTC1416 analog-to-digital converter (ADC), the AVR AtMega8515 microcontroller and the PDIUSB12D interface module for interaction with a PC via a USB port.

The functions of the last two modules can also be realized using a high-speed 32-bit ARM processor. The digitized signals from pressure and flow sensors with a sampling frequency of 500 Hz are transmitted via a USB interface to a PC for further processing and analysis.

The ADC quantization step is about 0.6 Pa for sensors with a measurement limit of 10 kPa, which is two orders of magnitude higher than the allowable limit (10%) of the maximum error (5%) of primary measurements converters, which for used sensors is 250 Pa.

Considering the small load on the data transfer channel and the relatively small amount of stored information, double-byte values from four sensors (three pressure sensors and an air flow sensor) with a frequency of 500 Hz, the data transfer speed on the interface will be about 4 kB / s (32 kB / s). Therefore, for communication with a PC, it is advisable to use the USB-2.0 interface in the Low-speed data transfer mode with a data exchange rate range of 10 - 1500 Kbit / s.

The theoretical justification for the use of a Venturi nozzle with a quadratic functional dependence of the pressure drop on the flow rate [6, 7] is the presence of

turbulent regime of air flow in the nasal cavity, which is confirmed by the data of most studies [2 - 6].

In fig. 2 shows a semi-structural flowmeter based on a Venturi nozzle, where a hole 2 with a diameter d is made in the housing 1, in which a pressure differential is measured using a hole 3 and a pressure transducer PD1 of a differential type with an analog output.

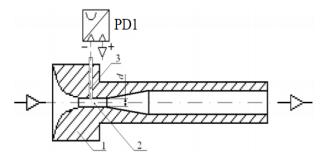


Fig. 2. Semi-constructive flowmeter based on a Ventury nozzle.

The message of the tube 3 with the input channel (receiver) "-" in the PD1 converter corresponds to the measurement of vacuum (vacuum) in the pipeline, and the + channel, measuring atmospheric pressure, allows you to obtain the pressure drop between the input channels. The technologically accurate design of the Venturi nozzle (according to GOST 10921 [7]) is advisable to implement on an automated machine with numerical control for all three sizes.

To increase the accuracy of measurements, it is advisable for patients with different physical abilities to provide Ventury nozzles with different diameters of the inlet openings (7 mm, 8 mm and 9 mm), respectively for small (up to 4 hp), medium (up to 61/s) and large (up to 81/s) air flow during inspiration (see Fig. 3, a). Pre-calibration of PD1 ... PD4 sensors is carried out using a cup water pressure gauge (see Fig. 3, b), after exposure of the PRX-device to the room for 15 minutes.

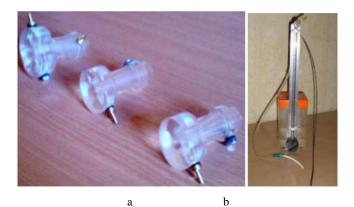


Fig. 3. Type of individual structural elements of the TNDA-PRX device:a Venturi nozzles for different diameters of the inlets, b - adjustment water manometer.

The main requirements for the software are: the ability to implement algorithms for statistical processing of data to increase the repeatability of survey results by analyzing a dynamic measurement model, conducting automated

processing of diagnostic indicators with the possibility of flexible software changes by the developer to improve diagnostic algorithms, the simplicity of calibration procedures for sensors and monitoring of measured values, as well as protection against unauthorized access.

IV. CONCLUTION

A methodology has been developed for metrological certification of a PRX device (determination of differential flow characteristics) as an individual measuring instrument included in the TND-PRX type computer rhinometery. According to the results of the metrological certification of the PRX device, it was found that the error in determining the measured parameters (air flow and pressure drops) is not more than 5% (certificate of state metrological certification No. 05-0102 of 01.04.2010), which allowed for preliminary clinical testing of the device and is the first step for its certification as a medical device.

To ensure flow measurement in the full range of pressure changes of the PD1 transducer and to increase the accuracy of measurements, the PRX device is equipped with RA flow meters with three nominal nozzle diameters - 7; 8 and 9 mm. In this case, the maximum values of the relative error in measuring the air flow do not exceed 4.9 in absolute value; 3.9 and 3.1% for Ventury nozzles with diameters of 7; 8 and 9 mm, respectively, and when measuring pressure, the maximum relative error in absolute value was 3.5%.

The prospect of this work is to study the influence of individual characteristics of the patient's breathing on the diagnostic results and to improve the dynamic model for analyzing rhinomanometry data.

ACKNOWLEDGMENT

The exchange program with East European Countries funded by DAAD (Ostpartnerschaften, project number 54364768) and joint Ukraine-Germany project MESU-BMBF 2019-2020 "3D-Model – Implementation of rapid prototyping to design and model the upper respiratory tract in normal and typical pathologies"

REFERENCES

- Nosova, Ya V., Kh I. Faruk, and O. G. Avrunin. "A tool for researching respiratory and olfaction disorders." Telecommunications and Radio Engineering 77.15 (2018): 1389-1395.
- [2] Nosova, Y., I. Younouss Abdelhamid, and O. Gryshkov. "Using 3D printing technology to full-scale simulation of the upper respiratory tract." Informatyka, Automatyka, Pomiary W Gospodarce I Ochronie Środowiska, Vol. 9, no. 4, Dec. 2019, pp. 60-63, doi:10.35784 / iapgos.681.
- [3] Al_Omari, Ahmad Khaleed, Husham Farouk Ismail Saied, and Olig Grigorovitsh Avrunin. "Analysis of Changes of the Hydraulic

Diameter and Determination of the Air Flow Modes in the Nasal Cavity." *Image Processing and Communications Challenges 3*. Springer, Berlin, Heidelberg, 2011. 303-310.

- [4] Fyrmpas, Georgios, et al. "The value of bilateral simultaneous nasal spirometry in the assessment of patients undergoing septoplasty." *Rhinology* 49.3 (2011): 297.
- [5] Saied, Husham Farouk Ismail, Ahmad Khaleed Al_Omari, and Olig Grigorovitsh Avrunin. "An Attempt of the Determination of Aerodynamic Characteristics of Nasal Airways." *Image Processing* and Communications Challenges 3. Springer, Berlin, Heidelberg, 2011. 311-322.
- [6] Zhang, G. H., et al. "Correlation between subjective assessment and objective measurement of nasal obstruction." *Zhonghua er bi yan hou tou Jing wai ke za zhi= Chinese Journal of Otorhinolaryngology Head and Neck Surgery* 43.7 (2008): 484-489.
- [7] Tingelhoff, Kathrin, et al. "Comparison between manual and semiautomatic segmentation of nasal cavity and paranasal sinuses from CT images." 2007 29th Annual International Conference of the IEEE Engineering in Medicine and Biology Society. IEEE, 2007.
- [8] Vogt, Klaus, et al. "4-Phase-Rhinomanometry (4PR)--basics and practice 2010." *Rhinology. Supplement* 21 (2010): 1-50.
- [9] Zambetti, G., et al. "Study and application of a mathematical model for the provisional assessment of areas and nasal resistance, obtained using acoustic rhinometry and active anterior rhinomanometry." *Clinical Otolaryngology & Allied Sciences* 26.4 (2001): 286-293.
- [10] Zhang, Gehua, et al. "Nasal airway volume and resistance to airflow." American journal of rhinology 22.4 (2008): 371-375.
- [11] Ismail, Husham Farouk, et al. "The role of paranasal sinuses in the aerodynamics of the nasal cavities." *International Journal of Life Science and Medical Research* 2.3 (2012): 52-55.
- [12] Avrunin, Oleg G., et al. "Study of the air flow mode in the nasal cavity during a forced breath." *Photonics Applications in Astronomy, Communications, Industry, and High Energy Physics Experiments* 2017. Vol. 10445. International Society for Optics and Photonics, 2017.
- [13] Farouk, H., and O. Avrunin. "Comparison Discriminate Characteristics Between Modern TNDA-PRH Rhinomanometer And Previously Methodology." *International Journal of General Engineering and Technology (IJGET) ISSN* (2013): 2278-9928.
- [14] SHELTON, DIANA M., and NOEMI M. EISER. "Evaluation of active anterior and posterior rhinomanometry in normal subjects." *Clinical Otolaryngology & Allied Sciences* 17.2 (1992): 178-182.
- [15] Toh, Song-Tar, Cheng-Hui Lin, and Christian Guilleminault. "Usage of four-phase high-resolution rhinomanometry and measurement of nasal resistance in sleep-disordered breathing." *The Laryngoscope* 122.10 (2012): 2343-2349.
- [16] Nosova, Yana, et al. "The use of statistical characteristics of measured signals to increasing the reliability of the rhinomanometric diagnosis." *Photonics Applications in Astronomy, Communications, Industry, and High-Energy Physics Experiments 2016.* Vol. 10031. International Society for Optics and Photonics, 2016.
- [17] Avrunin, Oleg G., et al. "Principles of computer planning in the functional nasal surgery." *Przegląd Elektrotechniczny* 93.3 (2017): 140-143.
- [18] Nosova, Yana, Oleg Avrunin, and Valery Semenets. "Biotechnical system for integrated olfactometry diagnostics." Innovative technologies and scientific solutions for industries 1 (1) (2017): 64-68.

Remote Debugging of Embedded Systems in STM32CubeMonitor

Oleksandr Velihorskyi ORCID 0000-0002-8256-7339 Biomedical radioelectronic apparatus and system department Chernihiv National University of Technology Chernihiv, Ukraine oleksandr.veligorsky@inel.stu.cn.ua Ihor Nesterov

Master student, "Telecommunications and radiotechnics" programme *Chernihiv National University of Technology* Chernihiv, Ukraine ihor.nesterov@inel.stu.cn.ua

Abstract—Debugging of embedded systems is one of the most important parts of firmware development. Real-time trace debugging by means of special software and hardware provides the best way to debug the firmware on real equipment. New challenges in higher education, caused by COVID-19 pandemic, require new approaches in courses, oriented on embedded system development. The paper is devoted to experience of STM32CubeMonitor implementation for remote debugging of STM32-based MCU boards during the quarantine and distance learning process, caused by COVID-19 pandemic.

Keywords—embedded systems, microcontroller, debug, firmware.

I. INTRODUCTION

Debugging of embedded software is one of essential part of radioelectronic devices and systems development. As it pointed in [1], process workflow of embedded software development consists of the next steps: business modelling, requirements, analysis and design, implementation, test and deployment. Debugging is a part of implementation and test parts, when the developer writing the code for microcontroller or signal processor, flashing the device, observing and analyzing the implementation. Various debugging techniques can be used in embedded systems [2], such as traditional (print method, run-time methods), as well as integration testing techniques. Such classic debugging techniques is based on breakpoints, observing of variables, debugging some functions, etc. Any IDE (Keil, Atollic TrueStudio, STM32Cube IDE) has their own functionality to provide debug: variables window, breakpoints (including conditional breakpoints), etc. Another powerful method is used for final tests - so called real-time trace debugging, when special additional software (e.g. Percepio Tracealyzer [3] for RTOS- or Linux-based systems), or hardware (e.g. PCAN-USB for tracing of CAN interfaces in embedded systems [4]) is used. It should be noted, that usually debugging data performed in digital format as numbers or strings (such as variable values, data packages values, etc.), so it is not so easy to track and visualize changes of data.

To provide unique debugging functions, usually, developer should design his own application (running on Windows on other operation system) that will visualize necessary data in convenient form, like flowcharts, graphs, gauges, etc. In this case, such additional work requests Maksym Khomenko ORCID 0000-0001-9084-3527 Biomedical radioelectronic apparatus and system department Chernihiv National University of Technology Chernihiv, Ukraine mr.homax@gmail.com

additional time. Moreover, any changes in data format require significant changes in designed application (including compiling, building, etc.). Taking into account the increasing complexity of debugging, some MCU and IDE vendors has already launched additional development tools, aimed to help with complex debug of firmware. One of the first such debugging tools was STM Studio [6] that helps real-time monitoring and visualizing of variables. Unfortunately, this tool has status "NRND – Not recommended for new design" now, but, STM has released a new, more powerful tools family, that will replace STM Studio - STM32CubeMonitor [5]. This paper describes the functionality and the practical experience of using the STM32CubeMonitor in remote Microcontrollers and Embedded Systems Lab on Biomedical radioelectronic and system (BRAS) department of Chernihiv National University of Technology (CNUT).

II. STM32CUBEMONITOR

A. Family of STM32CubeMonitor tools

The STM32CubeMonitor family helps in debugging of embedded software, developed for STM32 microcontrollers [5]. The tools provide real-time reading and visualization of any variables, including remote data. The family consist of the next tools:

- STM32CmonPwr monitoring on PC power data (currents, voltages and powers) from special X-Nucleo board;
- STM32CmonRF monitoring RF performance of STM32-based hardware devices, such as Bluetooth Low Energy and 802.15.4 integrated RF transceivers;
- STM32CMonUCPD monitoring and configuring of USB Type-C and Power Delivery applications for STM32 microcontrollers;
- STM32CubeMonitor monitoring and visualization of data on Linux, Mac and Windows for STM32 microcontrollers.

In other words, all family consists of specialized tools (power monitor, RF monitor, power delivery monitor), and versatile Cube monitor, that should be used in all other cases.

All mentioned above STM32 debugging tools are free of charge after the authorization on STM web-portal.

STM32CubeMonitor is based on open-source Node-RED [7], flow-based programming tool, oriented on collaboration of Internet of Things devices that has a huge variety of additional modules and strong user's community.

B. Configuration of STM32CubeMonitor

STM32CubeMonitor has two main windows – flowchart, containing all nodes for data acquisition, processing and visualization, and dashboard, where user can see all the data during the debug procedure. Examples of flowchart and dashboard are shown on Fig. 1 and Fig. 2, respectively. To add necessary nodes to the flowchart, the left, so called,

"nodes" panel should be used (Fig 3). The most important nodes for connection with microcontrollers are collected in group "ST Microelectronics": *acq in* and *acq out* – for receiving and transmitting the data from MCU. Debugger (e.g. ST-Link) should be selected in properties of these nodes for proper connection with target MCU. *Variables* node is used to select the variables or controller registers that will be used to visualize data or control in STM32CubeMonitor. It should be noted, that all data exchange is provided through *elf* or *axf* file (depends on used IDE), that have to be selected in properties window ("executable" field). Data from the board can be collected as fast as possible, or with some sampling frequency, continuously or starting from some trigger point. All these parameters can be configured in properties window of *variables* node.

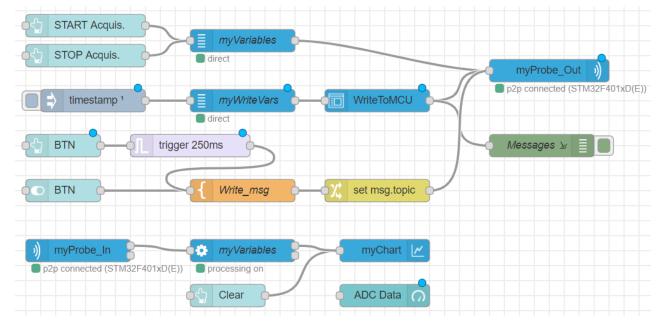


Fig. 1. Example of flowchart diagram in STM32CubeMonitor

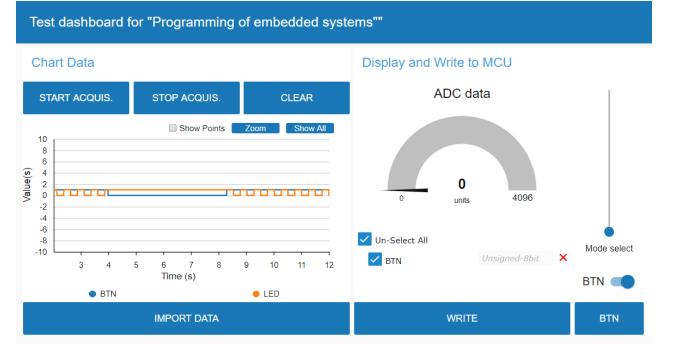


Fig. 2. Dashboard view in STM32CubeMonitor

II International Scientific and Practical Conference Theoretical and Applied Aspects of Device Development on Microcontrollers and FPGAs

MC&FPGA-2020

Starting point of data collection from MCU can be also set by using buttons that will send so called "topic" *start* or *stop* (you can see it in the top left corner on Fig.1 and Fig. 2). Another key topic – *clear* can be used to clear the data on chart. *Processing* node is used for separation of variables to duplets (x and y, for representing time-based charts) and further post-processing (e.g. mathematical calculations, statistical or logical expressions with data). To show the data from MCU various nodes can be used, e.g. *Gauges, Charts, Numeric* or *Text* windows. These nodes are collected in "dashboard" group in node panel.



Fig. 3. Node panel in STM32CubeMonitor

One of the most important parts of debugging is external events. As it was described above, classical debugging methods, implemented in IDE has a lot of limitations for external events, so, STM32CubeMonitor provide for developers many useful nodes, such as *button, switch, slider, numeric, text input, template* and *write panel* (Fig. 3). The easiest way to send the data from CubeMonitor to MCU is *write panel*. As it shown on Fig. 1, series connection of nodes *variables, write panel* and *acq out* guaranteed sending some variables from input fields (listed in the *MyNameVars* node) to MCU. The limitation of that way is all variables are represented in *Write panel* as text input fields. It is ok for text or numerical data, but not so good for Boolean data (e.g. buttons, switches, etc.).

To avoid this limitation a series connection of *Button* (or *Switch*), *Template* and *Change* nodes can be used (nodes *BTN*, *Write_msg* and *set.msg_topic* in the center of Fig. 1). The main part is template node, where JSON template should

be written, including address of the variable (all addresses of variables can be found in the "executable" field of the *Variables* node), and type (data type, e.g. $1 - \text{uint8}_t$, etc.). It should be noted, that implementation of *Button* node for sending the state to MCU requires additional trigger (violet block n Fig. 1), ensures resetting the button state to previous value with some delay (e.g. 250 ms). Unfortunately, "long press" can't be simulated in the current version of STM32CubeMonitor, so *Switch* node will be preferable for such cases.

After the connection of nodes in flowchart mode, user should distribute all widgets (nodes, represented in dashboard section of node panel - Fig. 3) on the dashboard (Fig. 2). "Dashboard - Layout - Layout" command should be used to organize all widgets on dashboard (Fig. 5). In such mode, size and sequence of widgets can be changed. User can also add groups (block, includes similar widgets, e.g. for visualization of data, or for writing data to MCU), tabs (separated dashboard that can be switched by clicking on Tab header), etc. To start the data acquisition, user should check the connection on flowchart (green marks "p2p connected", "direct"), "processing on", then press "Deploy", "Dashboard" buttons, and then "Start acquisition" in Dashboard window (Fig. 2). It should be noted, that in case of control from STM32CubeMonitor, debug in IDE will not works. Any other connection will lead to disconnection of STM32CubeMonitor (green marks will be replaced by red with error messages), but, user can set "shared mode" (based on TCP protocol instead of default p2p), providing debugging simultaneously in IDE and STM32CubeMonitor [8]. The only one drawback of such connection is lower rate of data acquisition.

In case, when project was changed, *elf* or *axf file* should be updated in *acq in* and *acq out* nodes. Otherwise, linking of variables and their addresses will be lost.

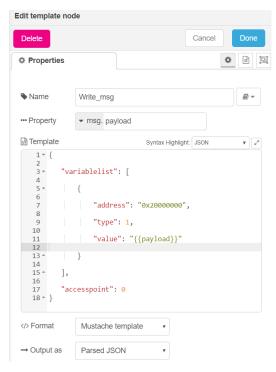


Fig. 4. Node panel in STM32CubeMonitor

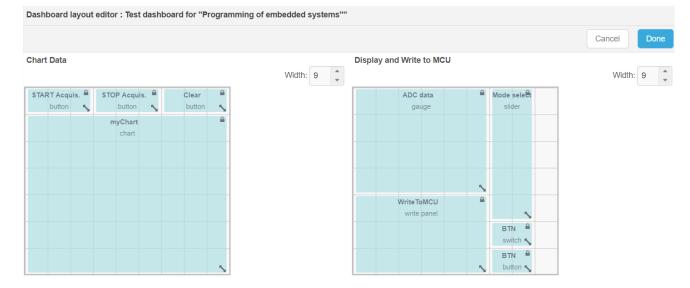


Fig. 5. Layout editor for dashboard in STM32CubeMonitor

III. IMPLEMENTATION OF STM32CUBEMONITOR IN REMOTE MICROCONTROLERS AND EMBEDDED SYSTEMS LAB

COVID-19 pandemic and quarantine has significantly impacted on higher educational institutions all over the world. To respond to COVID-19 challenges, universities deployed various distance learning technologies, including videoconferences, video lectures, course management systems for distance learning, etc. On master-level program "Telecommunications educational and radiotechnics" in CNUT BRAS department lectures was took place in YouTube streams and Zoom videoconferences modes. Meanwhile, one of the toughest challenges was providing for students all practical-oriented competences and learning outcomes, planned in educational program. To reach planned learning outcomes, on some courses lab equipment was temporarily lent to applicants for higher education during the quarantine, e.g. single-board PCs Raspberry Pi (course «Architecture of modern processors»). Taking into account that STM32 Nucleo boards in spring semester using in different courses for master and bachelor students, it was not possible to distribute these boards. So, taking into account the previous experience of collaboration between CNUT and Bonn-Rhein-Sieg University of Applied Sciences on remote lab [9], it was decided to establish Microcontroller and embedded system remote lab on BRAS department, with PCs, digital multifunctional equipped USBoscilloscopes ISDS205X (also includes DDS function signal generator and logic analyzer) and STM32 Nucleo development boards. To use this equipment remotely, TeamViewer software was used. Taking into account that PCs in this lab as of now doesn't have a static IP address, it is not possible switch on and switch off them remotely, and head of lab should switch on and off them manually.

One of the essential parts of the remote lab is STM32CubeMonitor, because remote operation doesn't provide possibility to use the input elements: toggle switches, press buttons, etc., whereas change of corresponding MCU registers not so convenient in IDE. So, STM32CubeMonitor was used to monitor the variables values, as well as for emulation of input elements. To provide full functionality of Remote lab from the starting of 2020-21 studying year, a new equipment based on STM32H7 MCUs was installed (with support of AgileVision.Io), and development of dashboards for all laboratory works is in the progress.

ACKNOWLEDGMENT

This work and establishing of remote Microcontrollers and Embedded Systems Lab on BRAS department was supported by company AgileVision.Io, one of the stakeholders of "Telecommunications and radiotechnics" master program in Chernihiv National University of Technology.

REFERENCES

- T Punkka, "Agile methods and Firmware Development," SoberIT 2005, pp.1-21. http://www.ngware.eu/blog/papers/agile_firmware_punkka_V103.pdf
- [2] Top Debugging Techniques Used In Embedded Systems, <u>https://www.totalphase.com/blog/2020/03/top-debugging-techniques-used-in-embedded-systems/.</u>
- [3] Percepio Tracealyzer https://percepio.com/tracealyzer/.
- [4] PCAN-USB. CAN Interface for USB <u>https://www.peak-system.com/PCAN-USB.199.0.html?&L=1</u>.
- [5] STM32CubeMonitor <u>https://www.st.com/en/development-tools/stm32cubemonitor.html</u>.
- [6] STM-STUDIO-STM32 <u>https://my.st.com/content/my_st_com/en/products/development-tools/software-development-tools/stm32-software-development-tools/stm32-performance-and-debuggers/stm-studio-stm32.html.</u>
- [7] Node-RED. Low-code programming for event-driven applications https://nodered.org/.
- [8] How to configure shared mode <u>https://wiki.st.com/stm32mcu/wiki/STM32CubeMonitor:How_to_con_figure_shared_mode.</u>
- [9] K. Pretz, "German University Opens Up Its Hands-on Remote FPGA Lab During the Coronavirus Pandemic," https://spectrum.ieee.org/news-from-around-ieee/the-institute/ieeemember-news/german-university-opens-up-its-handson-remote-fpgalab-during-the-coronavirus-pandemic.



The Use of Percepio Tracealyzer for the Development of FreeRTOS-based Applications

Maksym Khomenko ORCID 0000-0001-9084-3527 EMT Department Bonn-Rhein-Sieg University of Applied Sciences Sankt-Augustin, Germany maksym.khomenko@h-brs.de

Abstract—This paper discusses some problems of development and testing of FreeRTOS-based application. The use of Tracealyzer software tool is proposed to make this process more convenient. The benefits of such usage have been shown on typical issues that can be met in development and debug phase.

Keywords—microcontroller, RTOS, debug, embedded system, tracealyzer.

I. INTRODUCTION

Microcontrollers play a key role in the majority of nowadays embedded systems. Among the variety of 8-, 16and 32-bit microcontrollers the last ones (which mostly have an ARM core) take a dominant position in the embedded world [1]. They usually have more memory, different peripheral modules and of course higher frequencies and computational power compared to 8- and 16-bit microcontrollers for the reasonable price. The software of embedded systems also becomes more complex and often utilizes real time operational system (RTOS) such as FreeRTOS [1, 2] to gain flexibility and multitasking. However the development, test and debug of RTOS-based programs brings a new challenges to the software design Some of these challenges are task engineers. synchronization, resources sharing between tasks, task priority management and other.

Helping engineers to make the development and debug process less problematic Swedish company Percepio have developed software tool Percepio Tracealyzer. This tool together with library which should be linked with FreeRTOS-based program, visualize all the objects and events inside operational system that makes understanding of program flow and debug process easier and convenient

II. TRACEALYZER MAIN CONCEPTS

The tool consists of two separate parts as it is mentioned above: the trace recorder C library and main program with graphical user interface. The library is to be compiled with user FreeRTOS-based program for the target platform. It includes three configuration header files (*trcConfig.h*, *trcSnapshotConfig.h* and *trcStreamingConfig.h*) that can be used to set up one of two recorder mods of operation and various parameters of data tracing. One mode of operation is called "Streaming" in this mode the data collection and visualization is performed in real time. Collected data are constantly transmitted to the computer for the visualization Oleksandr Velihorskyi ORCID 0000-0002-8256-7339 Biomedical radioelectronic apparatus and system department Chernihiv National University of Technology Chernihiv, Ukraine oleksandr.veligorsky@inel.stu.cn.ua

through some communication interface (USB or Ethernet) or through hardware debugger (not all debuggers are supported). Another mode of operation is called "Snapshot" in this mode data are stored in the previously allocated (statically or dynamically) memory buffer on the target device and can be read to the computer trough any hardware debugger tool. The detailed description of how to include this library to custom FreeRTOS-based project and setup preferable tracing mode are given in [3].

The Tracealyzer itself is a powerful tool of RTOS data analysis. It contain huge batch of different views that can be open and allocated at the screen as part of main program or as separate window. So, the detailed description of all views can't be done in the scope of this paper. However most commonly used views are present in the Fig. 1.

Trace view (marked with a green frame in the Fig. 1) shows all tasks and RTOS events on the time line. It gives major information about system behavior. CPU load graph (marked with a yellow frame in the Fig. 1) represents information about CPU usage by different tasks in time. Selection details window (marked with a blue frame in the Fig. 1) shows some major parameters of the task slice or system event selected in the Trace view. Filter window (marked with a violet frame in the Fig. 1) can be used to enable or disable single objects or service events on other views of Tracealyzer. Such possibility makes inspection of the program flow more convenient because information that have no interest for the current analysis can be switch off. The brown frame in the Fig.1 shows different time related parameters of the tasks, the parameter of interest can be selected from the drop-down menu of this window (execution time parameter is selected in the Fig.1). Toolbar panel is placed on the left side of the main program window (red frame in the Fig. 1). It provides quick access to all other possible views of the program which also can be found in 'Views" menu. In addition, toolbar contains control buttons that are used to start/stop streaming in streaming mode and to make snapshot in snapshot mode.

Concerning selection of the operation mode is depend on the purpose of analysis. In development or in debugging phase for the easily reproduced bugs the snapshot mode can be used. Its main drawback is relatively short time period (usually some seconds) that can be stored due to device RAM limitation. On the other hand streaming mode of operation can be used when long time period should be

stored for analysis. Consequently this mode is useful for the

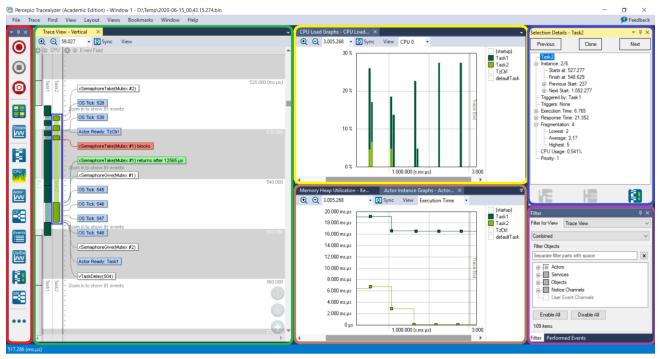


Fig. 1. Percepio Tracealyzer window layout

III. TRACEALYZER USE CASES

All use cases listed in this section utilize the Nucleo-F429 board (build on STM32F429 microcontroller) as a hardware base. Also all data traces have been taken in snapshot mode.

A. Periodicity of Task Execution

In RTOS-based programs most of the tasks do not need to run all the time. Usually they are triggered by other tasks and interrupts or use RTOS time management API functions to execute periodically and then go back to the blocked state till the next synchronization event. The demand of task execution period stability can be different for various tasks. For example, in control application the data sampling task should have low jitter to avoid system performance degradation [4].

FreeRTOS has two API functions to perform time delay: *vTaskDelay()* for the tasks where period jitter is not critical, *vTaskDelayUntil()* for the tasks with strict requirements to the period stability [2].

To compare the results of using different time delay API functions the test program was developed. It has two tasks one of which uses *vTaskDelay()* and other uses *vTaskDelayUntil()*. Both tasks have same time delay value (150 ms) and the same priority. The resulting periodicity of tasks execution is shown in the Fig. 2 (a). The first task shows stable period of execution as expected, while the second task has variations and shift in period due to use of simple *vTaskDelay()* API function which does not take in to account the time of task execution.

Fig. 2 (b) shows the results of the same program but with slightly changed conditions. Now the second task has priority higher than the first one. Despite the fact that the first task uses *vTaskDelayUntil()* function to provide a stable period it

suffer from period deviation at the times when it overlap with the second task having higher priority.

In the real system such inaccuracy in priority assignment can lead to the tricky bug in system behavior. But as it is shown in the Fig. 2 using Tracealyzer helps easily find this problem early in the development stage.

B. Mutual Execution Problems Accessing Shared Resources

debugging of randomly and rare appeared bugs.

In the multitasking system a special care should be taken when tasks want to access shared resources (this can be global variables, peripheral modules internal or external) to prevent simultaneous change of such resources from different tasks.

One of the commonly used approaches treating this issue in RTOS is to protect the access to shared resource with special mechanism called mutex (abbreviation of mutual execution). Each task before doing something with shared resource should take a mutex that protect this resource. If the mutex is successfully taken than task can access the resource but if not this means that some other task has already gain access to it and the first one should wait or skip the actions with such resource. When task finishes actions with shared resource it should give the mutex so that other tasks waiting for this resource can gain an access to it.

In the FreeRTOS mutex is a special type of binary semaphore therefore an API function for taken a mutex is *xSemaphoreTake()* and API function for given a mutex is *possibility* of so called "Deadlock". "Deadlock" occurs when two (or more) tasks can't continue execution because they are waiting for the resources held by each other. Fig. 3 illustrates such kind of situation that has occurred with two tasks and two mutexes.

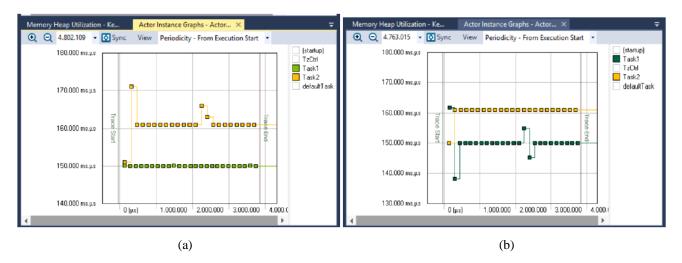


Fig. 2. Periodicity of tasks execution when tasks priority is equal (a) and when task1 has lower priority than task2 (b)

Test program showing this issue was developed. It consist of two tasks with equal priority that shares two resources global array and UART peripheral module and use two mutexes respectively. The first task 1 writes the message to the UART and fill global array with pseudo random numbers. The second task also writes the messages to the UART, and calculates the sum of array elements. At some point task 1 tries to get access to the UART while it is used by task 2. As the result the terminal stops displaying any messages (see Fig. 4). But what is the reason of such behaviour, how to find the roots of this problem? The Tracealyzer can help to find the solution.

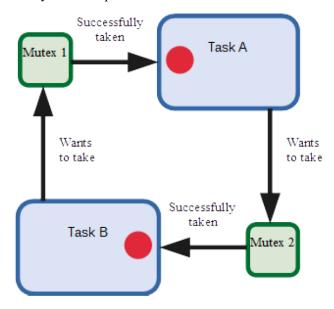


Fig. 3. Example of Deadlock situation with two tasks and two mutexes

From the trace view shown in the Fig. 5 can be clearly seen that both tasks stop the execution. Also there is shown "Mutex ownership diagram" next to the tasks on the trace view which were activated through "Intervals and State Machines" view by selecting diagrams of interest from the predefined ones. This diagrams shows that both mutexes are not free from the moment of tasks stop and till the end of trace. Global array access mutex is held by the first task while UART access mutex is held by the second task.

🎜 Terminal 🛛	🔗 Search	2	N	l ĝ			ß	٩	
Serial COM3 (22.06.20 12:47) ⊠									
time 0 Task1 in action									
time 1 Task	2 start calculating								
time 21 Tas	time 21 Task2 sum of array elements = 3170								
time 521 Task1 in action									
time 529 Task2 start calculating									
time 542 Task2 sum of array elements = 3175									
time 1042 T	ask1 in action								
time 1050 T	ask2 start calculating								

Fig. 4. UART messages from the test program in terminal window

Such analysis of system behaviour definitely shows that the "Deadlock" has occurred in the program. And now when the problem has been identified and localized it can be solved by the means of tasks logic reorganization in the part where they interact with mutexes getting access to shared resources.

IV. CONCLUSIONS

This paper discusses some issues that can be met by the embedded system developers dealing with the FreeRTOS and multitasking environment. The Tracealyzer software is proposed as useful tool that can make development and debug processes easier and faster. The benefits of this software tool have been proved on examples where it helps to figure out the problems with periodicity of task execution and "Deadlock" state of two tasks using shared resources and mutexes. As the result, Percepio Trasealyzer can be recommended to be used not only in development process but also in education courses for embedded system engineers.

REFERENCES

- [1] References"2019 Embedded Markets Study. Integrating IoT and Advanced Technology Designs, Application Development & Processing Environments.", Embedded.com, 2020. [Online]. Available: <u>https://www.embedded.com/wpcontent/uploads/2019/11/EETimes_Embedded_2019_Embedded_Markets_Study.pdf</u>. [Accessed: 20- Jun- 2020]
- [2] R. Barry, "Mastering the FreeRTOS™ Real Time Kernel A Hands-On Tutorial Guide", Freertos.org, 2020. [Online]. Available: <u>https://freertos.org/Documentation/161204_Mastering_the_FreeRTO</u>

II International Scientific and Practical Conference Theoretical and Applied Aspects of Device Development on Microcontrollers and FPGAs

MC&FPGA-2020

<u>S Real Time Kernel-A Hands-On Tutorial Guide.pdf</u>. [Accessed: 20- Jun- 2020].

- "Quick Start Guide Tracealyzer for FreeRTOS", Freertos.org, 2020.
 [Online]. Available: <u>https://percepio.com/gettingstarted-freertos/</u>.
 [Accessed: 20- Jun- 2020].
- [4] P. Marti, J.M. Fuertes, G. Fohler, K. Ramamritham, "Jitter compensation for real-time control systems", Proceedings 22nd IEEE Real-Time Systems Symposium (RTSS 2001), December 2001, pp 39-48.

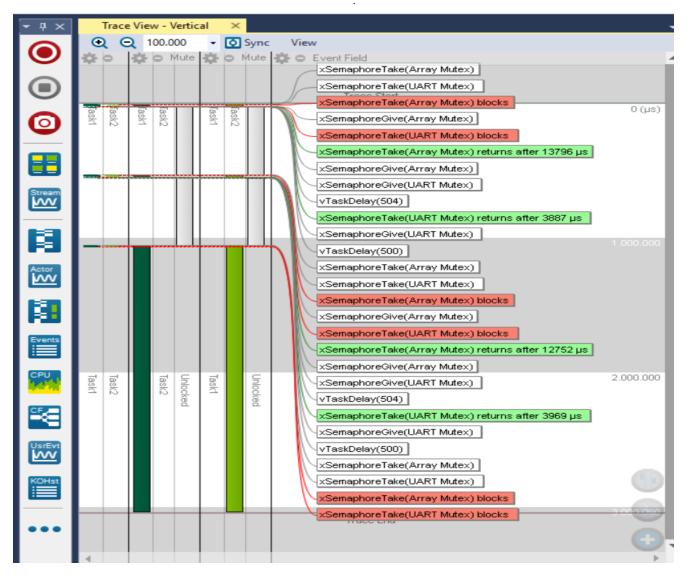


Fig. 5. Trace view of program with "Deadlock"

MC&FPGA-2020

Methods of Organizing Communication Between Microcontrollers in the System of Monitoring Energy Consumption

Sergiy Novoselov ORCID 0000-0002-3190-0592 Department of Computer-Integrated Technologies, Automation and Mechatronics Kharkiv National University of Radioelectronics Kharkiv, Ukraine sergiy.novoselov@nure.ua

Abstract—This paper discusses the principles of building networks based on modern LoRaWAN modems. The basics of implementation of data exchange in these networks are given. Experimental studies have been carried out which showed that in the case of "floating window" it is possible to increase the capacity of the network up to 10...15 packets per second without loss of data transmission speed.

Keywords—LoRaWAN modem, electricity accounting, automated control system, ASC, ASCAE

I. INTRODUCTION

Modern devices on microcontrollers are widely used in various spheres of human life. One of the promising areas of such equipment development is autonomous energy accounting systems. The use of microcontrollers combined with transmitters makes it possible to create built-in devices for monitoring energy consumption with low energy consumption from autonomous power sources. The solution of this problem is relevant for the construction of a distributed network of data collection from energy meters.

The paper proposes an analysis of different methods of communication between remote devices for guaranteed message delivery while using the minimum amount of energy consumed. The structure of the microcontroller tool for working with modern data transmission protocols in the LoRaWAN network is also considered.

II. STRUCTURE OF A MICROCONTROLLER DATA COLLECTION DEVICE FROM ENERGY METERING DEVICES

The network of energy metering devices includes the following types of devices: base module or gateway; wireless energy metering modules (meters); suitable sensors for measuring voltage, current, liquid flow, gas.

The block diagram of the basic module is shown in the Fig. 1. The main purpose of this module is the transmission of requests for energy meters to obtain from them data on the current state based on information from the sensor.

The base module is connected to the network, and then to a personal computer (control panel) through interface Oksana Sychova ORCID 0000-0002-0651-557X Department of Computer-Integrated Technologies, Automation and Mechatronics Kharkiv National University of Radioelectronics Kharkiv, Ukraine oksana.sychova @nure.ua

converter. The interface can be a serial RS-232 port or Ethernet.

The request is sent to the microcontroller, where a packet is formed for sending over a wireless network. Each packet receives a unique identifier. The transmitter sends the packet to the network and the device switches to receive mode, listening to information from network devices. The received data comes through the transmitter back to the microcontroller. Here they are checked for possible errors. After identification of the received data and their processing, the received information is sent also through the converter of interfaces to a local area network.

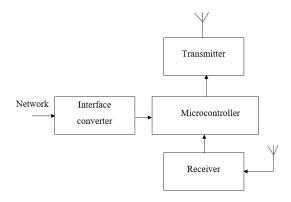


Fig. 1. Block diagram of the base module (gateway).

The block diagram of the energy metering device is shown in Fig. 2. The module includes: sensor; matching unit; analog to digital converter; microcontroller module; internal memory; status indicator; battery; power supervisor; transmitter; receiver.

The sensor is connected to the microcontroller via the matching unit. The sensor can be a digital or analog temperature sensor, current sensor, light sensor, humidity sensor, pressure sensor, etc. From the ADC output, the data is get to the input of the microcontroller through the I2C serial interface. The microcontroller module processes the commands received from the transmitter, and determines their affiliation to this sensor. After parsing the command, the data is read from memory and a packet is formed to be sent to the base module.

The transmission is performed by programmatically entering data that will be transmitted to the frame buffer Tx / Rx together with parameters such as destination address and number of iterations, programming one of the protocol timers to indicate the time at which the frame should be sent.

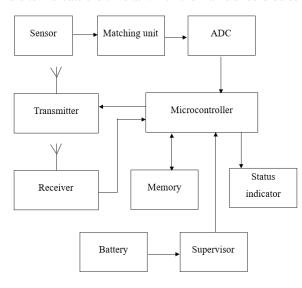


Fig. 2. Block diagram of the device of the metering of energy resources.

This time will be determined by higher-level software, such as the timing of the superframe and the interval. As soon as the packet is prepared and the protocol timer is set, the supervisor unit controls the transmission. When the scheduled time comes, the transmitter controls the sequence of operations of the radio unit and modem to perform the required transmission. The transmitter can execute all algorithms required by IEEE802.15.4, such as CSMA / CA and GTS without CPU intervention, including iterations and random returns.

When the transmission starts, the frame header is created from the parameters programmed by the software and sent with the frame data to the transmitter. At this time, the radio unit is ready for transmission. On the way the data flows to the modem, it enters the checksum generator, which calculates the checksum and attaches it to the end of the frame.

When receiving, the radio unit is configured to receive data on a specific channel. After receiving data from the modem, the frame is sent to the frame buffer Tx / Rx, where both the header and the frame data can be read by the protocol software. An interrupt may be generated when the frame header is received. The frame received from the receiver is transmitted to the checksum generator; at the end of the reception the result of the checksum is compared with the checksum at the end of the frame to control the correctness of the frame.

The network energy meter is powered by a built-in battery, so the program and design provide a mode of saving electricity. To do this, the device uses a supervisor. Its main task is to control the voltage on the battery.

In the case of its reduction to a critical value, the supervisor issues a signal to the microcontroller and it decides to transmit the signal to the network (warning about the transition from sleep mode) and switch to low power consumption mode.

III. ORGANIZATION OF THE MESSAGE EXCHANGE PROCESS

Two approaches to the organization of the confirmation exchange process are proposed: with downtime and with the organization of a floating window. Methods of communication are shown in Fig. 1.

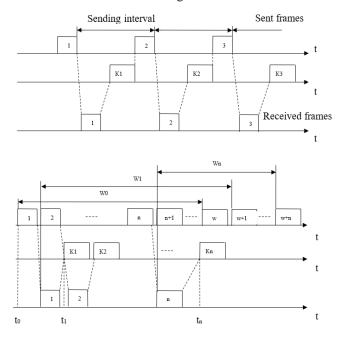


Fig. 3. Methods of organizing messaging.

The downtime method requires that the source that sent the frame expect to receive a confirmation (positive or negative) from the receiver and only then send the next frame (or repeat the distorted). If the confirmation does not fall during the timeout, the frame (or confirmation) is considered lost and its transmission is repeated.

In Fig. 3, *a* shows that in this case the performance of data exchange is significantly reduced. Although the transmitter could send the next frame immediately after sending the previous one, it must wait for the confirmation. The decrease in the productivity of this method of correction is especially noticeable on low-speed communication channels, i.e. in local area networks.

The second method is called the floating window method. In this method, to increase the use of the line, the source is allowed to transmit a number of frames in a continuous mode, i.e. at the maximum possible rate for the source, without receiving positive frames for these frames. The number of frames that can be transmitted in this way is called the window size. Fig. 3, b illustrates this method for a window the size of W frames.

The floating window method is more difficult to implement than the downtime method, because the transmitter must store in the buffer all frames for which positive confirmations have not yet been received. In addition, you need to track several parameters of the algorithm: the size of the window W, the frame number for which the confirmation was received, the frame number that can still be transferred before receiving a new confirmation.

The device may not send confirmations for each received correct frame. If several frames came almost together, the receiver can send a confirmation only for the last frame. This meant that all the previous frame and reached safely.

The floating window method has two parameters that can significantly affect the efficiency of data transmission between transmitter and receiver. This is the size of the window and the size of the timeout waiting for the confirmation. In reliability networks, the size of the window needs to be increased to increase the speed of data exchange. Because the transmitter will send frames with smaller pauses.

In unreliable networks, the window size should be reduced. With frequent losses and distortions of frames, their volume increases, so network bandwidth will be spent idle. Useful network bandwidth will be reduced. The choice of timeout does not depend on the network reliability, but on the delays in the frames transmission by the network. In many implementations of the floating window method, the window size and timeout are selected adaptively, depending on the current state of the network.

Thus, the method of data transmission using a floating window is advantageous at low speed information exchange and a reliable communication channel. If there is a problem area of the network, the method of sequential confirmation by speed is close to the method with a floating window due to the large number of lost frames and the need to resend the message.

IV. EXPERIMENTAL RESEARCH

The LoRaWAN protocol provides full two-way communication between network nodes and has special encryption methods to ensure the reliability and security of the system. A typical LoRaWAN network can be represented as end devices (points, nodes), the data of which is transmitted in encrypted form to the gateways, then to the provider's network server and then to the provider's application server, where it comes to the end user.

In a LoRaWAN network, gateways are also called hubs, endpoints, points, or nodes. LoRaWAN nodes can perform various functions. It is measurement, management and control. Typically, such nodes are located at a distance from each other, and are powered by batteries. Using the LoRaWAN protocol, these nodes (points) are configured to communicate with the gateway (hub) LoRa.

Data from nodes is transmitted in both directions, from the node to the server and back. The nodes operate in the transmission mode only for short periods of time, then a temporary window for receiving data opens. The rest of the time the nodes are either in a dormant state or in a receiving state, which depends on the class of the device.

We will use the AnyLogic tool as a modeling tool. AnyLogic contains a graphical modeling language and allows the user to extend the created models using the Java language.

The experiment will be to simulate the behavior of a wireless network. The network gateway is selected as the simulation object. Let this device receive packets from energy meters and send them with a LoRaWan modem. The speed of sending messages will take 9600 B/s. Processing one frame will take a random time from 0.5 to 1.5 ms. In the

experiment, the time scale will be increased to illustrate the passage of time. Therefore, one millisecond in real time will be replaced by one second in the simulation system.

In Fig. 4 shows the window for setting the "Delay" element, which delays the agents for a specified period of time.

🔲 Свойства 🛛	1 V 5	° 🗆
🕚 delay - Delay		
Имя: ПИсключить	delay 🗹 Отображать имя	^
Тип задержки:	 Определенное время До вызова функции stopDelay() 	
Время задержки:	🚽 triangular(0.5, 1.0, 1.5) секунды 🗸	
Вместимость:	=, 1	
Максимальная вместимость:	=, 🗆	
Место агентов:	=, v);	

Fig. 4. Setting item "Delay".

The delay time is calculated dynamically, may be random, depending on the current agent or any other conditions. This time is given by the triangular function, which is described by the formula:

$$f(x) = \begin{cases} \frac{2(x - \min)}{(\max - \min)(\mod e - \min)}, \min < x \le \mod e\\ \frac{2(\max - x)}{(\max - \min)(\max - \mod e)}, \mod e < x \le \max \end{cases}$$

where

min = minimum(x); max = maximum(x); mode = most likely.

The triangular distribution is often used in the absence of sufficient information or its complete absence. He can rarely accurately describe the value. Nevertheless, due to the ease of use, the triangular distribution is used as a functional form of representation of areas with blurred logic.

This function automatically checks whether the most probable value of x (*mode*) belongs to a certain interval (*min*, *max*). If the specified maximum value is exceeded, the function considers it as the maximum. Conversely, *max* is considered as *mode*, i.e. the appeal to the triangular function (1, 5, 10) is equivalent to triangular (1, 10, 5). This generates a variant of the triangular distribution with a minimum value of 1, a maximum value of 10 and the most probable value of 5. The result was the following scheme of the simulated process, as shown in Fig. 5.

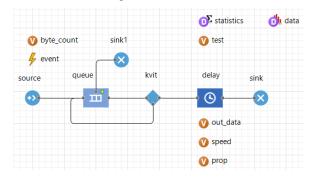


Fig. 5. Scheme of the simulated process.

In this scheme, each packet sent is waiting to be sent and then confirmed by the receiver. The diagram uses the "Kvit" element to model this behavior. This element can be configured so that the confirmation of packets will take place with a certain probability.

In this experiment, a value of 0.2 was chosen as the most appropriate to the actual values in the network. In fig. 6 shows the result of the experiment.

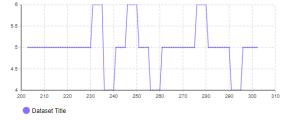


Fig. 6. The result of the experiment.

The result shows that the average network bandwidth is five packets per second.

The second experiment will be to implement a floating window to transmit a set (sequence) of message packets. In our case, the number of messages in the sequence is fixed and equal to five. After receiving the sequence of messages, their integrity is checked and a return message is sent, which confirms the correctness of the data.

The "Batch" component was selected to simulate a floating window. The Batch object converts a specified number of agents that enter the object to a single batch agent. The party can be permanent or temporary. With the creation of a permanent batch, the agents stored in the queue are destroyed (and the properties of the batch agent may depend on the properties of these agents). With the creation of a temporary batch, all these agents are added to the contents of the batch agent and can be subsequently removed from there using the Unbatch object.

This object contains a queue (Queue object) inside which stores the incoming agents. With the accumulation of the number of agents equal to a given batch size, one new agent (agent-batch) is created, which instantly leaves the object.

After receiving five message packets, the "Batch" component generates one final packet, which arrives at the block "Kvit_1". This unit also generates packets that have not been validated with a probability of 0.2. Information that has not been validated is returned to the queue by the "Split" component. In fig. 7 shows the properties of the component "Split".

🔲 Свойства 🛛		\bigtriangledown	
🕅 split1 - Split			
Имя:	split1 Отображать имя		^
Исключить			
Количество копий:	⊋ 5		
Новый агент (копия):	=_ 🚯 Агент 🗸		
	создать другой тип		
Изменить размеры:	=, 🗆		
Место копии:	= Не задано 🗸		

Fig. 7. Properties of the component "Split".

In Fig. 8 shows a diagram of the second experiment with a "floating window".

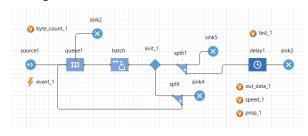


Fig. 8. Scheme of the second experiment with a "floating window".

In Fig. 9 shows the result of the experiment.



Fig. 9. The result of the experiment.

As can be seen from the experiments, in the case of using a "floating window" was able to solve the problem of increasing network bandwidth with the same data rate. In the second experiment, it was 10...15 packets per second.

V. CONCLUSIONS

Thus, the paper proposes two methods to increase the reliability of data transmission: the method of transmission with downtime and with the organization of a "floating window". The downtime method requires that the source that sent the frame expect to receive a confirmation (positive or negative) from the receiver and only then send the next frame (or repeat the distorted). According to another method, to increase the use of the line, the source is allowed to transfer a certain number of frames in a continuous mode, i.e. at the maximum possible rate for the source, without receiving positive frames for these frames.

An experimental study was conducted using the AnyLogic tool, which confirmed that the "floating window" method is best for these types of wireless networks.

REFERENCES

- Nevliudov I.Sh. Programming technology of industrial controllers in an integrated CODESYS environment: Study manual / I.Sh. Nevliudov, S.P. Novoselov, O.V Sichova. - Kharkiv: KNURE, 2019, 264 p. DOI: 10.30837/978-966-659-265-4.
- [2] Al-Juboori G., Tsimbalo E., Doufexi A. [et al.]. A comparison of OFDM and GFDM-Based MFSK modulation schemes for robust IoT applications // IEEE 85th Vehicular Technology Conference (VTC Spring). 2017. P. 1–5.
- [3] Lwanitz F., Lange J. OPC Fundamentals, Implementation, and Application. 2 rev. Heidelberg: Hating, 2002, 225 p.
- [4] Long-distance data networks LoRaWAN [Electronic resource] / Access mode: www / URL: http://gamma.spb.ru/media/pdf/ masters2015/LORA.pdf – Title from the screen.

Using Remote Hardware Education Kit to Study Electronics Courses

Sergii V. Afanasiev ORCID 0000-0002-7195-4499 Department of Computer Engineering Chernihiv National University of Technology Chernihiv, Ukraine qvinnn666@gmail.com Nikita S. Poberezkyi ORCID 0000-0002-5890-2504 Department of Computer Engineering Chernihiv National University of Technology Chernihiv, Ukraine Poberezsky@gmail.com

Abstract—Using of remote tools for studying courses in electronics (digital design or microcontroller programming) can increase the efficiency of student learning. RHE (Remote Hardware Education) is a set of software and hardware equipment. And also, to reduce the load on the use of hardware testing, which will entail a reduction in costs for the purchase of components.

Keywords—programming, C++, FPGA, master-server, slave-server.

I. INTRODUCTION

The COVID-19 pandemic has forced universities to move to distance education and completely change the way they teach. This has not only led to the intensive use of online technologies for lecturing, but also raised the question of conducting laboratory seminars using real equipment. Learning of digital design is impossible without gaining practical skills. For more, most educational institutions around the world use FPGA. That is reason why students are given the opportunity to study certain disciplines, while testing the acquired skills on the "development boards". With help of these "boards" the student can see immediately whether he understood the theoretical material correctly or not. But, unfortunately, the price on these boards is in such a price range that educational institutions cannot purchase so many units, that each student can work separately. In this case, students must form groups of three or five people and perform laboratory work in teams. It is the lack of individual student work that negatively affects the educational of the course.

To solve this problem, systems are used that allow students to perform laboratory work with hardware remotely, for example, at home, individually, while interacting with the required number of peripherals of the "stand", and see the results through the client [1, 5, 9].

II. TECHNICAL CHARACTERISTICS

RHE (Remote Hardware Education) is a set of software and hardware that allows you to remotely program FPGAs or microcontrollers.

The complex consist of a client part, in the form of a program that connects to the server part via the Internet. In turn, the server part consists of a Master-server, which manages the Slave-servers via wireless communication Sergey A. Ivanets ORCID 0000-0002-9587-0783 Department of Biomedical Radio-Electronic Devices and Systems Chernihiv National University of Technology Chernihiv, Ukraine Sergey.Ivanets@gmail.com

technologies. Each Slave-server is connecting to a development board with FPGA or microcontroller, which controls the peripherals that are installed on the board. Both Master and Slave servers are Raspberry Pi (specialized single-board computers) [4].

FPGA-based project development will take place on the client side with Quartus Prime software [3]. During development, the student must assign a chip and pins according to the documentation to the development board. While developing a project, the student simulate a project. Student make testbenches in the hardware description language (Verilog or VHDL) and time diagrams are drawn by simulation software [2, 8]. These timing diagrams can then be compared with those obtained on the debug board. The development board with the FPGA chip is connected to the slave server. If the project was compiled successfully, the student must upload the FPGA configuration file to the client part of the remote software and send it to the Master-server. This file will be transferred from the main server to the slave server. The FPGA programming tool will be installed on the slave server. In our case, this is Altera Remote JTAG Server - part of the Quartus tools. Slave-servers will program the connected development board through GPIO ports.

In the client part of the remote software, we can also control the signals that are fed to the input ports of the development board and can see signals from the development board.

III. THE CLIENT PART

As described above, the client part is a program on the user's computer [6]. The program will have the following interface: login/registration window and the main window. In login/registration window has placed fields for entering login and password; as well as additional fields, for entering last name, first name and organization, which use for registration in the system. The main window will display:

- development board with active components, particularly with switches or keys;
- static output signals from development board that emulate LEDs on board;

MC&FPGA-2020

- imitation of logic analyzer, which will show time diagrams from the data lines which the logic analyzer is connected;
- current consumption, which is read from the ammeter and allows experiments to measure the dependence of current on the frequency and size of the project on the FPGA;
- field for downloading the firmware file to the debugging board.

In case of working with the debugging board with FPGA, the client part will analyze the firmware file, in order to check the correct connection of such baselines as 'clk', 'reset' and switch lines according to the specific board.

IV. THE SERVER

The server is required to receive a request from a user who sends this request from the client side [7]. The server is essentially divided into two major sub-parts: part of the main control (Master-server) and part of the child controls (Slaveserver). The main control element is the part that is responsible for receiving the request from the user, then analyzes among a number of child elements and selects the one, that can process this request in the future. After the child element has been selected, the Master-server generates request to the Slave-server: this request includes commands, that directly control the process of interaction with the FPGA. When the FPGA-board starts, the Slave-server will analyze the activity on the I/O ports, generate and send data packets to the Master-server; the main control will forward the packets to the client.

Every Slave-server, that interacts with the FPGA, is allocated for each active session. The Master-server in turn acts as an arbiter.

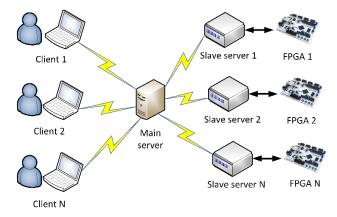


Fig. 1. Block diagram of the complex RHE

V. PART OF THE MAIN CONTROL ELEMENT

Both a regular computer and a specialized computer can be selected as the main control element (Master-server). The main requirement for the executing of this component is the operating system, which provides reception and processing of requests from the client, analysis of these requests and transmission to the selected child control (Slave-server) and the implementation of reverse exchange. Also, the task of the Master-server is to manage the process of working with many clients at the same time – this allows many students to perform work contemporaneously.

VI. PART OF THE CHILD CONTROLS

It is planned to choose a specialized computer with a high-level operating system for the role of one control element (Slave-server). This allows the use of multi-level software modules, services and drivers, which speeds up system development and simplifies software support in the future. For example, instead of creating an interface for FPGA programming, you can install a special driver for the programmer chip. One of the tasks of the Slave-server is the analysis of logical levels on the I/O ports: after starting the FPGA firmware, all logical levels will be read, data packets will be formed and sent to the Master-server; the Masterserver will send packets to the client, and the client will simulate and display the result in the form of time diagram.

The developed system provides several such controls. Each FPGA-board must have its own control (Slave-server), which will be subordinated to the main control (Masterserver).

An ammeter is used to measure the current consumption of the development board, which can be connected to a Slave-server via a USB port. This simple methods allows you to see how the current changes depending on the system frequency, the size of the project on the FPGA chip.

VII. CONCLUSIONS

The complex described in this article will allow you to work remotely with FPGA or microcontroller development board. This opportunity provides a solid foundation for building in the field of hardware, the process of distance learning, which is becoming increasingly popular every day, or is the only means of learning during today's emergencies. Also, remote work with hardware has great potential in creating an Internet service that provides a hardware platform for users, who do not have the opportunity to purchase a similar platform.

REFERENCES

- F. Morgan et al., "Remote FPGA Lab with Interactive Control and Visualisation Interface," 2011 21st International Conference on Field Programmable Logic and Applications, Chania, 2011, pp. 496-499, doi: 10.1109/FPL.2011.98.
- [2] Proektuvannya komp'yuternykh system na osnovi mikroskhem prohramovanoyi lohiky: monohrafiya / avt: V. V. Kazymyr, V. V. Lytvynov, S. A. Ivanets'. – Chernihiv: Chernihivs'kyy natsional'nyy tekhnolohichnyy universytet, 2013. – 305 s.
- [3] Quartus® Prime Standard Edition Handbook. Intel Corp., 2017.
- [4] Raspberry Pi (Trading) Ltd, "Raspberry Pi Compute Module 3+ Datasheet," Raspberry Pi (Trading) Ltd, 2019, pp. 7–8.
- [5] A. I. Strelets, V. S. Ivannikov, M. N. Yokhin and A. A. Skitev, "FPGA-based configurable virtual stand," 2018 IEEE Conference of Russian Young Researchers in Electrical and Electronic Engineering (EIConRus), Moscow, 2018, pp. 374-378, doi: 10.1109/EIConRus.2018.8317110.
- [6] B. Stroustrup, "Programming Principles and Practice Using C++," Moscow: Williams, 2016, pp. 456–467.
- [7] E. Tanenbaum, D. Weatheroll, "Computer networks," 5th ed., St. Petersburg: Piter, 2012, pp. 770–778.
- [8] Tsifrovoy sintez: prakticheskiy kurs / pod obshch. red. A. Y. Romanova, Y. V. Panchula. M.: DMK Press, 2020. 556 s.
- [9] M. Winzker and A. Schwandt, "Open Education Teaching Unit for Low-Power Design and FPGA Image Processing," 2019 IEEE Frontiers in Education Conference (FIE), Covington, KY, USA, 2019, pp. 1-9, doi: 10.1109/FIE43999.2019.9028694.

Fuzzy Logic Custom Instruction Set for NIOS II Processor

Sergey A. Ivanets ORCID 0000-0002-9587-0783 Department of Biomedical Radio-Electronic Devices and Systems Chernihiv National University of Technology Chernihiv, Ukraine Sergey.Ivanets@gmail.com Artem P. Fesenko ORCID 0000-0001-8730-3327 Department of Biomedical Radio-Electronic Devices and Systems Chernihiv National University of Technology Chernihiv, Ukraine gudrunas.ch@gmail.com Oleksandr M. Fesiuk Department of Biomedical Radio-Electronic Devices and Systems Chernihiv National University of Technology Chernihiv, Ukraine fesuks1@gmail.com

Abstract—The article describes a way to implement operations on fuzzy sets using additional processor instructions. As a target, a NIOS II soft processor is used. Due to the hardware implementation of instructions, the speed of their execution increases significantly. The integration of fuzzy instructions into the NIOS II processor instruction set simplifies the process of developing programs that use fuzzy inference algorithms.

Keywords—fuzzy logic, FPGA, custom instruction, NIOS II.

I. INTRODUCTION

The idea of developing processors with fuzzy logic is based on fuzzy mathematics. The mathematical theory of fuzzy sets was introduced by L. A. Zade [1]. Since its introduction, it was under intensive research and, as a result, have opened wide opportunities for system analytics. Based on fuzzy sets theory systems, correspondingly, have widened the application of fuzzy logic. Unlike the traditional formal logic, that operates with accurate and clear definitions such as true and false, yes and no, zero and one, fuzzy logic deals with values in certain analog or discrete range called linguistic variables, for example, "far", "close", "warm", "cool". Fuzzy logic control algorithms are called fuzzy inference systems.

Fuzzy inference systems have been successfully applied in fields such as automatic control, data classification, decision analysis, expert systems, and computer vision. Because of its multidisciplinary nature, fuzzy inference systems are associated with a number of names, such as fuzzy-rule-based systems, fuzzy expert systems, fuzzy modeling, fuzzy associative memory, fuzzy logic controllers, and simply (and ambiguously) fuzzy systems [2].

Embedded systems increasingly use FPGAs due to their superior cost and flexibility compared to custom integrated circuits [3]. FPGA systems often incorporate two types of processors, soft and hard. Soft processors are implemented using the fabric itself. Hard cores are fabricated separately and could offer higher performance compared to soft processors, but they are inflexible and wasted when not needed. Accordingly, there is a need to develop soft cores that provide high performance. The ways of improving the performance of soft processors were researched in [1]. According to research, among different techniques of improving the performance of soft processors, the most effective one is hardware processor system extension according to specific application domain. This approach is capable of bringing up to 100x performance improvement. There are two ways of implementing processor system extension: custom peripherals and custom processor instructions. Custom instructions approach if preferred way, if performance increase is considered in [4].

II. FUZZY LOGIC

The typical structure of fuzzy inference system or fuzzy controller includes the following components (Fig. 1):

- fuzzification unit;
- inference mechanism unit;
- rule base unit;
- defuzzification unit.

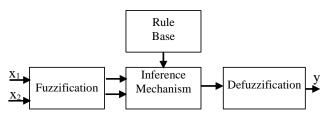


Fig. 1. The structure of typical fuzzy controller.

That is, according to the structure, fuzzy logic controller involves four main stages: fuzzification, rule base, inference mechanism and defuzzification. Fuzzification unit is responsible for converting real world crisp signals into fuzzy values for further processing. The inference mechanism determines the matching degree of the current fuzzy input with respect to each rule and decides which rules are to be fired according to the input field. Next, the fired rules are combined to form the control actions [5].

During the fuzzification step, the current system input values are compared against stored input membership functions to determine the degree to which each label of each system input is true. This is accomplished by finding the yvalue for the current input value on a membership function for each label of each system input. A membership function

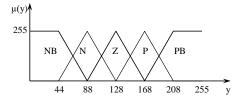


Fig. 2. Membership functions.

The use of piecewise membership functions is explained by the simplicity of their hardware implementation. To determine the trapezoid membership function (fig. 3), it is necessary to use four points a, b, c, d.

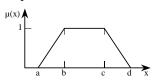


Fig. 3. Trapezoid membership functions.

Then the trapezoid membership functions will be represented by the following system:

$$\mu(x) = \begin{cases} 0, x \le a \\ \frac{x-a}{b-a}, a \le x \le b \\ 1, b \le x \le c \\ \frac{d-x}{d-c}, c \le x \le d \\ 0, d \le x \end{cases}$$
(1)

For the duration of fuzzy inference each rule is evaluated sequentially, but the rules as a group are treated as if they were all evaluated simultaneously. Two mathematical operations take place during rule evaluation. The fuzzy AND operator corresponds to the mathematical minimum operation and the fuzzy OR operation corresponds to the mathematical maximum operation. The fuzzy ABD is used to connect antecedents within a rule. The fuzzy OR is implied between successive rules. Before evaluating any rules, all fuzzy outputs are set to zero (meaning not true at all). As each rule is evaluated, the smallest (minimum) antecedent is taken to be the overall truth of the rule. This rule truth value is applied to each consequent of the rule (by storing this value to the corresponding fuzzy output) unless the fuzzy output is already larger (maximum). If two rules affect the same fuzzy output, the rule that is most true governs the value in the fuzzy output because the rules are connected by an implied fuzzy OR.

Rule base in fuzzy controller consists of IF-THEN rules. These IF-THEN rule statements are used to formulate the conditional statements that comprise fuzzy logic.

A single fuzzy IF-THEN rule assumes the form:

if x is A then y is B

where A and B are linguistic values defined by fuzzy sets on the ranges (universes of discourse) X and Y, respectively. The IF-part of the rule "x is A" is called the antecedent or premise, while the THEN-part of the rule "y is B" is called the consequent or conclusion.

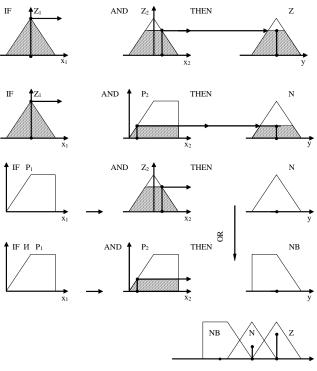


Fig. 4. Fuzzy inference.

)

Interpreting IF-THEN rules is a three-part process (fig. 4):

1. Fuzzify inputs: Resolve all fuzzy statements in the antecedent to a degree of membership between 0 and 1. If there is only one part to the antecedent, then this is the degree of support for the rule.

2. Apply fuzzy operator to multiple part antecedents: If there are multiple parts to the antecedent, apply fuzzy logic operators and resolve the antecedent to a single number between 0 and 1. This is the degree of support for the rule.

3. Apply implication method: Use the degree of support for the entire rule to shape the output fuzzy set. The consequent of a fuzzy rule assigns an entire fuzzy set to the output. This fuzzy set is represented by a membership function that is chosen to indicate the qualities of the consequent. If the antecedent is only partially true, (i.e., is assigned a value less than 1), then the output fuzzy set is truncated according to the implication method.

III. SYSTEM-ON-CHIP WITH NIOS II PROCESSOR

FPGA-based System-On-Chip (SOC) use processor cores. With Altera/Intel FPGA we can use NIOS II soft processor [6]. To work with this processor using the Quartus Prime software we need to create a microprocessor system. Figure 3 describes the functional diagram of simple microprocessor system with NIOS II soft processor. In addition to the NIOS II processor, the smallest system has a timer (T), RAM and ROM for data and instruction, JTAG-UART for debagging and download software and PIO for

II International Scientific and Practical Conference Theoretical and Applied Aspects of Device Development on Microcontrollers and FPGAs connecting external devices. All these modules are connected by Avalon system bus (fig. 5).

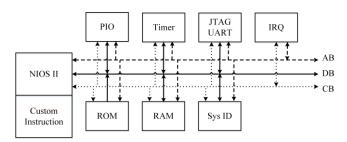


Fig. 5. Functional Diagram of NIOS II System.

All computational operations are performed by the NIOS II processor and NIOS II controls external devices using the bus Avalon, which includes: the address bus (AB), data bus (DB) and control bus (CB).

IV. CUSTOM INSTRUCTION SET

User instructions ("custom instruction") is the instructions for the processor, which creates the user, which allows to significantly accelerate the speed of operation of the processor. For NIOS II processor have the ability to create up to two hundred fifty-six of such instructions. To implement fuzzy logic support in NIOS II, it is necessary to implement such instructions in the processor:

- FUZZ fuzzification for two inputs;
- RULE calculation base of fuzzy rules;
- DEFUZZ defuzzification.

When the fuzzification step begins, the current value of the system input is in an accumulator of the NIOS II, one index register points to the first membership function definition in the knowledge base, and a second index register points to the first fuzzy input in RAM. As each fuzzy input is calculated by executing a FUZZ instruction, the result is stored to the fuzzy input and both pointers are updated automatically to point to the locations associated with the next fuzzy input. The FUZZ instruction takes care of everything except counting the number of labels per system input and loading the current value of any subsequent system inputs.

RULE instruction. Rule evaluation is the central element of a fuzzy logic inference program. This step processes a list of rules from the knowledge base using current fuzzy input values from RAM to produce a list of fuzzy outputs in RAM.

The complete rules are stored in the knowledge base as a list of pointers or addresses of fuzzy inputs and fuzzy outputs. For the rule evaluation logic to work, there must be some means of knowing which pointers refer to fuzzy inputs and which refer to fuzzy outputs. There also must be a way to know when the last rule in the system has been reached.

- One method of organization is to have a fixed number of rules with a specific number of antecedents and consequents.
- A second method, employed in Freescale M68HC11 kernels, is to mark the end of the rule list

with a reserved value, and use a bit in the pointers to distinguish antecedents from consequents [7].

• A third method of organization, used in the Freescale HSC12, is to mark the end of the rule list with a reserved value, and separate antecedents and consequents with another reserved value [8]. This permits any number of rules, and allows each rule to have any number of antecedents and consequents, subject to the limits imposed by availability of system memory.

These fuzzy outputs can be thought of as raw suggestions for what the system output should be in response to the current input conditions. Before the results can be applied, the fuzzy outputs must be further processed, or defuzzified, to produce a single output value that represents the combined effect of all of the fuzzy outputs.

The defuzzification instruction (DEFUZZ) calculates the value that best describes the fuzzy value of the output linguistic variable. For defuzzification we use the center of gravity method, sometimes called the center of gravity method for singletons. The calculation of the sums required by the method of the center of gravity turns out to be several orders of magnitude faster than the numerical integration required in the method of the center of the region:

$$Y = \frac{\sum_{i=1}^{p} Y_i \cdot a_i}{\sum_{i=1}^{p} a_i},$$
(2)

where Yi is the value of the center of the maximum for the ith term;

ai - weight of the i-th term.

V. CONCLUSIONS

Custom instructions are one of the benefits of software processors, as they are added directly to the processor core and instruction set. Using custom instructions in NIOS II processor significantly speeds up the operation of fuzzy control algorithms and simplifies the task of writing programs for such algorithms. This instructions increase processor size in FPGA chip, but are one of the most effective ways to speed up program execution.

REFERENCES

- L.A. Zadeh, "Fuzzy sets" Information and Control, Vol. 8, Issue 3, pp. 338-353, June 1965, doi: 10.1016/S0019-9958(65)90241-X.
- [2] J. Jantzen Foundations of Fuzzy Control: A Practical Approach. John Wiley & Sons, 2013. 352 p.
- [3] Proektuvannya komp'yuternykh system na osnovi mikroskhem prohramovanoyi lohiky: monohrafiya / avt: V. V. Kazymyr, V. V. Lytvynov, S. A. Ivanets'. – Chernihiv: Chernihivs'kyy natsional'nyy tekhnolohichnyy universytet, 2013. – 305 s.
- [4] Embedded Design Handbook. Intel Corp., 2020. 497 p.
- [5] C. C. Lee, "Fuzzy logic in control systems: fuzzy logic controller. I," in *IEEE Transactions on Systems, Man, and Cybernetics*, vol. 20, no. 2, pp. 404-418, March-April 1990, doi: 10.1109/21.52551.
- [6] Nios II Custom Instruction User Guide. Intel Corp., 2020. 66 p.
- [7] HC11. MC68HC11F1. Technical Data. Freescale Semiconductors, 2004. 158 p.
- [8] S12CPUV2 Reference Manual. HCS12 Microcontrollers. Freescale Semiconductors, 2006. 452 p.



Application of Software Signal Filtering in an Ultrasonic Rangefinder

Artem Khromenko ORCID 0000-0002-5120-1094 Department of Microelectronics, Electronic Devices and Appliances Kharkiv National University of Radio Electronics Kharkiv, Ukraine artem.khromenko@nure.ua

Abstract—This article describes an example of creating an ultrasonic rangefinder on the ARDUINO platform using inexpensive modules and components. The main feature of the device is the use of a software method of filtering values, which significantly increases its accuracy, and makes the device comparable in accuracy with industrial analogues, with a relatively low cost.

Keywords—board, ultrasonic sensor, Arduino, filter

I. OBJECTIVE

In everyday life, or in view of the characteristics of the sphere of activity, we often encounter the need to measure the distance to an object or its length, whether it be a wall, ceiling, room height, etc. It is not always convenient to use a classic measuring tool in the form of a ruler, tape measure or carpentry «meter», taking into account the measurement features, scope or other factors.

The aim of this work is to develop a portable pocket rangefinder of sufficient accuracy on an inexpensive element base for use in construction, carpentry or domestic purposes as a universal device for measuring short distances. The device must meet the following requirements:

- compactness;
- ergonomics (low power consumption);
- range of the measured distance to 4-5m;
- error in the measurement of 1 2 mm;
- digital display of information.

II. IMPLEMENTATION

To implement this project, the ARDUINO Nano platform on the Atmega 328 microcontroller was used as the main module. The HC SR04 ultrasonic sensor was used as the range finder sensor. Information is displayed on the fourdigit seven-segment display of the 74NS595. Conventional AA batteries were used as a power source. In the future, it is planned to equip the device with a lithium-ion battery with the possibility of recharging it. A modular diagram of the device is shown below. Liliia Saikivska ORCID 0000-0002-4139-7732 Department of Microprocessor Technologies and Systems Kharkiv National University of Radio Electronics Kharkiv, Ukraine liliia.saikivska@nure.ua

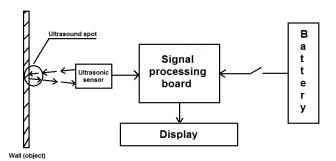


Fig. 1. A modular diagram of the range finder.

III. PRINCIPLE OF OPERATION

The operation of the device can be described as follows: the Arduino platform generates a series of consecutive pulses that are transmitted to the emitter of the ultrasonic sensor, the sensor emits these pulses, captures their reflections and generates signals at its output, which are fed to the processor digital inputs. The processor, according to the written algorithm, calculates the time between the signal sent to the sensor and its response to the reflected signal. The received data is generated into a data array and processed using software filtering, in order to avoid accidental outliers of false results, and to increase the measurement accuracy. Software filtering methods will be described below. From a certain frequency, the processed results, digitized and converted to metric format, are displayed on a digital display. The display refresh rate can be varied, the speed of updating the data on the display when the distance from the sensor to the object changes depends on it.

IV. APPLICATION SOFTWARE FILTERING

Using the ARDUINO platform, we can write program code using several methods to filter output values. This, in turn, can significantly improve the measurement results, namely, to minimize the noise generated by the ultrasonic sensor due to its design features.

A. Median filter

The appropriateness of using software filtering of signals received from an ultrasonic sensor is due to the fact that as a result of analog-to-digital conversion, a number of values can be obtained in which one or more will significantly differ from neighboring ones, for example: "58, 61, 59, 231, 60. " A value of 231 is supposedly anomalous and should be ruled out. If you try to use the classic linear filter, you will see that a value of 321 will have a significant effect on the result. The best solution in this case is to use a median filter. For even "n" values, the median is usually defined as the arithmetic average of two average samples of the ordered sequence, that is, in contrast to the arithmetic average, it finds the "average among the average", and not among all the values, thereby filtering out sharp outliers. The graph below shows the result of the filter against emissions:

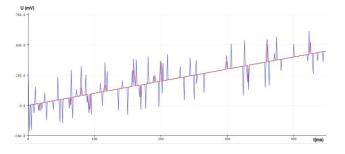


Fig. 2. Is a graph of the median filter, where the blue graph is the real value, the red is filtered.

It should be noted that the higher the dimension of the median filter, the better it cuts off frequent outliers, but at the same time the processor load increases as the number of calculations increases, which entails an increase in the time for updating data and displaying it. In this case, the median filter from the last 3 measurements is used, an example of program code using the median filter is shown below:

```
// Median filter of 3 values
float middle_of_3(float a, float b, float c) {
    if ((a <= b) && (a <= c)) {
      middle = (b <= c) ? b : c;
    }
    else {
      if ((b <= a) && (b <= c)) {
        middle = (a <= c) ? a : c;
    }
    else {
        middle = (a <= b) ? a : b;
    }
    return middle;
}</pre>
```

B. Filter running average

To achieve maximum accuracy, the running average filter algorithm was also used - this is a method of smoothing time series in order to exclude the influence of a random component. The method consists in replacing the actual values of the members of the series with the arithmetic mean of the values of the several members closest to it. A set of averaged values forms the so-called sliding window. A member whose value is replaced by the window average takes the middle position in the window.

The filter has a setting parameter as a "filtration coefficient", with the help of which a range of filtered values - outliers is adjusted. This coefficient ranges from 0 to 1.

The following is an example of applying a running average filter to combat random outbursts of a uniformly growing signal.

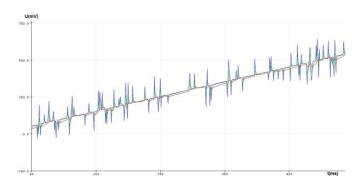


Fig. 3. Graph of the moving average filter, where the blue graph represents the real value, red filtered with a coefficient of 0.1, green with a coefficient of 0.5.

An example of program code using a moving average filter is shown below:

```
if (delta > 1) k = 0.7;
else k = 0.1;
dist filtered = dist * k + dist filtered * (1 - k);
```

V. CONCLUSION

The use of two types of filtering in the software and hardware code allowed to significantly increase the accuracy of the device to an error of only 1 mm, and its implementation on a common component base makes it affordable and cheap to manufacture.

This device is not an accurate measuring tool, but it can be used to perform small, often performed measurements in the home or construction.

REFERENCES

- Goldenberg, L.M. et al. Digital signal processing. Directory. Radio and communication / L.M. Goldenberg. - Moscow, 1985.- 312 p.
- Boxell, J. Learning ARDUINO. 65 do-it-yourself projects / J. Boxel -St Petersburg, 2017 .- 400 p.

MC&FPGA-2020

Processes Analysis of Networks Management Systems

41

Lubomyr Petryshyn dept. of Enterprise Management AGH University of Science and Technology Cracow, Poland l.b.petryshyn@gmail.com ORCID: 0000-0003-4168-3891 Wioleta Cieslik dept. of Computer Science AGH University of Science and Technology Cracow, Poland w.cieslik@gmail.com Mykhailo Petryshyn dept. of Computer Science and Information Systems Precarpathian National University Ivano-Frankivsk, Ukraine m.l.petryshyn@gmail.com ORCID: 0000-0001-6319-3768

Analizy Procesowa Sieciowych Systemów Zarządzania

Lubomyr Petryshyn kat. Zarządzania Przedsiębiorstwem AGH University of Science and Technology Kraków, Polska l.b.petryshyn@gmail.com ORCID: 0000-0003-4168-3891 Wioleta Cieślik kat. Informatyki Stosowanej AGH University of Science and Technology Kraków, Polska w.cieslik@gmail.com Mykhailo Petryshyn kat. Nauk Komputerowych i Systemów Informatycznych Precarpathian National University Ivano-Frankivsk, Ukraina m.l.petryshyn@gmail.com ORCID: 0000-0001-6319-3768

I. WSTĘP

Zarządzanie złożonymi systemami w warunkach kooperacji sektorowej wymaga zastosowania technologii informacyjnej, która zapewnia odwzorowanie stanu systemu i umożliwia zarządzanie systemem w czasie rzeczywistym. Analiza oraz wizualizacja procesów zarządzania pozwala na psychologicznej bariery i usuniecie unikniecie nieporozumienia pomiędzy klientem i twórcą systemów informatycznych, a także pozwala zmniejszyć koszty opracowania, wdrażania i obsługi takich złożonych systemów.

Celem opracowania jest przedstawienie techniki analizy procesowej jak podstawy wizualnych metod modelowania procesów zarządzania złożonymi systemami w warunkach kooperacji sektorowej, a także opracowanie uproszczonego przykładu systemu zarządzania siecią dostaw produkcji.

Nowacją pracy jest przedstawienie techniki analizy systemowej, która przy jej implementacji w trakcie modelowania informacyjnego systemów zapewnia wizualizację procesów zarządzania i upraszczają rozumienie ich przepływów.

Aspekt praktyczny polega na kompleksowej analizie struktury i przepływu procesów zarządzania, unikania nieporozumień przy formułowaniu zadania i zapewniania wymagań klienta, a także zmniejszania kosztów tworzenia i eksploatacji systemów zarządzania. W projekcie pozostał

cbiorstwem ka Science A y a il.com 168-3891

Adnotacja—Modelowanie procesów zarządzania w warunkach kooperacji sektorowej na podstawie rozproszonych systemów informatycznych pozwala zmniejszyć koszty opracowania i eksploatacji takich złożonych systemów. Proponowana technika analizy procesowej pozwala na dekompozycję całościowego procesu systemu zarządzania oraz na wizualizację modeli informacyjnych oraz odwzorowanie w formie graficznej procesów i upraszcza porozumienie się na etapie analizy i projektowania pomiędzy klientem a producentem systemu. Przedstawiono podstawy analizy systemowej i uproszczony przykład opracowania systemu zarządzania siecią dostaw produkcji.

Słowa kluczowe—analiza procesowa, modelowanie wizualizacyjne, procesy informacyjne, kooperacja sektorowa, systemy rozproszone, zarządzanie

Abstract—Simulation of the processes of sectoral cooperation management in distributed information systems allows to reduce the means of introduction and operation of such complex systems. The proposed method of visualization of information models reflects graphically the constituent processes and simplifies the understanding at the stage of analysis and design between the customer and the system developer. The basics of visualization modeling and simplified example of models development of multi-sectoral management system are presented.

Keywords—process analysis, visualization modeling, information processes, sectoral cooperation, distributed systems, management opracowany uproszczony przykład systemu zarządzania siecią dostaw produkcji gastronomicznej.

Podstawy modelowania wizualizacyjnego są opublikowane w [1]. Przeanalizujemy uproszczony przykład modelowania rozproszonego systemu zarządzania siecią sprzedaży produkcji z punktów gastronomicznych w skali kraju w celu usprawnienia i ułatwienia potencjalnemu klientowi wyboru konkretnego zamówienia wg jego potrzeb w danej chwili. Innym aspektem jest wypromowanie początkujące punktów gastronomicznych i poszerzenie oferty sprzedażowej tych, które już prosperują na rynku.

Na początku zostanie przedstawiona analiza jednostek organizacyjnych portalu (rys. 1) oraz ich funkcje systemowe. W trakcie modelowania systemu korzystano z istniejących już systemów prezentujących podobną ofertę.

II. ANALIZA POSZCZEGÓLNYCH JEDNOSTEK SYSTEMU

A. Zarząd

Główną funkcją zarządu jest wybór dyrektora, oraz kontrola wyników, jakie firma osiąga pod jego władzą.

B. Dyrektor

Do zadań Dyrektora należy optymalne zarządzanie wszystkimi działami firmy.

C. Dział Sprzedaży

Podstawową funkcją tego działu jest sprzedaż produktów i monitorowanie całego procesu sprzedaży, w szczególności zbieranie informacji o pozycjach najczęściej wybieranych przez klientów, najbardziej obleganych restauracji. Dział ten zarządza działem obsługi klienta, który dba o dobre relacje z klientem i rozpatruje wszelkie zgłoszone reklamacje.

D. Dział dostaw

Zajmuje się nadzorem nad poprawnym przebiegiem procesu dostawy. Czuwa nad tym, aby zamówienie klienta dotarło do odpowiedniego dostawcy usług gastronomicznych i kontroluje dostawę zamówienia z danego punktu gastronomicznego do klienta.

E. Dział finansów

Zajmuje się finansami oraz rachunkowością w firmie.

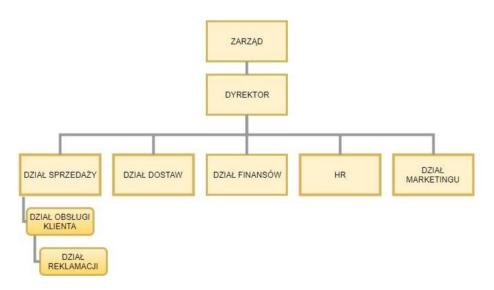
F. HR

Podstawową funkcją jest pozyskiwanie nowych pracowników, stworzenie możliwości rozwoju dla przyjętych już pracowników np. poprzez organizowanie szkoleń oraz dbanie o dobrą komunikację wewnętrzną. Ma na celu stworzenie dogodnych warunków pracy i zapewnienie rozwoju pracownikom.

G. Dział marketingu

Zajmuję się organizowaniem promocji i opracowywaniem strategii marketingowych mających na celu przyciągnięcie nowych klientów i zatrzymanie obecnych. Zbiera informację i zajmuję się ich przetwarzaniem oraz dokonuje analiz w celu obrania najlepszej drogi do polepszenia jakości oferowanych usług.

Modelowany system jest kompleksowym serwisem do zamawiania produkcji online z dostawa pod podany adres, kumulujący ofertę mnóstwa współpracujących z nim punktów gastronomicznych. Model ten jest oparty na współpracujących ze sobą modułach: zamówienia, dostawa, finanse, marketing, analiza, sprzedaż, obsługa klienta, zniżka.



Rys. 1. Struktura organizacyjna i analiza funkcji poszczególnych jednostek systemu.

Celem działania systemu "Eat something" jest uproszczenie potencjalnemu klientowi złożenia zamówienia poprzez zestawienie mu wszystkich restauracji i umożliwienie łatwego wyboru odnosząc się do tego, na co w danej chwili ma ochotę.

III. ANALIZA FUNKCJONALNYCH WYMAGAŃ UŻYTKOWNIKÓW

- Prowadzenie bazy danych punktów gastronomicznych i ich menu poziomy cen, promocje, rabaty, opakowania zbiorcze, kalkulacja cen;
- Możliwość obsługi dowolnej liczby klientów;
- Przyjęcie zamówienia złożonego przez klienta;
- Przekazanie informacji o zamówieniu do konkretnego punktu gastronomicznego;
- Obsługa promocji i rabatów dla stałych klientów;
- Rejestracja użytkownika;
- Logowanie użytkownika;
- Modyfikowanie danych użytkownika;
- Integracja z systemami poszczególnych punktów gastronomicznych;
- Obsługa koszyka zamówień;
- Przechowywanie historii zamówień i ich stanów w celu ich późniejszej analizy;
- Obsługa kanału SMS;
- Obsługa kanału e-mail (promocje);
- Obsługa płatności PayU;
- Przegląd lokali i menu na podstawie wybranych filtrów;
- Umożliwienie wyboru pozycji, dodatków wg preferencji klienta w danej chwili;
- Umożliwienie wyboru adresu dostawy, sposobu płatności oraz specjalnych życzeń klienta co do dostawy;
- Dodawanie i usuwanie reklam promocyjnych pojawiających się na określony czas.

IV. ANALIZA NIEFUNKCJONALNYCH WYMAGAŃ UŻYTKOWNIKÓW

- Baza danych oparta na technologii SQL client-server. W podstawowej wersji program jest dostępny dla Microsoft SQL Server;
- Dostępne są funkcje replikacji i kopii zapasowych baz danych;
- System współpracuje z aplikacjami: webową i mobilną;
- Aplikacja mobilna jest dostępna na: Android, iOS;
- Aplikacja webowa dostępna jest na wszystkich przeglądarkach;
- System hostingowany jest na platformie Home.pl;
- Hosting będzie zawierał system Ubuntu 64-bitowy;

- Obsługa serwera realizowana jest przez program Apache;
- Wszystkie requesty są szyfrowane za pomocą SSL'a;
- Backend zrealizowany w technologii Java Spring;
- Frontend zrealizowany w technologii AngularJS;
- System dostępny 24h i 7 dni w tygodniu;
- Maksymalny czas niedostępności systemu to 1h w ciągu miesiąca;
- Zapewnia równoczesny dostęp 1000 użytkowników;
- Maksymalny czas reakcji wynosi 10 sekund;
- System powinien dać się łatwo rozszerzać;
- Obsługa 10 000 transakcji tygodniowo.
- V. ANALIZA PROCESÓW ZARZĄDZANIA SYSTEMEM
- A. Realizacja zamówienia
 - Przyjęcie zamówienia złożonego przez klienta;
 - Sprawdzenie czy trwają obecnie akcje promocyjne;
 - Weryfikacja Klienta;
 - Informacja zwrotna na temat udzielenia rabatu dla danego klienta;
 - Zarejestrowanie transakcji;
 - Przekazanie zamówienia do punktu gastronomicznego;
 - Informacja zwrotna na temat realizacji zamówienia przez partnera;
 - Powiadomienie klienta o czasie realizacji zamówienia.
- B. Promocja
 - Opracowanie kampanii promocyjnej;
 - Ujęcie promocyjnych cen w systemie;
 - Zebranie wyników do analiz w czasie trwania promocji;
 - Przeprowadzenie analiz po promocji.
- C. Złożenie zażalenia przez klienta (przypadek uznania)
 - Informacja od klienta o nieprawidłowości zamówienia;
 - Zaksięgowanie reklamacji w systemie;
 - Poinformowanie punktu gastronomicznego;
 - Informacja zwrotna z punktu gastronomicznego o uznaniu reklamacji;
 - Informacja do klienta o uznaniu reklamacji.

VI. DEKOMPOZYCJA PROCESÓW ZARZĄDZANIA Oznaczenia modułów systemu: 44

M1 - zamówienia;

M2-dostawa;

M3 – finanse;

M4 – marketing;

M5 – sprzedaż;

M6 – analiza;

M7-obsługa klienta (support);

M8 – zniżka.

Definicja operacji systemowych:

D1.M1 – Zarejestrowanie zamówienia w systemie;

D1.M4 – Sprawdzenie czy trwa aktualnie kampania promocyjna na wybrany przez klienta produkt;

D1.M8 – Sprawdzenie czy dany klient jest uprawniony do rabatu i automatyczne przyznanie mu go;

D2.M1 – Otrzymanie informacji zwrotnej;

D3.M3 – Zaksięgowanie transakcji;

D3.M5 – Przesłanie zamówienia do punktu gastronomicznego, z którego klient wybrał zamówienie;

D3.M6 – Przesłanie danych do analizy;

D4.M1 – Otrzymanie informacji od punktu gastronomicznego;

D5.M2 – Powiadomienie klienta o czasie trwania dostawy;

D6.M4 – Opracowanie strategii promocyjnej;

D7.M1 – Ujęcie promocyjnych cen w systemie;

D8.M3 - Udokumentowanie promocji;

D9.M6 – Zebranie wyników do analiz w czasie trwania promocji i ocena promocji;

D10.M7 – Informacja od klienta o nieprawidłowości zamówienia;

D11.M1 – Zaksięgowanie reklamacji w systemie;

D12.M5 – Poinformowanie punktu gastronomicznego;

D13.M1 – Informacja zwrotna z punktu gastronomicznego o uznaniu reklamacji;

D14.M7 - Informacja do klienta o uznaniu reklamacji.

VII. PODSUMOWANIE

W oparciu o opracowane metody wizualizacji przebiegu funkcjonowania złożonych systemów zarządzania warunkach kooperacji sektorowej określono podstawy symulacji, które pozwoliły na prezentacje przebiegu procesów umożliwiły zarządzanie i systemem informacyjnym w czasie rzeczywistym. Opracowany materiał jest zintegrowaną częścią publikacji [2], która przedstawia metody oraz technikę wizualizacji procesów zarządzania, która z kolei pozwala usunąć barierę psychologiczną i uniknąć wzajemnego nieporozumienia między klientem i twórcą systemów informatycznych a także zmniejszyć koszty opracowania, wdrażania i obsługi rozproszonych systemów zarządzania.

Osiągnięto cel projektu, jakim była analiza procesowa systemu zarządzania portalem gastronomicznym. Dokonano dekompozycji systemu na podstawie analizy procesów zachodzących w rzeczywistości. Dzięki wdrożeniu systemu można zoptymalizować koszty, poprawić jakość obsługi oraz zautomatyzować procesy dostawy produkcji.

Wdrożenie opracowanego systemu pozwoliło na usprawnienie wymiany informacji między oddzielnymi jednostkami i przejście na elektroniczny system zarządzania. Wdrażanie zmian w systemie spowodowało wzrost konkurencyjności firmy, a funkcjonalność systemu dostosowano do standardów rynkowych.

LITERATURA REFERENCES

- [1] Л. Петришин, Я. Николайчук, Аналитическое моделирование информационных систем автоматизированного управления – Analytical modeling of infosystems of automated management. / Lyubomyr Petryshyn // Zarządzanie organizacjami w gospodarce rynkowej: X międzynarodowa naukowa konferencja "Zarządzanie przedsiębiorstwem. Teoria i praktyka": Kraków, 22-23 listopada 2007 г. / pod red. Wiesława Waszkielewicza; — Kraków: Wydawnictwa AGH, 2007. — ISBN 978-83-7464-153-1 — S. 268– 275. — Bibliogr. s. 338, Abstr.
- [2] L. Petryshyn, W. Cieslik, M. Petryshyn. Visualization Modeling of Networks Management Systems. II International Scientific and Practical Conference "Theoretical and Applied Aspects of Device Development on Microcontrollers and FPGAS" MC&FPGA-2020: Kharkiv, June 25-26, 2020. – Kharkiv, KhNURE, 2020, Ukraine. In press.

45

DOI: 10.35598/mcfpga.2020.014

Visualization Modeling of Networks Management Systems

Lubomyr Petryshyn dept. of Enterprise Management AGH University of Science and Technology Cracow, Poland l.b.petryshyn@gmail.com ORCID: 0000-0003-4168-3891 Wioleta Cieslik dept. of Computer Science AGH University of Science and Technology Cracow, Poland w.cieslik@gmail.com Mykhailo Petryshyn dept. of Computer Science and Information Systems Precarpathian National University Ivano-Frankivsk, Ukraine m.l.petryshyn@gmail.com ORCID: 0000-0001-6319-3768

Wizualizacyjne Modelowanie Sieciowych Systemów Zarządzania

Lubomyr Petryshyn kat. Zarządzania Przedsiębiorstwem AGH University of Science and Technology Kraków, Polska l.b.petryshyn@gmail.com ORCID: 0000-0003-4168-3891 Wioleta Cieślik kat. Informatyki Stosowanej AGH University of Science and Technology Kraków, Polska w.cieslik@gmail.com Mykhailo Petryshyn kat. Nauk Komputerowych i Systemów Informatycznych Precarpathian National University Ivano-Frankivsk, Ukraina m.l.petryshyn@gmail.com ORCID: 0000-0001-6319-3768

procesów Adnotacja—Modelowanie zarządzania w warunkach kooperacji sektorowej na podstawie rozproszonych systemów informatycznych pozwala zmniejszyć koszty opracowania i eksploatacji takich złożonych systemów. Proponowana metoda wizualizacji modeli informacyjnych pozwala na odwzorowanie w formie graficznej procesów i upraszcza porozumienie się na etapie analizy i projektowania pomiedzy zleceniodawcą a producentem systemu. Przedstawiono podstawy modelowania wizualizacyjnego i uproszczony przykład opracowania systemu wielosektorowego zarządzania siecią dostaw produkcji.

Słowa kluczowe—modelowanie wizualizacyjne, procesy informacyjne, kooperacja sektorowa, systemy rozproszone, zarządzanie

Abstract—Simulation of the processes of sectoral cooperation management in distributed information systems allows to reduce the means of introduction and operation of such complex systems. The proposed method of visualization of information models reflects graphically the constituent processes and simplifies the understanding at the stage of analysis and design between the customer and the system developer. The basics of visualization modeling and simplified example of models development of multi-sectoral management system are presented.

Keywords—visualization modeling, information processes, sectoral cooperation, distributed systems, management

I. WSTĘP

Zarządzanie złożonymi systemami w warunkach kooperacji sektorowej wymaga zastosowania technologii informacyjnej, która zapewnia odwzorowanie stanu i umożliwia zarządzanie systemem w czasie rzeczywistym. Opracowany materiał jest zintegrowaną częścią publikacji [1], która przedstawia technikę analizy procesowej w zarządzaniu, będącej z kolei podstawą modelowania Wizualizacja informacyjnego. procesów zarządzania pozwala na usunięcie bariery psychologicznej i uniknięcie nieporozumienia pomiędzy klientem i twórcą systemów informatycznych, a także pozwala zmniejszyć koszty opracowania, wdrażania i obsługi takich złożonych systemów.

Celem opracowania jest przedstawienie wizualnych metod modelowania procesów zarządzania złożonymi systemami w warunkach kooperacji sektorowej, a także opracowanie uproszczonego przykładu systemu zarządzania firmą.

Nowacją pracy jest opracowanie i przedstawienie graficznych metod modelowania, które zapewniają wizualizację procesów zarządzania i upraszczają zrozumienie ich przepływu.

Aspekt praktyczny polega na możliwości odwzorowania struktury i przepływu procesów zarządzania, unikania nieporozumień przy formułowaniu zadania i zapewniania wymagań klienta, a także zmniejszania kosztów tworzenia i eksploatacji systemów zarządzania.

Podstawy modelowania wizualizacyjnego są opublikowane w [2]. Przeanalizujemy uproszczony przykład modelowania rozproszonego systemu zarządzania siecią sprzedaży produkcji z punktów gastronomicznych w skali kraju w celu usprawnienia i ułatwienia potencjalnemu klientowi wyboru konkretnego zamówienia wg jego potrzeb

II International Scientific and Practical Conference Theoretical and Applied Aspects of Device Development on Microcontrollers and FPGAs



w danej chwili. Innym aspektem jest wypromowanie początkujące punktów gastronomicznych i poszerzenie oferty sprzedażowej tych, które już prosperują na rynku. Na podstawie analizy procesowej oraz dekompozycji systemu zarządzania [1] przeprowadzimy modelowanie informacyjne systemu.

II. MODELOWANIE PROCESÓW ZARZĄDZANIA

System zarządzania pozostał zdekomponowany na następujące jednostki organizacyjno-strukturalne: M1 – dział zamówienia; M2 – dział dostaw; M3 – dział finansów; M4 – dział marketingu; M5 – dział sprzedaż; M6 – dział analityczny; M7 – dział obsługi klienta (support); M8 – dział zniżek.

Wynikiem dekompozycji procesów systemu zarządzania [1] jest definicja następujących operacji systemowych:

D1.M1 – Zarejestrowanie zamówienia w systemie;

D1.M4 – Sprawdzenie czy trwa aktualnie kampania promocyjna na wybrany przez klienta produkt;

D1.M8 – Sprawdzenie czy dany klient jest uprawniony do rabatu i automatyczne przyznanie mu go;

D2.M1 – Otrzymanie informacji zwrotnej;

D3.M3 – Zaksięgowanie transakcji;

D3.M5 – Przesłanie zamówienia do punktu gastronomicznego, z którego klient wybrał zamówienie;

D3.M6 – Przesłanie danych do analizy;

D4.M1 – Otrzymanie informacji od punktu gastronomicznego;

D5.M2-Powiadomienie klienta o czasie trwania dostawy;

D6.M4 – Opracowanie strategii promocyjnej;

D7.M1 – Ujęcie promocyjnych cen w systemie;

D8.M3 – Udokumentowanie promocji;

D9.M6 – Zebranie wyników do analiz w czasie trwania promocji i ocena promocji;

D10.M7 – Informacja od klienta o nieprawidłowości zamówienia;

D11.M1 – Zaksięgowanie reklamacji w systemie;

D12.M5 – Poinformowanie punktu gastronomicznego;

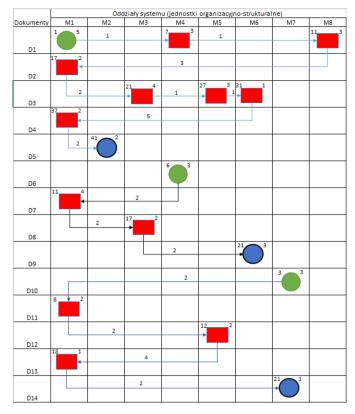
D13.M1 – Informacja zwrotna z punktu gastronomicznego o uznaniu reklamacji;

D14.M7 - Informacja do klienta o uznaniu reklamacji.

Wymienione operacje systemowe są uporządkowane w procesie zarządzania wg następujących modelów graficznych.

A. Model matrycowy

Model matrycowy procesu zarządzania całego systemu zawiera trzy podprocesy (rys. 2): realizację zamówienia, promocję i złożenie zażalenia przez klienta (przypadek uznania). Taki model pozwala na wizualizację postępu realizacji operacji systemowych w procesach przedsiębiorstwa, wykonywanych w odpowiednich jednostkach w skali czasu.



Rys. 1. Model matrycowy systemu zarządzania.

Na rys. 2: • - źródło informacji; • - przetwarzanie informacji; • - odbiór informacji.

B. Tablice czasowe

Tablice czasowe zawierają czasy rozpoczęcia, formowania, przetwarzania oraz ustalenia przetwarzania oraz przepływów operacji systemowych.

Tablice czasowe określają rozkład w skali czasu poszczególnych systemowych operacji procesów. Tabl. I przedstawia czasy rozpoczęcia, tworzenia, i ustalania operacji systemowych. przetwarzania Natomiast tabl. II pokazuje czasy przekazania dokumentów przy wykonaniu operacji systemowych.

C. Model "graf sieciowy"

Model graf sieciowy (rys. 3) jest podstawowym modelem, który umożliwia przejście do UML-modelowania i przedstawia podstawowe parametry systemu takie jak struktura, czas rozpoczęcia i trwania operacji systemowych oraz połączenie kanałów komunikacyjnych.

D. Model czasowy spójny

Aby ocenić pełne obciążenie obliczeniowe informatycznego systemu zarządzania stosuję się spójny model czasowy (rys. 4). Graf ten jednak nie uwzględnia działów, w jakich wykonują się poszczególne operacje systemowe.

						NIA DOKUMENTÓ ACJI SYSTEMOWY				
Dokumenty	Rozpoczęcia Formowania		Przetwa- rzania	Ustalania		Dokumenty			Czas przekazania	
D1.M1	1	5				D1.M1-D	1.M4	-	1	
D6.M4						D1.M4- D	1.M8		1	
	6	3				D1.M8 - D			3	
		_				D2.M1 - D			2	
D10.M7	3	3				D3.M3 - D3.M5		1		
D10.M7 D1.M4	7	5	3					1		
D1.M4	11		3			D3.M5 - D3.M6				
D1.M0	17		2			D3.M6 - D4.M1		5		
D3.M3	21		4			D4.M1 - D5.M2		2		
D3.M5	27		3			D6.M4 - D7.M1		2		
D3.M6	31		1			D7.M1 - D8.M3		2		
D4.M1	37		2			D8.M3 - D9.M6		2		
D7.M1	11		4			D10.M7 - D11.M1		2		
D8.M3	17		2			D11.M1 - D12.M5		2		
D11.M1	8		2			D12.M5 - D13.M1		4		
D12.M5	12		2			D13.M1 - D14.M7		2		
D13.M1 D5.M2	18 41		1	2		D15.M1 - L	/14.1/1		Z	
D5.M2 D9.M6	21			3						
D9.M6 D14.M6	21			1						
D1.M1	D6,M4	, D13.M1, D7,	M1	02.M1 032.M1 08.M9	D3.M3			M6		
	5	10	M8	20		25	30	35	40	

TABLICA I. CZASY WYKONANIA OPERACJI SYSTEMOWYCH

Rys. 2. Model "graf sieciowy" (typu Gantta).

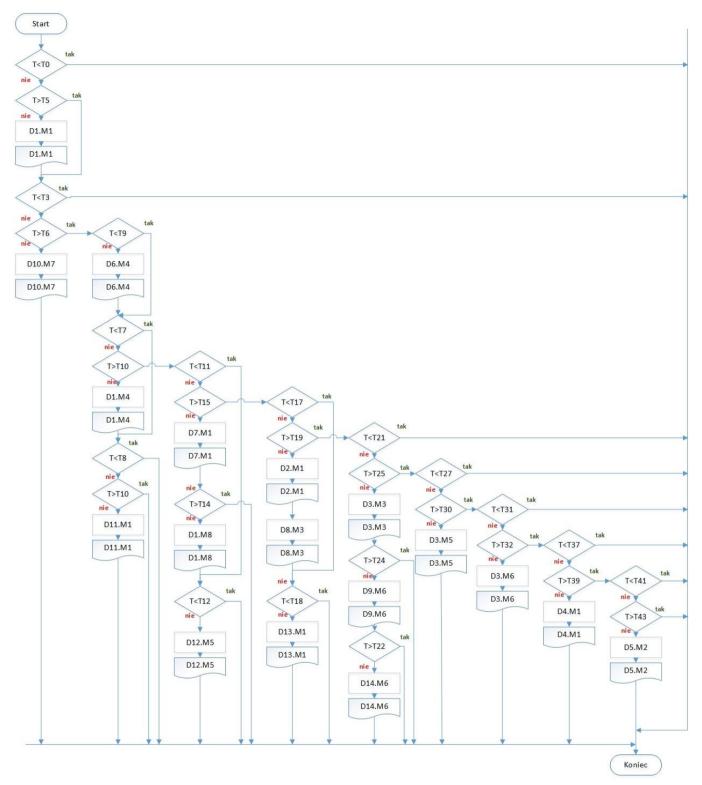
D1.M1	in the second	01.144	D1.M8	82 MI	D3.M3	D3.M5	ме	D4.M1	D5.M2
		D6.M4	D7.M1	D8.MB	D9.M6				
	D10.M7	D11.M1	D12.WS	DI3.M1	D14.M6				
	1	The second se	342				8		1 3
	5	10	15	20	25	30	35	40	45

Rys. 3. Model czasowy spójny wykonania operacji systemowych.

E. Schemat błokowy algorytmu wykonania operacji systemowych

Na podstawie modelu spójnego wykresu czasowego pozostał opracowany schemat blokowy algorytmu programu

wykonania operacji systemowych (rys. 5), który na podstawie programowania obiektowego umożliwia szybką implementację i wdrożenie oprogramowania aplikacyjnego.

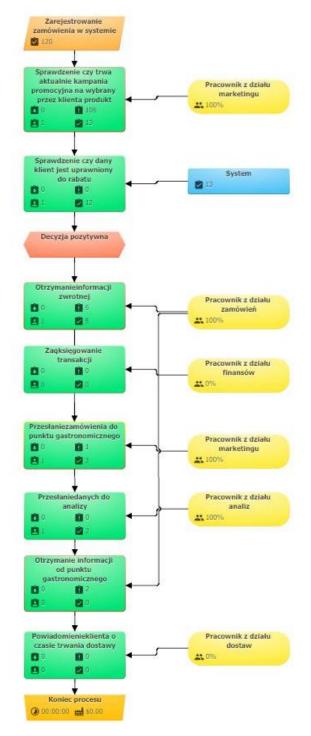


Rys. 4. Schemat blokowy algorytmu wykonania operacji systemowych.

MC&FPGA-2020

III. SYMULACJA PROCESÓW W MODELOWANYM SYSTEMIE

Symulację procesową przeprowadzono za pomocą online programu BPSimulator, znajdującego się na stronie <u>http://www.bpsimulator.com</u> [2]. Poniżej znajduje się model użyty do symulacji (rys. 6) oraz raport z niego wygenerowany (rys. 7). Symulacja pozwoliła oszacować koszty systemu i pokazać średni czas realizacji każdego procesu.



Rys. 5. . Model symulacji systemu zarządzania.



Rys. 6. Raport symulacji obciążenia informatycznego systemu zarządzania.

IV. PODSUMOWANIE

W oparciu o opracowane metody wizualizacji przebiegu funkcionowania złożonych systemów zarządzania w warunkach kooperacji sektorowej określono podstawy symulacji, które pozwoliły na prezentacje przebiegu i umożliwiły zarządzanie procesów systemem informacyjnym w czasie rzeczywistym. Wizualizacja procesów zarządzania pozwoliła usunać bariere psychologiczną i uniknąć wzajemnego nieporozumienia między klientem a twórcą systemów informatycznych a także zmniejszyć koszty opracowywania, wdrażania i obsługi rozproszonych systemów zarządzania.

Osiągnięto cel projektu, jakim było modelowanie systemu obsługi portalu gastronomicznego. Dokonano modelowania systemu na podstawie procesów zachodzących w rzeczywistości. Dzięki wdrożeniu systemu można zoptymalizować koszty, poprawić jakość obsługi oraz zautomatyzować procesy dostawy produkcji.

Wdrożenie opracowanego systemu pozwoliło na usprawnienie wymiany informacji między oddzielnymi jednostkami i przejście na elektroniczny system zarządzania. Wdrażanie zmian w systemie spowodowało wzrost konkurencyjności firmy, a funkcjonalność systemu dostosowano do standardów rynkowych.

LITERATURA REFERENCES

- L. Petryshyn, W. Cieslik, M. Petryshyn. Processes Analysis of Networks Management Systems. II International Scientific and Practical Conference "Theoretical and Applied Aspects of Device Development on Microcontrollers and FPGAS" MC&FPGA-2020: Kharkiv, June 25-26, 2020. – Kharkiv, KhNURE, 2020, Ukraine. In press.
- [2] Л. Петришин, Я. Николайчук, Аналитическое моделирование информационных систем автоматизированного управления – Analytical modeling of infosystems of automated management. / Lyubomyr Petryshyn // Zarządzanie organizacjami w gospodarce rynkowej: X międzynarodowa naukowa konferencja "Zarządzanie przedsiębiorstwem. Teoria i praktyka": Kraków, 22-23 listopada 2007 г. / pod red. Wiesława Waszkielewicza; — Kraków: Wydawnictwa AGH, 2007. — ISBN 978-83-7464-153-1 — S. 268– 275. — Bibliogr. s. 338, Abstr.
- [3] BP Simulator. [Online]. Available: https://www.bpsimulator.com/run/ july 09, 2019.

Distance Training of Higher Education Specialists Using Virtual Presence Technologies

Valerii Semenets ORCID 0000-0001-8969-2143 Department of Metrology and Technical Expertise Kharkiv National University of Radio Electronics Kharkiv, Ukraine valery.semenets@nure.ua

Evgen Chuguy ORCID 0000-0001-5028-7968 Department of Biomedical Engineering Kharkiv National University of Radio Electronics Kharkiv, Ukraine evgen.chuhuy@nure.ua Oleg Avrunin 0000-0002-6312-687X Department of Biomedical Engineering Kharkiv National University of Radio Electronics Kharkiv, Ukraine oleh.avrunin@nure.ua

Yana Nosova ORCID 0000-0003-4310-5833 Department of Biomedical Engineering Kharkiv National University of Radio Electronics Kharkiv, Ukraine yana.nosova@nure.ua

Abstract—The technologies of creating modern educational content based on video with the effect of presence are considered. The features of the technology for creating a modern panoramic video and examples useful for creating educational content in different fields are given.

Keywords—high resolution, educational process, panoramic video, viewing angle, situational problems

I. INTRODUCTION

Modern requirements for the development of disciplines and the results of the final training of modern university graduates are based on the formation of competencies integrated characteristics aimed at developing the ability to combine the acquired knowledge, abilities and skills into a single whole to achieve the goal, taking into account the context, specific situation and functionality. At the same time, the drawbacks of traditional training at present are the formality of the knowledge gained and the insufficient ability to apply their practical activity, which generally indicates the incomplete formation of professional thinking, which is absolutely necessary with a modern approach to employment [1-2].

Modern challenges associated, for example, with the pandemic of the COVID-2019 virus, and the necessary strict measures of long-term total quarantine in an emergency situation, lead to a complete reorientation to distance learning methods, which from the auxiliary become the main ones throughout the teaching cycle of most disciplines. Therefore, along with the possibilities of placing electronic educational materials with presentations, calculations and tests, as well as organizing interactive interaction with students in video conferencing modes, it is necessary to provide the educational process with the most realistic content available for distance learning services. Video content based on panoramic video technologies can become such content at the present stage. Tatyana Nosova ORCID 0000-0003-4442-8001 Department of Biomedical Engineering Kharkiv National University of Radio Electronics Kharkiv, Ukraine tatyana.nosova@nure.ua

Oleksandr Gryshkov ORCID 0000-0002-3116-8792 Institute for Multiphase Processes Leibniz University of Hannover Hannover, Germany gryshkov@imp.uni-hannover.de

The widespread use of panoramic video technology appeared only a few years ago. Panoramic refers to video with viewing angles in the horizontal 360 ° and vertical 180 ° planes, respectively. Thanks to these viewing angles, such a video is also called spherical. Moreover, in most viewing programs, the user can change the viewing angle interactively using manipulators or touch screen systems. Modern panoramic cameras, as a rule, have two wide-angle (over 180°) lenses overlapping each other. There are models with a large number of standard lenses, for example: 6 (Insta 360 evo) (Fig.1), 8 (VUZE 360) and even 24 (Surround \times 24). The advantage of multi-lens models is a smaller number of geometric distortions compared to the image formed by wide-angle lenses, however, there is a greater likelihood of artifacts from combining images formed by different cameras and differences in illumination may occur [3-5].



Fig. 1. Panoramic camera Insta 360 evo.

In fact, to obtain panoramic video, the device registers video streams from different cameras, and then combines them - the so-called "stitching" (Fig.2).

Compared to traditional ones, panoramic videos take up a large amount, which is associated not only with an increase in visibility, but also due to, as a rule, high resolution, for example, 4K (3840×1920), 5.7K (5760×2880) and 8K (7680x4320) at a frequency of not less than 30 frames per second. For example, when working with an Insta360 EVO

device that has 2 recording cameras with wide-angle lenses (with a viewing angle of 200 °), 2 * .insv files from each camera are formed, which are then programmatically converted to a panoramic video file in * .mp4 format. So, a 9-second panoramic video with a resolution of 5K in * .mp4 format occupies 149 MB with the size of two * .insv files of 65 MB each; A 27-second panoramic video in the resolution of 1600 * 800 in the * .mp4 format occupies 420 MB with the size of two * .insv files of 169 MB each; A 7-second panoramic video in low resolution 800 * 400 in * .mp4 format occupies 40 MB with the size of two * .insv files of 60 MB each. You can view this content right away from your smartphone with the help of a specialized Holo Frame screen cover, 3D glasses, as well as standard virtual reality glasses (Oculus Go, Samsung Gear VR, etc.).



Fig. 2. Frame reversal training video 360.

It should be recognized that lowering the resolution below Full HD (1920×1080), or close to it, significantly degrades the image quality and does not allow to fully realize the effects of scaling. Given the prospects for technology development, at the present stage it is advisable to use the resulting video with a resolution close to 4K (3840×1920).

Panoramic view, interactive control and high resolution allow you to realize the key advantage of such a panoramic video - the effect of presence. Given that expensive equipment is often used in medicine, access to which is limited for development [6-7], as well as various new approaches and methods, for example, in surgical treatment [8], which must be demonstrated in order to acquire practical skills [9], it is advisable to use panoramic educational video content for these purposes.

Also, it is advisable for conducting laboratory workshops in technical disciplines [6-7], where students need to get the most out of the real work of not only one device, but, in some cases, a whole complex of complex equipment [10-12].

Even when listening to a standard lecture, or shooting a video of a practice lesson, an interactive panoramic video allows you to create the effect of being in the audience, which is very important for a long distance learning form, when for a long time the possibility of real communication and being in the audience is lost.

II. USING A VIDEO WITH A PRESENCE EFFECT

For several decades, information technology has been actively used in training. At the same time, a huge number of approaches for distance learning have been proposed, ranging from digitized training materials, video lectures, and test programs [13,14], to the organization of video conferencing, interactive courses and modeling of typical situations using virtual reality tools [15-16]. In medicine, such technologies make it possible to solve situational problems with virtual patients and simulate surgical operations with maximum realism, while training engineers to remotely perform laboratory work not only using virtual equipment, but also on real equipment using interactive systems with feedback.

Despite the fact that a sufficient number of distance learning courses have been developed and applied throughout the world in various fields of knowledge, until now, in the classical university educational process, these technologies have been only a kind of high-tech support for traditional teaching methods and have been used mainly only to further consolidate practical skills, or with independent work of students.

III. SITUATIONAL TASKS

A special role in the educational process when acquiring practical skills is brought by the solution of situational problems, which allow creating conditions as close as possible to real tasks and circumstances. Such a concept for learning is realized by describing a real situation that needs to be resolved by answering, in the simplest case, a list of issues of a problematic nature, or by completing a series of tasks that characterize the effectiveness of the knowledge used and the chosen approach.

This may be the determination of a malfunction of a device or system in engineering, the diagnosis and determination of adequate therapy for a patient in medicine, the solution of real-life problems in other areas. In the process of solving situational problems, such universal methods of working with information are formed as analysis, classification, recognition, structuring, generalization, comparison, search for analogies, choice of options, and synthesis of new knowledge. This approach has a clear practical orientation and allows you to implement the skills acquired in the learning process and the above to work in a real situation.

The simplest and most traditional way of presenting situational tasks is their textual description. Given the features of the perception of information, especially among modern students who are accustomed to rely more on visual images in the world of digital gadgets, this approach, unfortunately, does not fully ensure immersion in the real task.

In addition, in many areas it is precisely a comprehensive assessment of information from various sources. To increase the effectiveness of such an approach, increase the reliability and make the created situation more realistic, it is advisable to develop content that allows maximum approximation to the real environment. To do this, it is necessary to use approaches with a high level of interactivity, created on the basis of virtual reality technologies [1], panoramic video [2], which make it possible for a modern student to interest and transfer the solution of a situational problem from a routine training task to the most realistic environment with which you can interact and get additional information that minimally limits the creative activity of the student.

II International Scientific and Technical Conference Theoretical and Applied Aspects of Device Development on Microcontrollers and FPGAs Only immersion in the environment with the help of carefully thought-out interactive video content with the effect of presence allows you to fully use the mechanisms of mental activity to make decisions and develop practical skills in solving situational problems. This allows you to take a illustration of the event to a new level; actualization of the problem and requires a whole range of measures and the development of appropriate methodological material to create a realistic virtual environment that adequately simulates typical situations. It is advisable to apply approaches to creating virtual patients in medicine, a virtual laboratory base [3, 4] with the technical focus of training.

The main goal of situational tasks is to develop the competencies and skills necessary to solve practical problems. And in the first place is the creation of quality content that simulates the environment in the context of which the task arises. All aspects of integrative approaches to learning are clearly manifested here, which allows us to develop and produce new ones based on the previously acquired comprehensive knowledge and skills.

IV. CONCLUTION

The widespread introduction of situational tasks allows us to transfer the educational process at universities in advanced courses to a qualitatively new level, which allows us to acquire practical knowledge and to model the ability to make responsible decisions. This, in turn, increases the interest and self-esteem of students, and develops their willingness to act in real situations, which is taken into account in employment.

When using panoramic content, the student, while at home, has the opportunity to see what is in the classroom in the appropriate directions, either by standard means of personal computers, or by mobile phone or tablet (moving his gadget to the side). Thus, the student has the opportunity to observe the teacher at the same time, which, for example, explains the laboratory work at the study layout, the presentation of control commands and data processing on the monitor screen, supporting materials, such as displayed on the board, additional equipment and by the reaction of classmates next to him in the audience.

Despite the fact that it takes a lot of time to create really high-quality educational panoramic content, it allows to increase the efficiency of the educational process, especially in quarantine, and promotes social adaptation of people with special educational needs in the implementation of inclusive education. Panoramic video technologies allow you to take training videos to a whole new level, providing an almost full-fledged presence effect for the student, allowing you to interactively change the angle of view and observe the manipulations in all directions of the space available for viewing. The prospect of work is the creation of virtual laboratories and panoramic video-content of complete research based on the laboratories of NIFE and IMP which situated in the Leibniz University of Hannover.

ACKNOWLEDGMENT

The exchange program with East European Countries funded by DAAD (Ostpartnerschaften, project number 54364768) and joint Ukraine-Germany project MESU-BMBF 2019-2020 "3D-Model – Implementation of rapid prototyping to design and model the upper respiratory tract in normal and typical pathologies"

REFERENCES

- V. Kobzev, V. Semenets and V. Filatov, "Components of the information system for monitoring the quality of education in Kharkov National University of Radio Electronics", in 7th Int. scientific and technical conf. Information systems and technologies (IST-2018), Kharkiv-Koblevo, 2018, pp. 51-54.
- [2] V. Semenets, I. Svyd and L. Saikivska, "Methods of improving the quality of preparation of technical specialists", in Engineering education: challendes and developments : materials of the IX International Scientific and Methodological Conference, Minsk, Belarus, 2018, pp. 415-416.
- [3] Iorns, Thomas, and Taehyun Rhee. "Real-time image based lighting for 360-degree panoramic video." Image and Video Technology. Springer, Cham, 2015.
- [4] Youvalari, Ramin Ghaznavi, et al. "Efficient coding of 360-degree pseudo-cylindrical panoramic video for virtual reality applications." 2016 IEEE International Symposium on Multimedia (ISM). IEEE, 2016.
- [5] Kwon, Oh-Seol, and Yeong-Ho Ha. "Panoramic video using scaleinvariant feature transform with embedded color-invariant values." IEEE transactions on Consumer Electronics 56.2 (2010): 792-798.
- [6] O. Avrunin, O. Kruk, T. Nosova and V. Semenets, "Technical aspects of the development of virtual laboratory works on technical educational disciplines", Open Education, vol. 3, pp. 11-17, 2008.
- [7] O. Avrunin, S. Sakalo and V. Semenetc, "Development of up-to-date laboratory base for microprocessor systems investigation," 2009 19th International Crimean Conference Microwave & Telecommunication Technology, Sevastopol, 2009, pp. 301-302.
- [8] Gubanov, A. V., Zhemchuzhkina, T. V., Nosova, T. V., & Nosova, Y. V. (2014). Electromyographic data processing module 5th International radio electronic forum «Applied electronics. Status and Development Trends», Conference «Problems of Biomed Engineering. Science and Technology, 3, 25-27.
- [9] Nosova, Ya V., Kh I. Faruk, and O. G. Avrunin. "A tool for researching respiratory and olfaction disorders." Telecommunications and Radio Engineering 77.15 (2018): 1389-1395.
- [10] Avrunin, O. "Development of Automated System for Video Intermatoscopy/OG Avrunin, V. Klymenko, A. Trubitcin, O. Isaeva." Proceedings of the IX International Scientific and Practical Conference International Trends in Science and Technology. Vol. 2. 2019.
- [11] Avrunin, O., Ya Nosova, and S. Khuadaieva. "Features of creation technologies for educational panoramic video content." Modern approaches to the introduction of science into practice. Abstracts of X International Scientific and Practical Conference. San Francisco, USA 2020. Pp.256-259.
- [12] Nosova, Y., I. Younouss Abdelhamid, and O. Gryshkov. "Using 3D printing technology to full-scale simulation of the upper respiratory tract." Informatyka, Automatyka, Pomiary W Gospodarce I Ochronie Środowiska, Vol. 9, no. 4, Dec. 2019, pp. 60-63, doi:10.35784 / iapgos.681.
- [13] Saghir, Ali. "Influence of Vidio Games in Learning." Journal of Emerging Trends in Computing and Information Sciences 7.8 (2016): 338-342.
- [14] I. Tarasov. Organization of the educational process in the design of digital devices using an initial level based boards FPGA Spartan-6 company Xilinx. Components and Technologies, 2011,12, pp.10-14.
- [15] V. Semenets, V. Kauk, O. Avrunin. "The advanced technology of remote training at the initial process" ["Vprovadjennya tehnologiy dystantsiynogo navchannya u navchalnii protses"], High School, 2009. – No. 5. – P. 40–45.
- [16] Avrunin, Oleg G., T. Nosova, and V. Semenets. "Experience of Developing a Laboratory Base for the Study of Modern Microprocessor Systems." Proceedings of I International Scientific and Practical Conference "Theoretical and Applied Aspects of Device Development on Microcontrollers and FPGAs" MC&FPGA-2019, Kharkiv, Ukraine, 2019. P. 6–8.

II International Scientific and Technical Conference Theoretical and Applied Aspects of Device Development on Microcontrollers and FPGAs

3D Printing in Online Education

Hanna Zavolodko ORCID 0000-0003-0000-8910 dept. System and Information . VO . Kravets NTU " HPI " Kharkiv ann.zavolodko@gmail.com

Abstract—The review object is the subsystem verification and printing 3D-model online learning system mixed type. To do this, a review of analogues, technologies, stages of printing were identified. The aim is to design with IP topics that uses the additive technologies in the educational process. In the given IDEF - diagram describing the function of the system; authentication rules, verification of 3D-models, sending the model to print, selecting a device online, and basic screen forms.

Keywords—additive technologies, blended learning, 3d-model, 3d-printing, rules database, database.

I. INTRODUCTION

With the development of technology, new requirements for learning appear and the educational process is transformed Education uses blended learning, part of which is distance learning. The use of additive technologies allows to make the modeling process more meaningful and progressive. Thus, if distance education is the ability to develop a 3D model online and check its loyalty, it optimizes the learning process. [1-5].

II. USING 3D PRINTING DURING ONLINE LEARNING

Learning – the process of transferring knowledge, skills and abilities from teacher to student. To date, there are fulltime, distance and online - learning. They all use interactive tools. Interactive learning - the use of technical means to organize joint activities of students and teachers in order to maintain knowledge, skills and abilities. Distance learning remote independent learning of a student with the use of technical means. Teacher functions - checking the student's work and communicating with the student through forums and chats. Online learning - virtualization of face-to-face learning using interactive tools.

In cooperation with the international project "dComFra -Digital competence framework for Ukrainian teachers and other citizens / dComFra (No. 598236-EPP-1-2018-1-LT-EPPKA2-CBHE-SP)" a framework of digital competencies for different segments of the population was developed . Today, being competent in the digital field means that the citizen must have competencies in all areas of DigComp. The Digital Competence Framework can help with selfassessment, defining learning goals, identifying learning opportunities, and facilitating job search. In many areas of modern and future professions, the ability to develop a 3D model online and check its accuracy, send the model to print is a necessary task. Nataliia Haidar dept. System and Information . VO . Kravets NTU " HPI " Kharkiv nata.haydar.nh@gmail.com

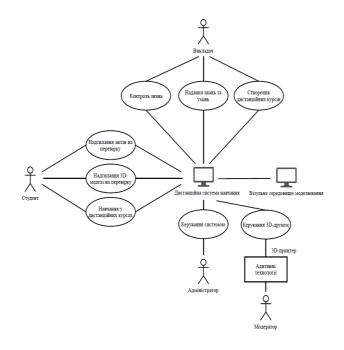


Fig. 1. Block diagram of the relationship of objects.

In a remote system that uses additive technologies, it is possible under the supervision of a moderator and a teacher to perform the functions of checking the 3D model and sending to print [6].

This approach will allow the use of modern devices in distance learning.

Based on the analysis of existing solutions, the stages of 3D printing were identified - the creation of a digital model [7] export of 3D model in STL format, G-code generation, preparation of 3D printer, 3D model printing and finishing of the object.

In general, the system model can be represented using the IDEFO methodology, in which the input data is a formalized task, the mechanism is an analyst, the control mechanisms are 3D modeling technologies and printing standards. And at the output the result is a printed model.

The first two levels covered by the system (see Figure 2) are performed in the simulation tools and sent to the system for verification. Validation of the 3D model involves the

division into stages, for which the input data can be developed model.

Thanks to modeling technologies, a digital model is created. Such a model must also meet printing standards. Then the model is sent for printing.

The simulated system uses a base of rules based on a production model of knowledge representation.

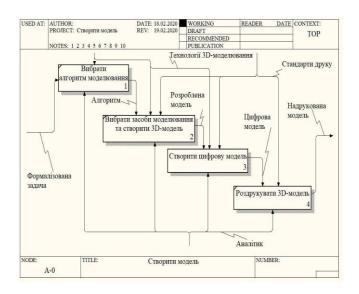


Fig. 2. Simulation algorithm.

Types and subtypes of rules were identified for the correct operation of the system.

For each type of rule, there is a subtype that defines the rules that are involved at a particular stage and are needed for validation.

A file with a 3D model is fed to the input model in the unit for checking the compliance of the additive model. The model is checked by the teacher.

To check, we use the rules that are in the database of rules, which are provided to the teacher in the form of a web page.

If, as a result of checking 3D model validation rules, the model does not meet the requirements, the process exits and the user is sent an error message.

If as a result of checking the rules such as "send the model to print" all the rules are met, the model is passed on to print, if not - the process is completed and users are notified.

In the unit for checking the selection of the print device, a model file that has already been previously tested for 3D model requirements is fed at the input.

After the user selects the desired device, it is checked whether the selected device meets the requirements for 3D printing. If so - the model is sent for printing, if not - printing is not allowed and the corresponding message is sent to the user.

III. CONCLUTION

The development of innovative thinking in students should become a priority of modern education [8, 9], and the introduction of new elements in modern learning is inevitable. And given the development of 3D-printing technologies, JSCs are the most promising for the application of visualization in pedagogical activities of online learners and blended learning.

REFERENCES

- Lipnitski L.A., Pilgun T.V. Additive technologies and their perspectives in education. «System analysis and applied information science». 2018;(3):76-82. (In Russ)
- [2] M. Palinchak and V. Yzheshchuk, "Basic models of food education in the context of political ideology of the European Union", Geopolitics of Ukraine: history and modernity, vol. 0, no. 219, pp. 108-123, 2017. doi: 10.24144 / 2078-1431.2017.2 (19) .108-123.
- [3] I. Pavlova and E. Tarasova, "The role of modern innovative technologies in the educational process", International Journal of Advanced Studies, vol. 8, no. 3, p. 61, 2018. doi: 10.12731 / 2227-930x-2018-3-61-78.
- [4] V. Povzun, "The role of the modern educational technologies in the development of system thinking of university students", Contemporary Higher Education: Innovative Aspects / Sovremennaia Vysshaia Shkola: Innovatsionny Aspect . Dec 2019, Vol. 11 Issue 4, p. 45-51, 2019. doi: 10.7442/2071-9620-2019-11-4-45-51.
- [5] C. Vorotnikova, "Application of modern information technologies in the educational process", european humanities studies: state and society, vol. 3, no., pp. 43-51, 2019. doi: 10.38014/ehs-ss.2019.3-i.04.
- [6] I Gibson I., Rosen D. W., Strucker B. Additive Manufacturing Technologies. Rapid Prototyping to Direct Digital Manufacturing. Springer, 2010. 459 p.
- [7] I. Ituarte, N. Boddeti, V. Hassani, M. Dunn and D. Rosen, "Design and additive manufacture of functionally graded structures based on digital materials", Additive Manufacturing, vol. 30, p. 100839, 2019. doi: 10.1016/j.addma.2019.100839.
- [8] S. Sysoieva and k. Osadcha, "Status, technologies and prospects of distance learning in higher education in Ukraine", information technologies and learning tools, vol. 70, no. 2, p. 271, 2019. doi: 10.33407 / itlt.v70i2.2907.
- [9] I. Gevko, "Application of computer technologies in the educational process of training in higher education institutions", naukovi zapiski, vol. 0, no. 142, pp. 51-59, 2020. doi: 10.31392/nz-npu-142.2019.06.
- [10] C. Schelly, G. Anzalone, B. Wijnen and J. Pearce, "Open-Source 3-D Printing Technologies for Education: Bringing Additive Manufacturing to the Classroom", SSRN Electronic Journal, 2015. doi: 10.2139/ssrn.3331158.

Special Features of the Educational Component "Design of Devices on Microcontrollers and FPGA"

Iryna Svyd ORCID 0000-0002-4635-6542 Department of Microprocessor Technologies and Systems Kharkiv National University of Radio Electronics Kharkiv, Ukraine iryna.svyd@nure.ua

Oleg Zubkov ORCID 0000-0002-8528-6540 Department of Microprocessor Technologies and Systems Kharkiv National University of Radio Electronics Kharkiv, Ukraine oleh.zubkov@nure.ua Oleksandr Vorgul ORCID 0000-0002-7659-8796 Department of Microprocessor Technologies and Systems Kharkiv National University of Radio Electronics Kharkiv, Ukraine oleksandr.vorgul@nure.ua

Valeriia Chumak ORCID 0000-0002-2403-020X Department of Microprocessor Technologies and Systems Kharkiv National University of Radio Electronics Kharkiv, Ukraine valeriia.chumak@nure.ua

Abstract—Questions of features of the distribution and the implementation of the educational component "Design of devices on microcontrollers and field programmed logical gate arrays" with the support of all stakeholders' requirements to the latest technical knowledge are considered. Structural and technical description of the educational component is discussed.

Keywords—technical education, laboratory workshop, design of devices, laboratory model, MatLab, microcontroller, CPLD, FPGA, Xilinx, STM32, dashboard.

I. INTRODUCTION

Education of students at the Department of Microprocessor Technologies and Systems (MTS) of Kharkiv National University of Radio Electronics (KNURE) began in the 2018-2019 academic year. The main task of the fundamental department of MTS is to strengthen the quality of training of professional engineers in accordance with European standards in the field of microprocessor technologies and systems [1-3].

The curriculum of the discipline "Design of devices on microcontrollers and FPGA" was developed in close cooperation with colleagues from the University of Limoges (France), Lublin University of Technology (Poland) and Istanbul Technical University (Turkey). The best European training practices have been taken into account in the development of the curriculum.

In modern society, much attention is paid to quality of training of technical specialists as a component of scientific and technological progress. Research and teaching staff of KNURE in accordance with the mission and main direction of the university pay sufficient attention to the development and implementation of new technologies in technical education [4-10].

Valerii Semenets ORCID 0000-0001-8969-2143 Department of Microprocessor Technologies and Systems Kharkiv National University of Radio Electronics Kharkiv, Ukraine valery.semenets@nure.ua

Natalia Boiko ORCID 0000-0002-7524-729X Department of Microprocessor Technologies and Systems Kharkiv National University of Radio Electronics Kharkiv, Ukraine natalia.boiko@nure.ua

II. DESCRIPTION OF THE CURRICULUM

When developing the curriculum in the discipline "Design of devices on microcontrollers and FPGA" it was taken into account the best European practices of partner universities, the wishes of stakeholders, scientific and pedagogical experience of university professors: the maximum practical component; solution of block consecutive practical problems; division of discipline into related logical modules; training on modern equipment; use of the latest technologies and so on.

The discipline "Design of devices on microcontrollers and FPGA" is taught in the cycle of general and special professional training for students of the first (bachelor's) level of higher education at the faculties of the university: Faculty of Automatics and Computerized Technologies; Faculty of Information Radio Technologies and Technical Information Security; Faculty of Electronic and Biomedical Engineering; Faculty of Infocommunications. The discipline is studied by students of the following specialties: 125 Cybersecurity; 151 Automation and computer-integrated technologies; 152 Metrology and information-measuring equipment; 163 Biomedical Engineering; 171 Electronics; 172 Telecommunications and radio engineering; 173 Avionics.

Materials of the discipline "Design of devices on microcontrollers and FPGA" in the amount of 10 ECTS credits are divided into three modules:

- Modeling of digital signals by means of MATLAB and VHDL (2 ECTS credits);
- Microcontrollers (4 ECTS credits);
- FPGA (4 ECTS credits).

In the distribution of auditorium hours between types of classes, it is paid a special attention to the practical

II International Scientific and Practical Conference Theoretical and Applied Aspects of Device Development on Microcontrollers and FPGAs orientation of the discipline. Therefore, 75% of the study time is spent on laboratory workshops, and 25% of the time is spent on lectures.

The study of each module of the discipline is designed for one semester. Each module includes lectures, practical classes and labs. There are nine laboratory works in each module. Laboratory work of the first module is performed in two academic hours. While the laboratory work of the second and third modules are performed in four academic hours.

A. Simulation of Digital Signals Using MATLAB and VHDL

This module is aimed at studying the mathematical foundations of digital signal processing and mastering the basic algorithms used for analysis and synthesis of digital signal filtering devices. The laboratory workshop is performed using MatLab software or Octava [11]. The materials of the module are aimed at obtaining the following results by the applicant:

- calculate the spectral, temporal and correlation characteristics of discrete signals, find their Z image;
- determine the system function of digital filters;
- calculate the time and frequency characteristics of digital filters;
- build block diagrams of digital filters in direct, canonical, cascade and parallel forms as well as its transposed variants;
- synthesize filters with infinite and finite impulse characteristics.

When performing a laboratory workshop is modeled:

- discrete signal;
- linear discrete system;
- discrete Fourier transform;
- synthesis of FIR filters by the window method;
- synthesis of FIR and IIR filters by the method of the best uniform approximation;
- synthesis of IIR filters by bilinear z-transformation;
- synthesis of FIR and IIR filters using FDATool and FilterBuilder in order to obtain VHDL description of the filter given.

B. Microcontrollers

This module is aimed at studying the programming of modern microprocessors STM32F407VGT manufactured by ST in C ++, in-circuit debugging of microprocessor software. Much attention is paid to learning the programming language, working with software packages IAR Embedded Workbench for ARM, STM32CubeMX and STM32CubeIDE, to write and debug programs, the use of these microprocessors in digital devices for transmission and processing of information. The laboratory workshop is performed on STM32F4 DISCOVERY models using MatLab, STM32CubeMX, STM32CubeIDE, IAR Embedded Workbench for ARM v 8.3 Kikstart software [12]. The materials of the module are aimed at obtaining the following results by the applicant:

- develop schematics and compose the embedded software for such devices as: keyboard controller, PWM and analog signal generator, analog sensor meter, digital signal filtering device, UART communication device, graphic display control device, etc.;
- debug software using STM32CubeMX, STM32CubeIDE and IAR Embedded Workbench for ARM simulation packages;
- program the microprocessor and test the software composed.

When performing a laboratory workshop the following tasks are carried out:

- study of the architecture and principles of operation of the I / O ports of the processor STM32F407VGT;
- study of programming timers-counters;
- study of programming of the built-in digital-to-analog converter;
- study of programming of the built-in analog-to-digital converter;
- digital filtering of analog signal;
- study of programming of the built-in asynchronous interface UART;
- data storage in the internal flash memory of the processor;
- control of LCD indicator ILI9328 through the built-in FSMC interface;
- development of graphic interface with the ILI9328 indicator.
- C. FPGA

This module is aimed at studying the architecture and programming of modern programmable logic integrated circuits of the Artix-7 FPGA family manufactured by Xilinx, VHDL digital device design language and debugging methods and tools using the Vivado CAD software package; use of FPGA for the development of digital signal processing devices. The laboratory workshop is performed on Artix-7 FPGA Xilinx models using CAD Vivado HLx Design Suite 2018.2, MatLab [13-15]. The materials of the module are aimed at obtaining the following results by the applicant:

- solve at the hardware and software level the task of building specialized hardware;
- create models of digital systems at different levels of description: abstract, schematic and software;
- master the methods of decomposition of the system, which are implemented in hardware and software;
- implement a description of logic (program) of medium complexity in VHDL;

• develop embedded microprocessor systems based on FPGA.

When performing a laboratory workshop are carried out:

- execution of logic modeling of digital input signals;
- 7-segment indicator control;
- formation of a periodic sequence of pulses;
- PWM signal generation; formation of a sinusoidal analog signal;
- control of analog-to-digital converter;
- analog-to-digital and digital-to-analog conversion.

III. EDUCATION ORGANIZATION OF THE DISCIPLINE

Prior to the beginning of the semester, all educational materials of the discipline are posted on the website dl.nure.ua, which implements the computer network educational environment by means of the platform based on the Moodle. Each student gets an access to the courses. This system allows the students to plan their studies more rationally and prepare for classes in advance. Also, when studying the discipline, students have the opportunity to participate in research at the Department of MTS.

The discipline has implemented an accumulative system of points, which takes into account: class attendance, reports on laboratory work, tests; also, above the maximum score, the scientific work of students is taken into account.

During the laboratory work, students receive a large number of graphs, screens of modeling and of verification stages, program codes, photos of the boards, etc. Students submit all completed reports exclusively in electronic form.

Such a system of work on the discipline was introduced at the beginning of the discipline.

IV. CONCLUSIONS

Discipline "Design of devices on microcontrollers and FPGA" corresponds to modern trends in society for the training of highly qualified technicians in the field of microprocessor systems and technologies. It also makes a great contribution to the formation of specialists in embedded systems, which corresponds to the areas of IoT and IIoT.

The proposed distribution of types of classes in the discipline "Design of devices on microcontrollers and FPGA" allows the best way to ensure the practical orientation of training.

This approach made it possible to greatly facilitate the transition of teachers and students to remote work in quarantine conditions.

It is planned to further implement a system of joint work of students on projects and the possibility of remote access to hardware platforms at the laboratory workshop.

REFERENCES

- Valerii Semenets, Liliia Saikivska, Iryna Svyd, Oleksandr Maltsev. Trends in Training Modern Technicians. // First International Scientific and Practical Conference «Theoretical and Applied Aspects of Device Development on Microcontrollers and FPGAs» MC&FPGA-2019, Kharkiv, Ukraine, July 26-27, 2019. – Kharkiv: NURE, MC&FPGA, 2019. – P. 35-36. DOI: 10.35598/mcfpga.2019.013
- [2] V. Semenets, I. Svyd and L. Saikivska, "Methods of improving the quality of preparation of technical specialists", in Engineering education: challendes and developments : materials of the IX International Scientific and Methodological Conference, Minsk, Belarus, 2018, pp. 415-416.
- [3] Semenets V.V., Svyd I.V., SaikivskaL.F. Current trends in the training of specialists in the technical field. // Specialized Exhibition «KharkivProm Days. Production and efficiency». Collection of materials of the forum section «Automation, electronics and robotics. Development Strategies and Innovative Technologies». - Kharkiv, KNURE, Exhibition Company ADT, 2019. - P. 4-5.
- [4] Svyd I.V., Litvinenko O.V., Bilotserkivets O.G. Features of designing digital devices based on Xilinx FPGA in CAD Vivado HLx Design Suite. // Specialized Exhibition «KharkivProm Days. Production and efficiency». Collection of materials of the forum section «Automation, electronics and robotics. Development Strategies and Innovative Technologies». - Kharkiv, KNURE, Exhibition Company ADT, 2019. - P. 43-44.
- [5] V. Semenets, V. Levikin and V. Sayenko, "Research and analysis of the didactic policy of the university in the training of specialists in information technology", Automated control systems and devices, vol. 175, pp. 4-14, 2018.
- [6] V. Kobzev, V. Semenets and V. Filatov, "Components of the information system for monitoring the quality of education in Kharkov National University of Radio Electronics", in 7th Int. scientific and technical conf. Information systems and technologies (IST-2018), Kharkiv-Koblevo, 2018, pp. 51-54.
- [7] I. Tarasov. Organization of the educational process in the design of digital devices using an initial level based boards FPGA Spartan-6 company Xilinx. Components and Technologies, 2011,12, pp.10-14.
- [8] Avrunin O.G. Basics of VDHL language for designing digital devices on FPGA: a textbook. / O.G. Avrunin, T.V. Nosova, V.V. Semenets. -Kharkiv: KNURE, 2018. - 196 p.
- [9] V. Semenets, "Technical aspects for development laboratory base for learning FPGA and microcontroller systems.", in 10th International Conference The Experience of Designing and Application of CAD Systems in Microelectronics, Lviv-Polyana, Ukraine, 2009, p. 145.
- [10] V. Semenets, V. Kauk, O. Avrunin. "The advanced technology of remote training at the initial process" ["Vprovadjennya tehnologiy dystantsiynogo navchannya u navchalnii protses"], High School, 2009. – No. 5. – P. 40–45.
- [11] Digital signal processing and MATLAB: textbook. allowance / A.I. Solonina, D.M. Klionsky, T.V. Merkucheva, S.N. Perov. - SPb .: BHV-Petersburg, 2013 .- 512 p.
- [12] Geoffrey Brown. Discovering the STM32 Microcontroller. USA, $2016.-244\ p.$
- [13] V. Soloviev, Architecture of the CPLD of the firm XILINX: CPLD and FPGA of the 7th series. Moscow: Hotline - Telecom, 2016, p. 392.
- [14] "Artix-7 FPGAs Data Sheet:DC and AC Switching Characteristics. Product Specification. DS181 (v1.25) June 18, 2018", *Xilinx.com*, 2018. [Online]. Available: https://www.xilinx.com/support/ documentation/data_sheets/ds181_Artix_7_Data_Sheet.pdf.
- [15] Design of digital systems using VHDL language / Semenets V.V., Hahanova I.V., Hahanov V.I. - Kharkiv: KhNURE, 2003.-492 p.

Literacy is an Important Factor in Professional Training of Modern Specialist

Viktoriia Tsyhanenko ORCID 0000-0003-2272-3501 Department of Ukrainian Studies Kharkiv National University of Radio Electronics Kharkiv, Ukraine viktoriia.tsyhanenko@nure.ua Alla Serhiieva ORCID 0000-0001-8962-2452 Department of Ukrainian Studies Kharkiv National University of Radio Electronics Kharkiv, Ukraine alla.serhiieva@nure.ua

Nataliia Ochkurova ORCID 0000-0003-0105-7781 Department of Ukrainian Studies Kharkiv National University of Radio Electronics Kharkiv, Ukraine nataliia.ochkurova@nure.ua

Abstract—The abstracts of the report draw attention to such a factor as language literacy, which is extremely important in any communication in the professional field. The problems that arise when using words-terms of foreign origin, verb nouns, adjectives and verbs are considered. Attention is drawn to the difficulties of translating professional terms, especially from the Russian language.

Keywords—borrowing, foreign origin, verb nouns, terminology, terms, suffixes.

I. INTRODUCTION

Modern Ukrainian literary language has long standing origin, complicated history and in spite of all difficulties it is state language of Ukraine, language which is recognized in the world, functions and develops. It unites both generally used words and special, words, which are used in professional speech. Professional words are widely used during project presentation, signing the agreements for cooperation (as well as international), having talks, objections etc. That is why it is important to use easily and correctly technical language.

II. MAIN PART

The problem of technical scientific language used by science and technics in actual, because terms make the main layer of vocabulary used by scientists. Strengthening of internation relations, development of science is impossible without particular special scientific terms usage. There may be difficulties while translating, terms, lexeme usage, that are not in dictionaries or needs additional explanation, usage of verbal nouns, participles.

Besides students have difficulties in using word-terms because scientific style is difficult for comprehension especially when there are too many special unknown lexemes.

There is a problem as to borrowings: it is well-known Ukrainian science uses professional vocabulary both Ukrainian and borrowing origin. Beginning from XVII century scientists did not come the consent as to the problem. One part of scientists insist on only Ukrainian origin terms usage, the other – only borrowed.

There are several ways of borrowings. The first: the words appears in the language together with concept. These words have not Ukrainian corresponding word: reklama (advertisement), gigabajt (gigabyte), polityka (politics).

The second – it is attempt to detail the object, which is already used: revaluation – increase, devaluation – decrease.

Certain parts of foreign origin words (as barbarians ok, fake, bug) does not influence on technical language development.

One must be careful as to words-dublicate. This words have one meaning but they are different. For example – helicopter (Greek origin) and vertolit (Ukrainian); orange (French) – zhovtogaryachyj (Ukrainian).

One must be careful as to verbal nouns with -nnya:

- *uyava* (imagination) *uyavlennya* (concept);
- *zsuv* (shear) *zsuvannya* (movement);
- *roztyag* (tension) *roztyagnennya* (extension) *roztyaguvannya* (extensibility);
- sklad (warehause) skladannya (resignation);
- *zriz* (section) *rizannya* (cut);
- promova (speech) promovlyannya (whisper);
- *napruga* (tension) *napruzhennya* (strain);
- *zvorot* (addres) *zvernennya* (appeal) *zvertannya* (treatment);
- pry`jom (reception) pry`jnyattya (decision) pry`jmannya (acceptance);
- *rozv'yazok* (issue) *rozv'yazannyaя* (solution);
- *spoluka* (connection) *spoluchennya* (communication).

II International Scientific and Practical Conference Theoretical and Applied Aspects of Device Development on Microcontrollers and FPGAs



It is widely spread when presence or absence of the ending leads gradually to initial semantic change of the word.

As to scientic terminologe we have great changes as:

- there is a tendency to gradual edjection of active Present Participle as a result of the Russian language influence. Adjective forms are more used for example modelyuval`nyj, deformuval`nyj, roztyagal`nyj;
- terms with suffix [anya] for showing process are preferred: zapy`suvannya (zapy`s), nagrivannya (nagriv);
- there is a tendency of terms introduction such as «stepenuvannya», «kubuvannya» instead of «pidnesennya do stepenya», «pidnesennya do kuba»;
- terms such as «tverdishaty», «vuzhchaty», «bil`shaty» are more economical than the ones used now «stavaty tverdishym», «stavaty vuzhchym», «stavaty` bil`shym»;
- it is advisable to use successful synonyms for international terms: photography svitly`na, percentage vidsotok, progress postup.

Many mistakes are made while Present Participle Active usage in scientific languafe if there are suffixes -ach(yj), uch(yj): golovuyuchy`j, vy`konuyuchy`j, povazhayuchy`j (chairman of the meeting; who performs, who respects). Almost every word is a translation loan word from Russian. Active Participles must be replaced by subordinate clauses of Adjectives:

- Terms with suffix -uval`n-: absorbuyuchy`j absorbuval`ny`j; akty`vuyuchy`j – akty`vuval`ny`j; vidfil`trovuyuchy`j – vidfil`trovuval`ny`j;
- Terms with suffix -al`n-: vy`peredzhuyuchy`j vy`peredzhal`ny`j; obertayuchy`j obertal`ny`j; shtovxayuchy`j shtovxal`ny`j;
- Terms with suffix -ivn-: interferuyuchy`j interferivny`j; komutuyuchy`j – komutivny`j;
- Terms with suffix -n-: vidxy`lyayuchy`j vidxy`l`ny`j; nagrivayuchy`j – nagrivny`j; nezny`kayuchy`j – nezny`kny`j.

There participles that are substited by adjective with other roots:

- bly`z`kodiyuchy`j bly`z`kosyazhny`j, korotkosyazhny`j;
- dalekodiyuchy`j dalekochy`nny`j, dalekosyazhny`j;
- diyuchy`j chy`nny`j;
- zmazuyuchy`j zmashhuval`ny`j, masty`l`ny`j;
- zumovlyuyuchy`j, obumovlyuyuchy`j spry`chy`nyal`ny`j;
- otochuyuchy`j dovkil`ny`j;
- slidkuyuchy`j stezhny`j;
- teplovy`dil`ny`j, teplovy`dilyayuchy`j teplovy`datny`j.

III. CONCLUTION

So you may make a lot of mistakes if you don't know the peculiarities of scientific speech. Modern specialist must not only use literary scientific speech properly but understand the rules of terminology units creation.

REFERENCES

- Andrusyshyn O. Adjectives in Ukrainian scientific and technical terminology. Bulletin of the National Lviv Polytechnic University. Series "Problems of Ukrainian terminology". 2011. № 709. P. 31–34.
- [2] Vakulenko M.O. Modern problems of terminology and Ukrainian scientific terminology. Kyiv, 2009. 69 p.
- [3] Kunch Z.Y. Problems of foreign language influence on Ukrainian scientific and technical terminology. Terminological bulletin. 2013. Vip. 2 (1). Pp. 215–220.
- [4] Petrovich L.I. Problems of spelling and use of scientific terminology in the Ukrainian language. URL: https://scholar.google.com/scholar
- [5] Sirik O.M. Problems of standardization and codification of Ukrainian railway terminology. History of technology. P. 81–86.
- [6] Yaremenko N.V. Strategies for translating English scientific and technical terminology into Ukrainian. Scientific Bulletin of the National University of Life and Environmental Sciences of Ukraine. Series: philological sciences. 2017. Vip. 272. S. 44–52.

Scientific Edition

II International Scientific and Practical Conference Theoretical and Applied Aspects of Device Development on Microcontrollers and FPGAs MC&FPGA-2020

Conference Proceedings

June 25-26, 2020 Kharkiv, Ukraine

Issue Editor:

Iryna Svyd

Papers are presented in author's edition

Head of the Department of Microprocessor Technologies and Systems Kharkiv National University of Radio Electronics, Nauky Ave. 14, Kharkiv, 61166, Ukraine Phone: +38 (050) 4061-220 E-mail: mcfpga@nure.ua , iryna.svyd@nure.ua Conference on Web: mcfpga.nure.ua

MC&FPGA-2020