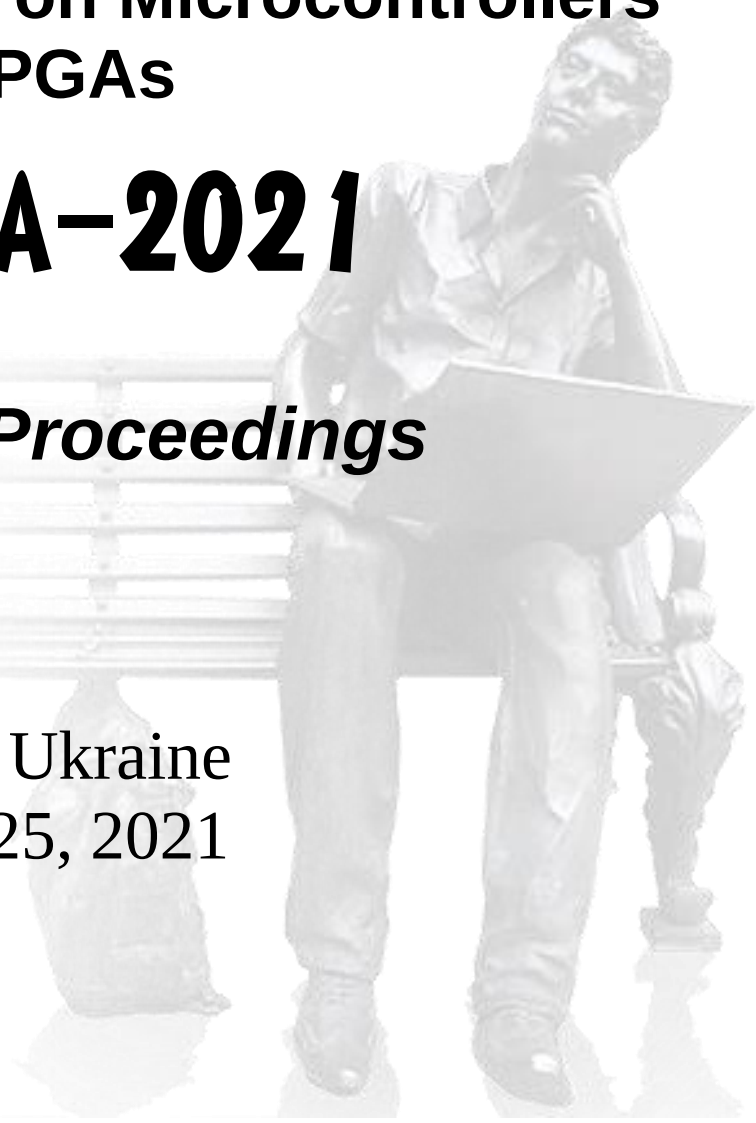
III International Scientific and Practical Conference

Theoretical and Applied Aspects of Device Development on Microcontrollers and FPGAs

MC&FPGA-2021

Conference Proceedings



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There proceedings depict: mathematical modeling of information signals and systems; hardware description languages; systems of computer aided design of devices on microcontrollers, microprocessors and FPGAs; features of device development on microcontrollers and microprocessors; aspects of the development of devices in the FPGA; architecture and microarchitecture of specialized computing systems; modern trends in the design of microprocessor technology; the problem of improving the quality of training specialists.

Papers are presented in authors' edition.

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Features of the Digital Filters Implementation on STM32 Microcontrollers

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***Abstract*—The purpose of this work is to study the efficiency of compilation of digital filters software implementation for STM32 microcontrollers. The research included: the stage of filter synthesis according to its amplitude-frequency characteristic and order, analysis of the signal at the filter output for various types of the program code optimization. As a result of the research, practical recommendations were given for choosing a compiler and the level of optimization in devices containing digital filters.**

Keywords—compiler, microcontroller, optimization, low pass filter, frequency response

I. Introduction

Digital signal filtering is widely used in modern electronic technology. It is used in: positioning and navigation devices, radar signal processing, multimedia and communication technology, etc. [1, 2] Digital signal filtering allows you to isolate a useful signal from the background of noise or suppress interference spectral components. To implement a digital filter, time sampling and quantization of the analog signal amplitude is performed using an analog-to-digital converter (ADC). After that, the obtained samples are processed using filters with a finite or infinite impulse response (FIR or IIR). The filtering result can be written to a information storage or fed to a digital-to-analog converter (DAC).

Digital filters today are implemented in hardware or software. For hardware implementation, FPGAs are most often used [3-5], which allows achieving high performance and processing signals at frequencies up to several GHz. However, such devices are expensive and require significant financial resources for software development. In most devices for industrial and domestic use, digital filters are implemented in software on specialized DSP processors or general-purpose controllers [6].

In recent years, STM32 controllers have been widely used in industrial, communication, multimedia devices [7, 8]. The F4, F7, H7 series of these controllers have a DSP module that allows you to perform floating point calculations at the hardware level, which reduces signal processing time. The microcontroller manufacturer provides information out filter performance for various microcontroller series. However, the effectiveness of the filter depends on the result of the program compilation. Various compilers are used in modern software development environments STM32CubeIDE, IAR, etc. The user is also given the opportunity to select the levels of program optimization. However, when optimizing a program, the compiler can simplify the program code, which can affect the accuracy of calculations or cancel certain actions. Therefore, the purpose of these studies was to study the effect of using different compilers and optimization modes on the performance and implementation correctness of the filter.

II. Designing a Digital Filtering Device on STM32

A. Filter type selection and its parameters calculation

For practical implementation, a low-pass FIR filter was chosen. For high-quality suppression of interference or out-of-band emissions in practical tasks, high-order filters from the 30th to the 200th are used, depending on the technical requirements for the filter. To calculate the filter coefficients, we used the Filter Builder utility from the Matlab R2014b package [9-11]. 2 filters of the 50th and 100th orders were designed. The mathematical description of the 100th order filter has the form

$$y(n) = \sum_{i=n}^{n-100} x(i) \cdot b(i-n), \qquad (1)$$

where y (n) is the signal value at the filter output, x (i) are the input signal samples, which are stored in the filter memory cells, b (i-n) are the filter coefficients.

Fig. 1 shows the amplitude-frequency characteristic (AFC) of the synthesized filter of the 100th order.

The sampling frequency of the signal at the filter input is 44 kHz. The cutoff frequency of both filters is 2 kHz, the frequency of filter suppression is 4 kHz. Suppression of spectral components at frequencies above 4 kHz in the 50th order filter is 43dB, and in the 100th order filter at least 79dB. The calculated filter coefficients are 32 bit real numbers.

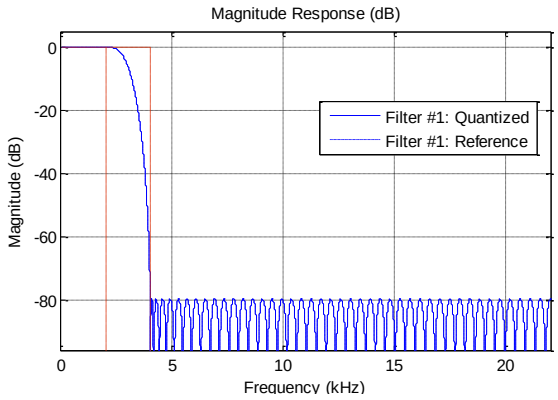

Fig. 1. Frequency response of the synthesized low-pass filter.

B. Hardware implementation of the filter

The STM32F407VG microcontroller with a core clock frequency of 168 MHz was chosen as the hardware platform. This microcontroller contains a built-in 12-bit ADC and DAC. Also, due to the presence of a built-in multi-channel controller for direct memory access (DMA), it is possible to transfer the results of analog-to-digital conversion to RAM and samples from the filter output to the DAC in parallel with the execution of the main task. The timing of the start of converting the analog signal to digital form and digital samples to analog voltage is set by the timer. It generates internal events, according to which the ADC and DAC work synchronously. Then the functional diagram of the digital filtering device on the STM32F407VG has the form (Fig.2).

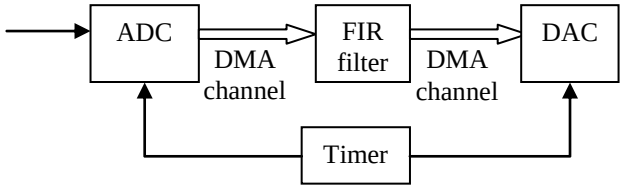

Fig. 2. Functional diagram of the filtration device.

During the research, the developed digital filter worked in two modes: without input data buffering and with input data buffering. In the first mode, when one sample of the analog signal arrived from the ADC, it was fed to the input of the filter and the result of filtering through the DMA channel was fed to the input of the DAC. In the second mode, 128 samples of the input signal were transferred to the RAM buffer via the DMA channel. Upon completion of the buffer filling, an interrupt from the DMA channel was generated and the contents of the buffer were filtered. The filtered data array was transferred to the DAC. The second mode is more efficient, since it takes a certain amount of time to enter and exit the interrupt when processing single samples.

During the research, generator Siglent sdg 2122 was used to generate signals at the ADC input. The signal at the DAC output was investigated using an Intrustar ISDS 220B USB oscilloscope and an Siglent SSA3021 spectrum analyzer.

III. Research Results

To study the software implementation of the filter, the two most popular development platforms IAR Embedded Workbench 8.3 and STM32CubeIDE 1.4 were selected. The first platform has a certified compiler and the ability to choose one of 4 optimization modes: None - no optimization, Low, Medium, High. Produce microcontrollers offers its own development environment STM32CubeIDE, which uses the free popular GCC compiler. In this platform, the user can also select the optimization level: O0 - no optimization, O1 - the main optimization level tested on many tasks, Og - the lowest optimization level for debug mode, O2 - speed optimization with increasing code, O3 - speed optimization with increasing code, Os - optimization for speed without increasing the code, Ofast - maximum performance.

The main parameters for the study were: the speed of the filter (loading the microcontroller to perform filtering operations), the correspondence of the filter characteristics to those obtained during synthesis

Table 1 shows the results of studying the filter speed and the results of measuring the attenuation in the suppression band after compiling the program in the IAR Embedded Workbench.

TABLE I. Research Results for IAR Embedded Workbench

Parameter	**Optimization**					
	None		***Low***		***Medium***	
	Filter order					
	50	***100***	***50***	***100***	***50***	***100***
Efficiency without/with buffer, µs	12,3/ 11,9	24,1/ 23,5	11,9/ 11,6	23,97/ 22,9	6,45/ 6,13	13,05/ 12,09
Attenuation on 4kHz, dB	39	-70	39	-65	-9	-20

When using the optimization levels Medium and High, the suppression of spectral components above 4 kHz does not match the synthesis results. Therefore, when using the IAR Embedded Workbench to compile digital filter code, optimization levels higher than Low should not be used.

Table 2 shows the results of studying the speed of the filter and the results of measuring the attenuation in the suppression band after compiling the program in the STM32CubeIDE environment.

TABLE II. Research Results for STM32CubeIDE

Parameter	**Optimization**					
	O0		***Og***		***O1***	
	Filter order					
	50	***100***	***50***	***100***	***50***	***100***
Efficiency without/with buffer, µs	20/ 17,6	37,9/ 28,9	7,9/ 6,3	15,5/ 12,8	4,2/ 3,8	8,3/ 6,5
Attenuation on 4kHz, dB	39	-70	39	-40	-12	-23

When using STM32CubeIDE to compile a software implementation of a digital filter, it is unacceptable to use optimization levels higher than Og, since the measured filter characteristics do not correspond to the synthesis results.

The usage of data buffering can reduce processing time by up to 18%.

IV. CONCLUSIONS

In the absence of optimization, the program compiled in the STM32CubeIDE environment is inferior in performance to the program compiled in the IAR Embedded Workbench environment. However, at the first level of optimization, the controller manufacturer's GCC compiler provided a significant performance advantage over the IAR Embedded Workbench compiler. Application of any optimization types in STM32CubeIDE leads to a significant deviation of the filter characteristics from the calculated ones.

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Using FPGA Structures For Automotive Electronics

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***Abstract*—As microelectronics becomes increasingly important in automotive systems, transport electronics developers are increasingly relying on FPGA programmable structures to create applications with better performance and flexible architectures.**

Keywords—electronic control units, transport applications, programmable logic blocks, automotive information technology, hardware, digital signal processing

I. Improving Computing Performance for Transport

Although cars have a long and rich history, electronics have been used extensively in transport applications relatively recently, becoming an integral part of the automotive world only in recent decades. Today, car companies compete fiercely not only with each other, but also with the latest and most modern technologies [1].

Currently, manufactured cars rely on many sensors to measure many internal and external variables that could affect the car's driving behavior, as well as additional parameters such as visibility and passenger comfort. Depending on their level of sophistication, sensors can be classified from simple sensors that directly measure individual physical parameters (eg ambient light sensors and temperature sensors) to complex intelligent sensors that determine environmental parameters using broad-spectrum signals (eg radio frequency, radars and light, video); in addition to measurements, they perform data processing and have the ability to perform drives [2].

Using processor-based electronic control units (ECUs), it is difficult to keep up with consumer electronics due to the long cycles of chip development and strict standards of reliability and quality applied to the automotive industry. The automotive industry uses increasingly sophisticated electronic systems to offer the driver better safety and efficiency. Programmable arrays of valves (FPGAs) can play an important role in filling this gap, providing up-to-date performance and high flexibility to system architects to customize projects through a flexible (programmable) electronic circuit structure.

The main goal in automotive design is to reduce the total number of ECUs, as they increase the overall cost of the vehicle and reduce reliability. Thanks to the latest advances in FPGA structures, it is now possible to combine electronic components inside the car more intelligently.

For example, the implementation of a purely hardware processor architecture is a problem that needs to be addressed urgently. However, one possible solution to these interferences is a hybrid approach that combines processors and ECUs with FPGA-based chip systems (SoC), Fig.

FPGAs contain an array of programmable logic blocks, such as built-in memory, digital signal processing units (DSPs), and high-speed receivers. With FPGAs, the automotive system becomes easily scalable with minimal hardware changes.

In this way, FPGAs create opportunities for automotive original manufacturers and suppliers to more effectively build innovative safety programs, such as adaptive cruise control, driver assistance, collision avoidance and blind spot warning.

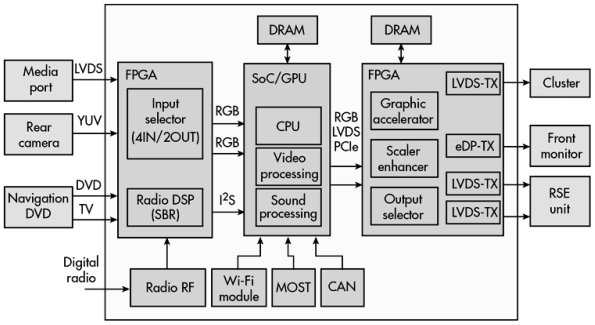

Fig. 1. Hardware processor architecture

As the name implies, driver assistance includes fea-tures such as reversing cameras, three-dimensional sur-veillance cameras, lane departure warning systems, pe-destrian detection and more [3].

II. Hardware and Software

FPGA is a semiconductor device based on a matrix of programmable logic blocks, which are determined by their functionality. This feature distinguishes FPGAs from specialized integrated circuits (ASICs) designed for applications designed for specific design tasks. ASICs and FPGAs have a number of key benefits that need to be carefully evaluated before making a decision. With the

development of unmatched logic density and many other features such as digital signal processing, clock speed and high-speed serial bus, FPGAs become a reliable helper for almost any type of design.

For example, automotive infotainment systems are of great importance in modern vehicle design and have a significant impact on the sale of global vehicles. In these systems, it is important to choose the right main system processor to differentiate the user interface with the latest graphics. With several models to support, you may have to choose different SoCs due to system variations and the emergence of new interoperability technologies.

Thanks to FPGA, the system becomes easily scalable, which allows you to update the firmware remotely to support more manufacturers, regions and models with minimal hardware modifications. You can use the FPGA to support any combination of I / O interfaces [4].

The most important design factor of FPGAs is that they are programmable logic devices. Of course, CPU software can be upgraded, but the same cannot be said for computer architecture. On the other hand, FPGAs can be configured or reprogrammed to perform various functions an infinite number of times. In many recent cars, the software tracks many functions during operation. For example, Tesla models already support software updates remotely.

Thanks to this feature, FPGAs are able to constantly support the original software of manufacturers with the latest versions of programmable or customized hardware architecture systems. Such software updates can be applied to various car features, which may include more FPGA-oriented structures as they become more powerful, smaller and cheaper [5].

Connected vehicles are able to analyze information in real time to provide new information to car users, optimizing their experience. Meanwhile, IoT connectivity can help develop new development models for the automotive market by transforming the relationship between automakers and drivers.

III. Automotive Information Technology

As more IoT technologies are implemented in auto-motive applications, this is a prerequisite for the conver-gence of innovations - especially in the electronics in-dustry. However, experienced engineers know that there is a learning curve when using something new that comes into direct conflict with less development time. In turn, this increases the project risk.

For this reason, designers tend to reuse technologies that are already well known or have been used before. Over time, this philosophy transforms some architecture into widely used industry standards, while most others are used only in narrow market niches.

IoT engineers will have to deal with significant issues such as energy efficiency and management of incompati-ble interfaces. The FPGA-based design approach can help solve these problems by offering a fully functional hardware platform for very low-power IoT applications.

When researching which 32-bit processor will best serve customers, many companies realize that the stand-ard industry architecture offers significant benefits to the owner. Standard industry processors, as a rule, have a wide range of development tools, a large number of available software codes and designers who have the knowledge and experience to use them. Such benefits ac-celerate project development time (and therefore time to market) and also reduce a project risk, which in turn pro-vides users with higher value-added solutions [6].

On this front, the ARM Cortex – M1 processor, de-signed from scratch for use in FPGAs, stands out. One of the main functions - it helps to minimize the amount of resources needed to meet the requirements of the devel-oper. For example, debugging functions can be enabled or removed. Operating system extensions for system tim-ers and software interrupts are not required. Cortex-M1 works with most basic FPGAs, which means that switch-ing from one FPGA device to another requires minimal effort.

IV. Conclusions

FPGAs are now implemented separately or together with processors in many automotive systems, as they provide more efficient and faster solutions for hundreds of ECUs in a vehicle. They provide higher performance without consuming more energy, and improve customiza-tion and scaling capabilities [7].

FPGAs can also help reduce overall car ownership costs by integrating and / or reducing the number of ex-ternal components, speeding up time to market, and con-solidating accelerated project development.

In addition, thanks to innovative and cost-effective imaging solutions, FPGAs support the implementation of even more automotive features. Finally, they often offer a more cost-effective option in programs such as traffic control systems or engines. At present, it is expected that the design needs of the growing hybrid and electric vehi-cle industry will also focus on expanding the FPGA mar-ket.

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Using Benchmark Tests for Research State Memory Encoding in Finite State Machine

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***Abstract*—The synthesizer will automatically assign the state memory codes based on the most effective use of the target technology (e.g., binary, gray code, one-hot) in FPGA. But exists alternative, when user by himself choose type of memory encoding. There was considered user defined state coding method for Quartus Altera.**

Keywords—FPGA, finite state machine, state memory, memory coding, synthesizer, one-hot, sequential, johnson, optimization, speed of performance

I. Introduction

Finite state machines can be easily modeled using the behavioral constructs in FPGA. Within the VHDL state machine model, three processes are used to describe each of the functional blocks: state memory, next state logic, and output logic[1].

The model of the state memory of the FSM using a process describes the behavior of the D-Flip-Flops in the FSM that are holding the current state on their Q outputs. Each time there is a rising edge of the clock, the current state is updated with the next state value present on the D inputs of the D-Flip-Flops. This process must also model the reset condition. At all other times, the process will simply update current_state with next_state on every rising edge of the clock. The process model is very similar to the model of a D-Flip-Flop. This is as expected since this process will synthesize into one or more D-Flip-Flops to hold the current state. The sensitivity list contains only clock and reset, and assignments are only made to the signal current_state. The following syntax shows how to model the state memory of this FSM example.

The synthesizer will automatically assign the state codes based on the most effective use of the target technology (e.g., binary, gray code, one-hot). But exists alternative, when user by himself choose type of memory encoding.

The aim of the work is a comparative study of the possibilities of using the state coding methods to reduce increase the speed of the logic circuit of the finite state automaton.

II. Types of Memory Encoding

There are variants of memory encoding. 1. "One-hot." A separate trigger is used to encode each state. The number of triggers is equal to the number of states of the machine. At any given time, only one trigger can have a single value. To form the value of each trigger, a logical equation is used, in which the number of terms is equal to the number of transitions to the corresponding state. 2. "Sequential". The synthesizer finds long sequences of states in the machine, consisting of unconditional transitions, and encodes the states within them with consecutive binary codes of minimum sufficient bit size. As a result, the address inputs of the Look-Up Table (LUT) elements are not fed to the input signals of the machine, and only the current state code is fed, which usually has a small bit compared to the number of input signals. Sequential state coding provides more optimal filling of static memory cells of LUT elements and reduces the number of unused cells. 3. Johnson. State coding is performed using Johnson code. Each value of this code contains only one continuous sequence of single bits, and any two adjacent values in an ordered sequence of values differ by only one bit. Johnson's code is a cyclic code with an excess and reduces the number of electrical interference caused by the simultaneous switching of several bits of the register circuit. Thus, when using the Johnson code to encode the states of the machine, the number of triggers involved will be greater than in the case of sequential encoding. 4. "Gray." State coding is performed using Gray code, in which two adjacent values in an ordered sequence of values differ in the value of one binary digit, and the number of bits coincides with the number in the case of sequential coding. Like Johnson's code, Gray's code should be used to encode state chains, because each automatic transition in such a chain will be accompanied by a change of only one bit in the machine's memory register. 5. "Auto". The synthesizer chooses one of the above coding methods at its discretion based on the analysis of the VHDL description of the

machine. The choice of coding method also depends on other settings (for example, on the leading optimization strategy - hardware costs or speed), but the generalized approach is as follows: if the machine contains a small number of states, one-hot coding is used; with an average number of states, the Johnson code is used; with a large number of states, the Gray code is used.

III. Using Benchmark Tests for Compare Speed of Performance for Different State Memory Encoding

It is known the input project is synthesized into a circuit that consists of logical elements of logical blocks in a FPGA. Quartus converts a system description in one of the hardware description languages (HDL from Hardware Description Language) into a set of microcircuit-independent functional and storage elements. After the synthesis is completed, information can be obtained on the number of LUT-elements and triggers required for its implementation, as well as the estimated maximum frequency of operation [2].

The difficulty lies in the fact that the same project can be placed in the FPGA in different ways, and there are millions of these ways. Some placement and routing is better, others are worse. The main criterion for the quality of the resulting system is the maximum frequency at which the project can operate with a given arrangement of elements and with a given routing of links. It is influenced by the length of the links between the blocks and the number of programmable switches between them. To use advanced settings that impact the synthesis of design it is necessary to access to settings. To click Assignments > Settings > Compiler Settings > Advanced Settings (Synthesis). The Optimization mode setting enables various combinations of these settings to achieve design goals.

```
.i 2
.o 1
.p 11
.s 4
-0 st0 st0 0
11 st0 st0 0
01 st0 st1 -
0- st1 st1 1
11 st1 st0 0
10 st1 st2 1
1- st2 st2 1
00 st2 st1 1
01 st2 st3 1
0- st3 st3 1
11 st3 st2 1
```

Fig. 1. Benchmarklion in KISS2 format [5]

As it turned out, not every program is suitable for the analysis of efficiency, for example, the vending machine [1] showed the same performance for all types of encoding. So we had to turn to special state machines, benchmarks. Benchmarks have their own names [2], for example, “lion”. Their number will reach more than 50 pieces. Initially, they are recorded in the KISS2 format (fig.1) The KISS2 format is a very popular text format for describing the nehavior of a control units. A KISS2 file is devided into two parts: header and a state transition table. The header contains generic parameters of control unit, i.e. the number of inputs, the number of outputs, the number of states and the number of terms.

```
.i <number of inputs>
.o <number of outputs>
.p <number of products>
.s <number of states used>
.r <reset state>
<input> <current-state > <next-state> <output>
.
.
.
<input> <current-state > <next-state> <output>
```

Fig. 2. Example of headers KISS2[4]

Due to application of TimeQuest Timing Analyzer from Tools Menu Quartus Altera[7] there was estimated time of performance for hybrid of finite state machine from[1] and [5,6]. The results from Report Fmax Summary are for Auto and One-Hot Encoding - 854.7MHz, for Sequential and Minimal Bits 1000 MHz, .Johnson and Gray encoding 1001 MHz, which partially coincide with results from [2].

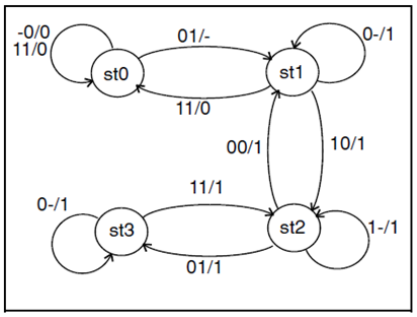

Fig. 3. Graph of the lion benchmark [6]

IV. Conclusion

One can use his own User-Encoded style, or select One-Hot, Minimal Bits, Gray, Johnson, Sequential, or Auto (Compiler-selected) encoding [3]. The best speed of performance has one-hot encoding.

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FPGA Implementation of Floating-Point Significand Multiplier

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***Abstract*—Development of high-performance computational devices needs fast methods of operations with numbers which are presented in floating-point format. One of the most common approaches to build a significand multiplier is using a Wallace CSA-adder tree structure which shows good performance in adding partial sums. Significand multiplier was implemented in FPGA as a part of floating-point multiplier which works with single precision numbers in IEEE-754 standard.**

Keywords—multiplier, floating-point number, carry-save adder, FPGA

I. Introduction

FPGA finds its usage in many different fields such as sorting and data search, audio, video and image processing, cryptography, processing of data packets in networks, random numbers generation. Among new important markets one can distinguish finance, bioinformatics and hardware for radio communication [1]. High performance of FPGA comes from its flexibility, which gives a possibility to realize optimized devices for specific purposes [2]. It is worth mentioning that inner structure of FPGA aslo allows to parallelize data processing.

Lots of computational devices use floating point arithmetic in their operations with numbers. Floating point numbers have such advantage as wide range, which makes them suitable in digital signal processing and scientific modeling.

Multiplication is one of most common operations which computational devices perform. There are a lot of methods of implementing floating point multiplication in hardware. Significand or mantissa multiplication is the main part of floating point multiplication algorithm, therefore much attention should be paid to a structure of significand multiplier.

This paper describes FPGA implementation of significand multiplier which is based on CSA-adder tree. CSA-adder tree performs summation of partial sums that are generated during significands multiplication process.

II. Theoretical Background

A. IEEE-754 Standard

In modern computers and other computational devices floating point numbers are represented according to IEEE-754 standard. This standard defines single and double precision floating point numbers. Single precesion numbers are represented as one which consists of one sign bit, 8 exponent bits and 23 significand bits.

B. Wallace multiplier

Multiplication of significands of floating-point numbers uses the same methods as fixed-point numbers multiplication. According to [3] Wallace multiplier have better performance than array multiplier which is another common method of multiplication. Wallace multiplier consists of CSA-adder tree.

Wallace multiplier is a method of acceleration of multiplication which allows to add several partial sums simultaneously. Wallace CSA-adder tree reduces several k-bit operands to two k+2 bit operands. Unlike Dadda CSA-adder tree Wallace CSA-adder tree reduces the number of operands as early as possible what minimizes the overall delay by making the final carry-propagation adder as short as possible [4].

Another method that can speed up multiplication process is high-radix multiplication which decreases number of partial sums. In this work these two methods were combined together.

C. CSA-adder

One way to add more than two operands simultaneously is to use CSA-adder. CSA-adder is a full adder without carry propagation chain. On the output of CSA-adder there are sum and carry vectors, which then can be added using usual carry-propagation adder. A typical structure of CSA-adder is shown below.

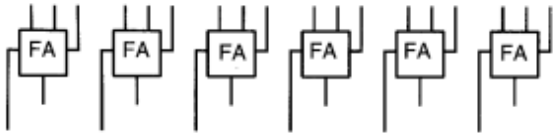

Fig. 1. Structure of CSA-adder [4]

As it can be seen from fig. 1 CSA-adder adds three operands simultaneously. Another structure that adds several operands simultaneously is 4:2 compressor, which is in fact two CSA-adders. The structure of 4:2 compressor is shown below.

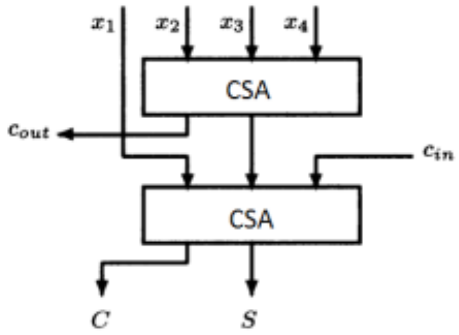

Fig. 2. Structure of 4:2 compressor [5]

The use of 4:2 compressors allows to simplify the structure of a multiplier.

III. FGPA IMPLEMENTATION

As mentioned previously significand of floating point number in IEEE-754 standard consists of 23 bits with one implicit bit will lead to 24 bits. Therefore there will be 24 partial sums. In this work Wallace radix-4 multiplier is used what decreases number of partial sums to 12. The developed structures of significand multiplier and CSA-adder tree are shown below.

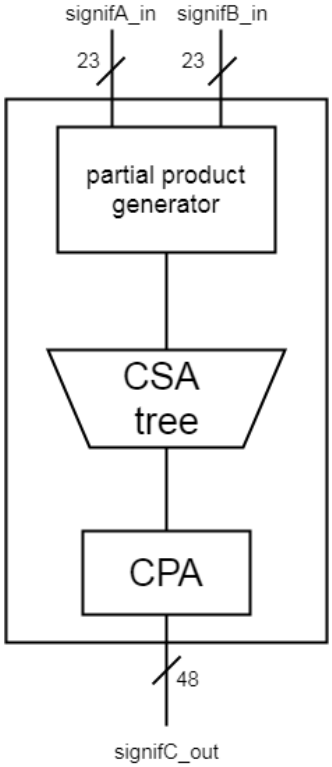

Fig. 3. Structure of significand multiplier

As it can be seen from fig. 3 significand multiplier consists of partial product generator module, CSA-adder tree which reduces number of partial sums to two operands and carry-propagation adder which adds these two operands.

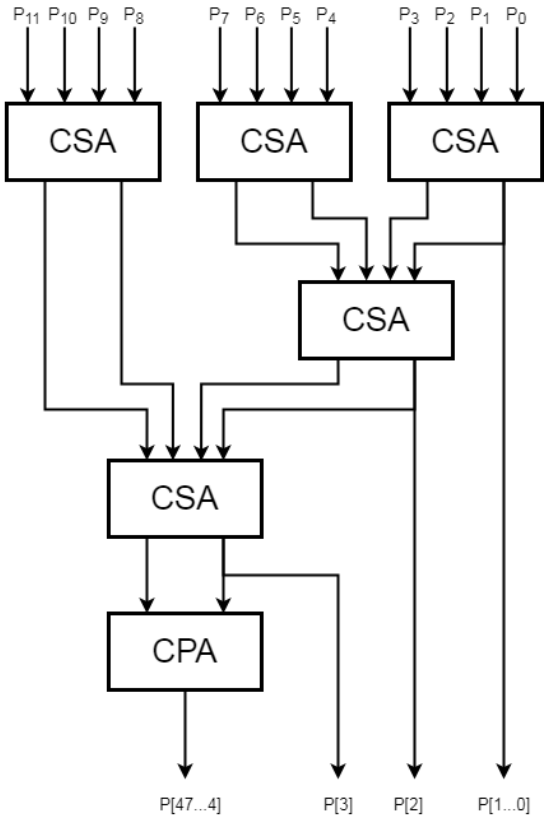

Fig. 4. Structure of Wallace CSA-adder tree

Significand multiplier was simulated in Modelsim and implemented on FPGA Altera Cyclone IV using VHDL. According to compilation report significand multiplier utilizes 1,196 logic elements.

IV. CONCLUSION

Significand multiplier which is based on CSA-adder tree is one of the most common ways to implement high-performance floating point multipliers. The use of significand multiplier which is based on Wallace tree in FPGA projects allows to speed-up multiplication and save embedded FPGA multiplier elements.

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Use of Microprocessor-Based Debug Modules for the Development of GPS (GPRS) and GSM Communication Devices

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***Abstract*—This report is devoted to an overview of the technical characteristics and the specifics of the use of modern debugging microprocessor modules for the development of devices for geolocation of objects and data transmission over a mobile communication channel.**

Keywords—microcontroller system, RASPBERRY PI, arduino ide, GSM(GPS-GPRS)-module

I. INTRODUCTION

The success of modern technologies has made it possible to create microprocessor modules for obtaining geolocation data on the location of an object and means of transmitting the received data.

Fig. 1. GSM communication module SIM900 with USB-TTL converter for connection to a computer

One of these modules is shown in fig.1. It is a mobile communication processor, a SIM card socket, a power stabilizer, an interface for communication with a PC and an external microprocessor [2].

SIM800C is the world's smallest GSM / GPRS module in an LCC case with end contacts. Its distinctive features, in addition to its ultra-miniature size, are support for Bluetooth 3.0 at the chipset level, as well as very good indicators of power consumption, RF sensitivity and support for additional features such as DTMF detection / generation, audio file recording / playback, built-in POP3, SMTP protocols, MMS, FTP, HTTP, SSL, etc. Supported by GPRS multi-slot class 12 (↕85.6 Kbps).

The SIM800C module was created by SIMCom Wireless Solutions specifically taking into account the wishes of our customers and has dimensions of only 17.6 * 15.7 mm and an LCC case with contacts along the perimeter, which implies the possibility of both manual and automated installation.

The Bluetooth transceiver in the module is implemented at the chipset level, so its presence does not affect the cost. Supports SPP, OPP, HFP profiles and work is underway to support additional profiles.

Figure 2 shows the module for determining the satellite coordinates of an object with a ceramic antenna, it has the parameters that are given below [3]:

Power Supply Range: 3 V to 5 V;

Model: GY-GPS6MV2;

Ceramic antenna;

EEPROM for saving the configuration data when powered off;

Backup battery;

LED signal indicator

Antenna Size: 25 x 25 mm.;

Module Size: 25 x 35 mm.;

Mounting Hole Diameter: 3 mm;

Default Baud Rate: 9600 bps.

Fig. 2. Module GPS-location Neo-8m ceramic antenna

NEO-6M GPS module with antenna and built-in EEPROM. This is compatible with various flight controller modules that provide GPS computer test software [3].

This board features the u-blox NEO-6M GPS module with antenna and built-in EEPROM. This is compatible with various flight controller boards designed to work with a GPS module.

II. Main Parts

Let's consider further the option of using these modules to obtain a GPS location shown at Fig. 3.

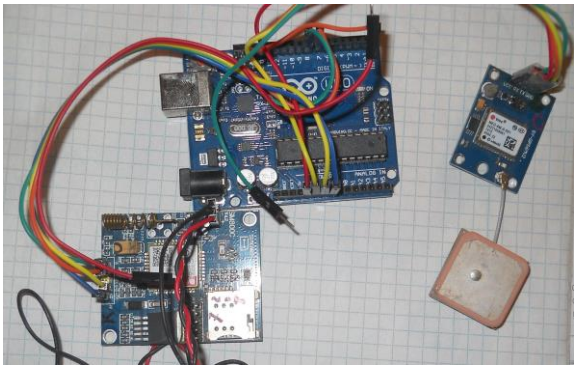

Fig. 3. Application of a laboratory model for determining the geolocation of an object and transmitting their data via mobile communication based on arduino-uno

Overview module a9g-gsm/gprs/gps 32u4 (arduino leonardo). An alternative to the circuit shown in Fig. 3 is the industrial module presented in Fig. 4 [4].

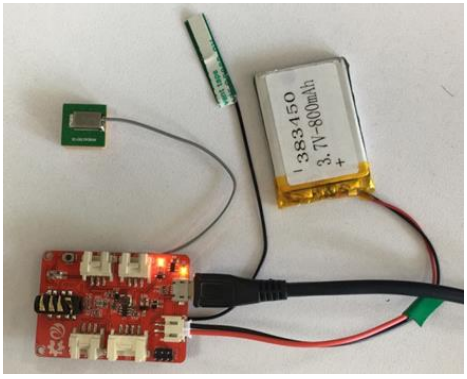

Fig. 4. Module a9g-gsm/gprs/gps 32u4 view down

The 32U4 with A9g GPRS/GSM/GPS Board is based on Mega32U4 and A9 GPRS/GSM/GPS module.

Fig. 5. Module a9g-gsm/gprs/gps 32u4 view up

It can be used to make a call, send text messages and get GPS positioning. Also it has one analog interface, one IIC interface and two digital interface, which you can connect to other expansion modules. It is very easy for you to make a GPS Tracker by using this board. It is also very easy to use AT firmware and use several AT commands can be configured successfully. Two miniature coaxial RF connector is present on the back of the 32U4 with A9G GPRS/GSM/GPS Board to connect with a GSM antenna or a GPS antenna. The connector present on the 32U4 with A9G GPRS/GSM/GPS is called a U.FL connector [4]. The GSM Antenna supplied with the GPRS Shield has an SMA connector (and not an RP-SMA connector) on it. The connection topology is shown in the diagram below:

- ATMEGA32U4+A9G.
- Work voltage: 3.3V to 5V.
- Operating temperature： -30 ℃ to + 80 ℃.
- Three kinds of interfac.
- Equipped with 3.5mm headphone jack.
- 3.7V Battery power supply.
- Standby average current 3ma or less.
- Support the GSM / GPRS/ GPS Quad-band, including 850,900,1800,1900MHZ.
- Support China Mobile and China Unicom's 2G GSM network worldwide.
- GPRS Class 10.
- Sensitivity < -105.
- Support GPS Positioning.
- Support for voice calls.
- Support for SMS text messaging.
- Support GPRS data business, the maximum data rate: download 85.6Kbps, upload 42.8Kbps.
- Supports standard GSM07.07, 07.05 AT commands and Ai-Thinker extended commands.
- Supports two serial ports, a serial port to download an AT command port.

- Support for Global Positioning System.

Horizontal positioning accuracy of less than 2.5m.

- AT command supports the standard AT and TCP / IP command interface.
- Support digital audio and analog audio support for HR, FR, EFR, AMR speech coding.

The battery socket needs to be connected to 3.7V lithium battery, connected to GSM and GPS antenna, and the SIM card slot is inserted into the SIM card slot. Connect the computer to the circuit board via micro USB, as shown in the figure 4-5.

The following describes how to test the module.

Download the "a9_serial_test.ino" program file to the target board.

Open SSCOM32 serial debugging assistant, serial port baud rate :115200 bit/sec.

Test the GPS function. Remember to plug in the GPS antenna.

Send the following command:

- AT return OK;
- AT+GPS=1 return OK;

-AT+GPSRD=1 return OK.

An example of testing the A9G module with the arduino platform is given below.

The test itself is implemented with a connected module via the computer's usb port. This test code complies with the Arduino development environment:

```
void setup()
{
    Serial.begin(115200);
    Serial1.begin(115200);
 pinMode(4, OUTPUT);
 pinMode(5, OUTPUT);
 pinMode(8,OUTPUT);
 digitalWrite(5, HIGH);
 digitalWrite(4, LOW);
 digitalWrite(8, HIGH);
 delay(3000);
 digitalWrite(8, LOW);
 Serial.println("A9 Power ON!");
}
void loop()
{
    char dat;
    if(Serial1.available()){
        dat = Serial1.read();
        Serial.print(dat);
    }
    if(Serial.available()){
        dat = Serial.read();
        Serial1.print(dat);
    }
}
```

III. CONCLUSIONS

The overview of the characteristics of the specified microprocessor modules and ways of their use shows that their compatibility with ARDUINO platform and RASPBERRY PI also debugging kits - STM-32 kits. The example kit is STM-32-OPEN32L-D with STM-32 - Discovery. For example, STM-32 use in development of exclusive and pilot projects [5]. The modules under consideration have a wide range of use the A9G module combined with ARDUINO-LEONARDO platform despite the worst parameters of the antenna devises, has much smaller sizes than devises in figure 3. The size A9G module: 19.2*18.8*3 mm, size all module (fig.5) 45*35 mm. The optimal way to use modules it is creation of tracking systems with GPS-tracks recording.

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The Use of Intelligent Microprocessor Modules for Working with Sound Communication in the Development of Educational Equipment

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***Abstract*—This report is devoted to an overview of the technical characteristics and the specifics of the application of modern debugging microprocessor modules for recognizing audio and text signals.**

Keywords—microcontroller system, RAM memory, EEPROM memory, RSC-4128 speech recognition processor

I. INTRODUCTION

The success of modern technologies has made it possible to create intelligent microprocessor-based speech and sound recognition modules with built-in MEMS micro-phones and with traditional microphones that are connected. One of these modules is shown in Fig.1. It includes 4 microphones created using MEMS technology.

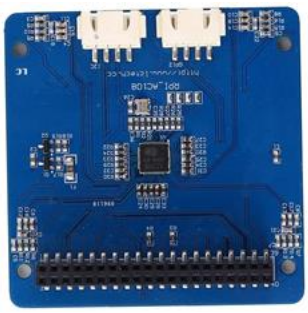

Fig. 1. Voice recognition module AC-108

Fig. 2 shows a plug-in microphone module. These appliances can be used in industrial devices. [1-2].

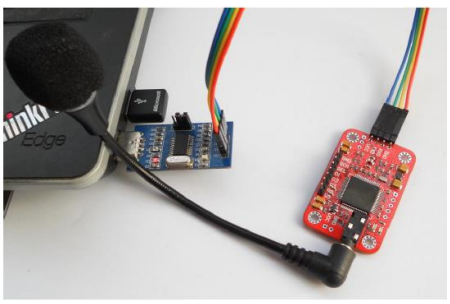

Fig. 2. Voice recognition module V3.1 Elechouse

It has the following parameters: input memory can record 80 seconds sound voice of beep and put in EEPROM memory (storage without power supply). Before recognizing voice commands, they must be loaded from the storage memory (EEPROM) into the recognizer memory. RAM memory - the operative recognizer is designed for 7 voice commands, which means the module is able to simultaneously compare up to 7 voice commands with the incoming sound signal.

The module shown in Fig. 1 uses the RASPBERRY PI 40PIN interface, suitable for motherboards of the RASPBERRY PI series. There are 12 programmable full-color LEDs APA-102-2020 on the module board.

Raspberry Pi control interface: I2C, audio interface: I2S, Raspberry Pi drives the microphone array to capture voice via I2C interface, and then transmits the voice signal to the Raspberry Pi via I2S interface and finally 3.5mm headphones. basic / interface HDMI audio output.

The audio-wm8960 sound recognition module is shown in the Fig. 3.

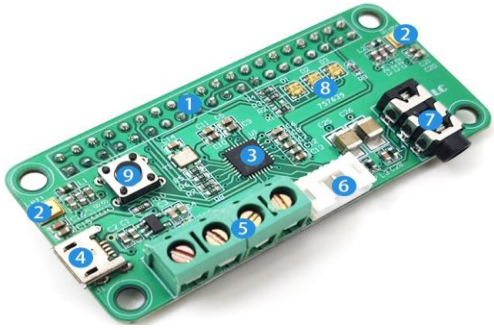

Fig. 3. Voice recognition WM8960

1) Communication interface with minicomputer RASPBERRY Pi.

2) Levi and right MEMS microphone;

3) WM8960: low-power stereo codec;

4) Additional power. If the output is connected to a microphone, this micro USB provides sufficient current;

5) KF301-4P - left and right output channel of the speaker, pressure 2x1 W;

6) PH2.0-4П: left and right output channel speaker, pressure 2x1 W;

7) Output to the headphones: pressure 40 MW (16 Ohm, 3.3V);

8) RGB LED: 3 APA102 color-coded LEDs, connected to SPI interface for Ruspberry Pi.

II. Main Parts

Consider further the ELECHOUSE V3 recognition module based on the RSC-4128 sound processor, since it has a removable microphone, which makes it possible to expand the practical aspects of its use [3-4]. In addition, there is information about the characteristics of this microphone:

- sensitivity: -38dB;
- load impedance: 2.2 kOhm;
- supply voltage: 3 V;
- frequency response: 100 Hz to 20 kHz.

The module is able to work without an external microcontroller, since the manufacturer has laid down functional independence, it is only necessary to record voice commands once and set the settings for independent operation using an external device (PC or MK).

To start working with the voice recognition module, we need to connect it either to a computer (we need a USB-UART connector Fig. 2), or to a microcontroller. If a microcontroller is used, it is necessary to develop a program code to control the module.

The principle of sound recording is associated with fast Fourier transform, creates an array of frequencies from time and then compares the input data with the available arrays. To train the module, the scheme shown in Fig. 2 is used. For the training process, a terminal program (Fig. 4) and instructions (commands) from the datasheet are used.

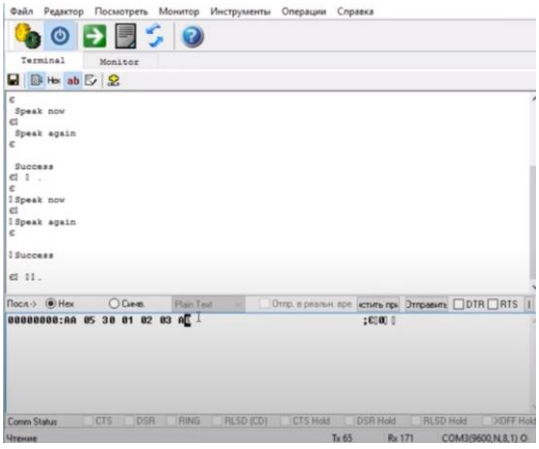

Fig. 4. Application will write commands to module V3 c using the terminal program

Fig. 2 shows that 4 pins (IN0, IN1, IN2, GND) can be used to input the required groups of voice commands from storage into the voice command recognizer [3]. In order for the module to start recognizing voice commands after turning off and turning on the power, you need to specify which voice commands are required to be automatically loaded from the storage into the recognizer when power is applied. The OUT-0 ... .6 pins are designed to record the fact of recognition. It reacts to the recognition of the voice command in the 0-6 cell of the recognition device [3] RSC-4128 Overview presented Fig.5.

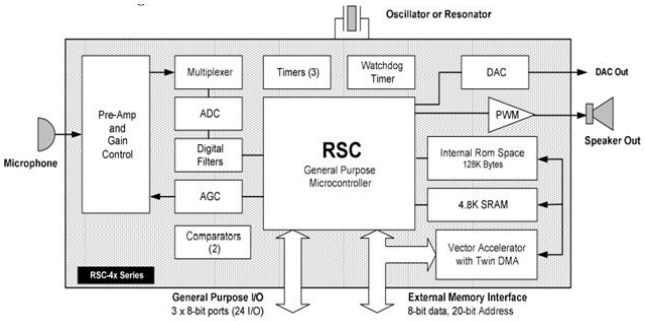

Fig. 5. Structura signal proseccor RSC-4128

The RSC-4128 operates in tandem with FluentChip firmware, an ultra compact suite of recognition and synthesis technologies [4]. The CPU core embedded in the RSC-4128 is an 8-bit, variable-length-instruction micro-controller. The instruction set is similar to 8051microcontroller, and has a variety of addressing mode, mov and 16 bit instructions.

The RSC-4128 has a high frequency (14,32 MHZ) clock as well as a low (32,768 Hz) clock. The RSC-4128 128 kbytes ROM, 16 bit ADC, 10bit DAC and micro-phone.

III. Conclusions

A brief overview of the specifications of the specified microprocessor devices gives an opportunity for developers of experimental (exclusion) projects both scientific and industrial purpose to save time for development of the product.

Small overall dimensions and low energy consumption allows to actively use the designed module in projects type “Smart house” and others.

This fact is especially relevant because the modules are software and hardware compatible with the popular “Arduino” and “Rassberry “ microcontrollers.

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Hardware of Monitoring the Identity of Operating Cycles of Diesel Generator

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***Abstract*—It is offered to use a signal of fluctuations of speed of rotation of a cranked shaft at monitoring of identity of working cycles of the power unit. Hardware has been built and information technology for primary signal processing has been created. A deterministic mathematical model of a diesel circuit in the form of a mechanical system with four degrees of freedom under the condition of friction, Laplace transform, methods of similarity theory and signal graph theory, as well as the method of determinants is used in the development of algorithmic software. The monitoring procedure leads to the solution of a system of redefined algebraic equations with optimization of results based on the method of least squares.**

Keywords—fluctuation signal, information technology, algorithmic software, Laplace Transform

I. INTRODUCTION

Technical and economic indicators of the diesel generator (DG) determine the setting of operating cycles [5], which depends on the uncertainty of setting the phases of gas distribution [6, 7]. The use of hardware for software setting of these phases allows to reduce the uncertainty of setting the identity of work cycles. Solving this problem will provide fuel savings of 5% [2] and reduce the likelihood of overloading individual cylinders. Therefore, the choice of the method of measuring the input information, construction of hardware and algorithmic monitoring of the identity of the operating cycles is an urgent scientific and applied task.

II. ANALYSIS OF LITERARY DATA

The authors propose the idea of monitoring the identity of the operating cycles of DG 3TD-1 based on the processing of data of indirect measurements. As a signal of measuring information, the authors chose fluctuations in the speed of rotation of the crankshaft. The results of studies of the signal of non-uniformity of rotation of the crankshaft DG 6NVD48UA are given in [4]. A measuring transducer and a method for calculating the average effective cylinder pressure, engine power, excess air ratio and exhaust gas temperature have been developed. In [3], a method was proposed to improve the control uncertainty of the fuel supply process to the cylinders based on measurements of the amplitude of angular velocity oscillations and phase shifts of their extremes relative to the top dead center of the first cylinder. Reduces the effect of random interference on the information signal of the non-uniformity of the crankshaft rotation of the high-pass filter with a finite impulse response [1]. In this research the technique of processing of a signal of fluctuations with use of possibilities of the Matlab software environment is developed.

Known hardware and software tools for monitoring the identity of operating cycles have unsatisfactory metrological characteristics and low productivity of input information processing, as well as there is no algorithmic and applied software for processing indirect measurement data. The aim of research is to reduce the uncertainty of the hardware for measuring the signal of the crankshaft speed fluctuations and to improve the productivity of the process of estimating the identity of the working cycles of the DG.

III. CONSTRUCTION OF HARDWARE

The authors used electro-hydraulic injectors as actuators for adjusting the processes of fuel and air supply to the cylinders. Synchronization of the hardware with the phase of rotation of the crankshaft provides a signal of the top dead center of the first cylinder. The block diagram of the hardware for monitoring the identity of the operating cycles of the power unit based on the processing of data of indirect measurements is presented at Fig. 1. The architecture of the system consists of the following components: instantaneous crankshaft speed sensor (SS), top dead center sensor of the first cylinder (TDCS), measuring transducer (MT) of the fluctuation signal, microcomputer and three actuators (ACT1, ACT2 and ACT3).

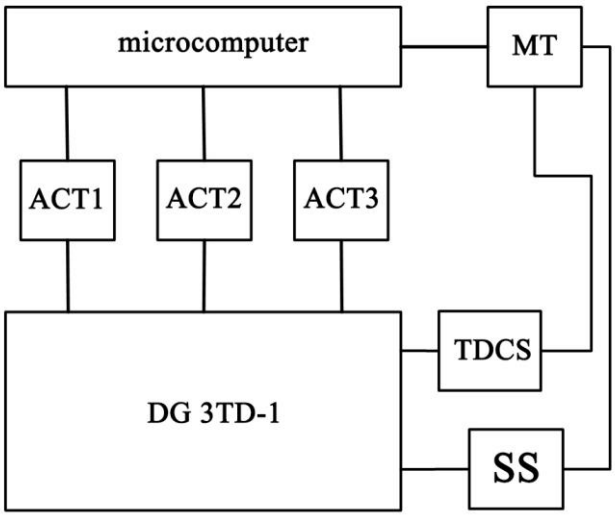

Fig. 1. Hardware architecture

The procedure for monitoring the identity of the operating cycles of DG 3TD-1 involves the following actions:

- measurement of the crankshaft speed signal;
- averaging of the received information and formation of a sample within one turn of a cranked shaft;
- obtaining an array of discrete values of the fluctuation signal;
- construction of a mathematical model of the steep circuit DG 3TD-1;
- solving a deterministic system of differential equations of mass motions in order to monitor the identity of operating cycles;
- establishment of deviations of the working process of the power unit;
- formation of ACT1, ACT2 and ACT3 software control signals.

A method for measuring the signal of fluctuations of the crankshaft speed DG is proposed, which due to the use of hardware to compensate for the kinematic uncertainty of the primary transducer provides the required accuracy. The method consists in the construction of hardware for processing frequency-modulated signal based on multi-channel measurements of time intervals, which are formed by the selected line of the primary converter and correspond to the full rotation of its shaft. In this case, its kinematic uncertainty of the primary converter does not affect the duration of the periods of the output frequency-modulated signals. Based on the processing of experimental data using the information approach, it was found that multi-channel measurements of crankshaft rotation periods significantly reduce the uncertainty of fluctuation signals. Based on this method, MT was developed.

IV. Torque Circuit Simulation

Subject to friction and oscillations between the masses, the torsional scheme of the power unit is presented in the form of a mechanical system with four degrees of freedom. The dynamics of rotation of the cylindrical masses of the crankshaft is described by a system of linear differential equations of this kind:

$$J_i\varphi_i'' + \beta\varphi_i' - \frac{\varphi_{i+1}-\varphi_i}{e} + \frac{\varphi_i-\varphi_{i-1}}{e} = M_i \qquad (1)$$

where $i = 1, 2, \ldots 4$; e is pliability of relations between the masses; $M_i(t)$ is torque obtained as a result of processing of indicator diagrams and compression diagrams, without taking into account the average value; $\varphi_i(t)$ is angle of rotation of the mass; J_i is moment of inertia of the mass; β is friction.

The system of differential equations (1) is reduced to a dimensionless form by means of similarity theory theorems. The Laplace transform under zero initial conditions gives this system the following form:

$$\left(J_i e p^2 + \beta e p + 2\right)\varphi_i - \varphi_{i+1} - \varphi_{i-1} = eM_i \qquad (2)$$

After mathematical transformations, the system of equations (2) takes the following form:

$$\varphi_1 = \sum_{j=1}^{3} \frac{\Delta_j}{\Delta} M_j = \sum_{j=1}^{3} W_j M_j \qquad (3)$$

where $\varphi_1(p)$ - is the Laplace transform of the speed signal of the first mass; $M_j(p)$ – torque; Δ, Δ_j – determinants of the system of equations; W_j – transmission functions that establish information links between the torques of individual cylinders and the signal of fluctuations in the speed of rotation of the first mass. Determinants were obtained using the Mathcad software environment.

The calculation of the CFC of the crankshaft-cylinder paths was performed using the capabilities of the Matlab software environment. As a result of the analysis of LFA, it was concluded that they have an intersection point and in the frequency band 9 - 50 Hz there are oscillations. The roots of numerators and denominators of transfer functions are obtained. The establishment of information links between the torques of the cylinders and the signal of fluctuations of the speed of rotation of the first mass is also carried out on the basis of the use of the topographic rule of the theory of signal graphs. Special points of transfer functions are established.

Algorithmic support is based on solving a system of algebraic equations:

$$BD = \varphi_1 - \varphi_{1,0} \qquad (4)$$

where B - the matrix, the coefficients of which are determined on the basis of the transfer functions and torques of the cylinders, depending on the chosen calculation method; D – vector-column of coefficients; φ_1 – vector-

column of the signal of measurement information; $\varphi_{1,0}$ – vector column of the fluctuation signal of the first mass of the crankshaft in the absence of fuel supply to the cylinders.

This signal is calculated in advance on the basis of processing of compression diagrams of cylinders for the purpose of receiving frequency representation of torques and the received transfer functions. Its time representation can be obtained in the form of the sum of the convolution integrals between the torque of the cylinder and the weight function, which is set on the basis of the transmission.

The number of equations in system (4) is determined by the number of harmonic components of the frequency representation of torque. Accordingly, system (4) is overridden, so the software uses the least squares method to optimize the solution. The number of sampling intervals of the signal of fluctuations of the rotational speed of the first mass is chosen using Kotelnikov's theorem. Computer simulations of the effects of random interference on the uncertainty of the calculation of coefficients have been performed D_i. The influence of additive interferences of hardware on the signal of measuring information, additive technological interferences of phase delays of cylinders concerning the first, and also at known additive interference of a signal of fluctuations for change of width of a spectrum of its frequency representation is investigated. Appropriate graphs are constructed, with the help of which the requirements to the uncertainty of the measurement information signal are formulated.

In the temporal representation of the measurement information, the system of algebraic equations (4) is the balance between the values of the fluctuation signal of the first mass at specific points in time and the corresponding sum of the calculated contributions of each cylinder. The addition to the amount is determined by the product of the coefficients D_i on the corresponding weight function of the contribution of the cylinder to the fluctuation signal. This function is calculated in advance as the convolution interval between the torque of the individual cylinder and the corresponding transfer function. For this purpose, the algorithmic support for monitoring the operating cycles of DG implements the appropriate computational procedures.

Algorithmic support for monitoring the identity of the operating cycles of DG 3TD-1 is based on the use of time and frequency representation of the signal of measuring information. It is established that their use provides a fairly close performance of calculations. If random information is measured on the signal of the measurement information, preference should be given to the use of the algorithm for obtaining estimates of the maximum likelihood of the coefficients of the cylinders.

V. CONSOLUTION

The concept of software movements of hardware for controlling the processes of fuel and air supply to the cylinders DG, a feature of which is the use of indirect measurement data to monitor the identity of operating cycles. The hardware uses a signal of measuring information in the form of fluctuations in the speed of rotation of the crankshaft, and also has a device for synchronization with the operating cycle of the first cylinder.

The representation of the torsional scheme of DG in the form of a deterministic mechanical system with four degrees of freedom is offered. The dynamics of mass motions of a mathematical model taking into account friction is described by a system of second-order differential equations, the parameters of which are normalized on the basis of similarity theory theorems. The mathematical apparatus of the Laplace transform was used to solve it

The transfer functions which establish information communications between torques of cylinders and a signal of fluctuations of speed of rotation of the first weight of a cranked shaft are received. It is established that the use of determinants and methods of signal graph theory give almost identical expressions for transfer functions. The scheme of computer modeling of the signal of measuring information is constructed and on the basis of using the method of the model which is studied, the procedure of identification of its parameters is carried out.

Computer modeling of the computational procedure for establishing the coefficients of cylinders under the action of random algebraic equations on the system is carried out. Algorithmic and application software for computer simulation of noise has been developed. Graphs of uncertainties of calculation of identity of working cycles of DG are received. Requirements for the uncertainty of the VP unit have been established.

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The Development of Soft Skills for Professional Activity (Trend or Reality)

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***Abstract*—Nowadays it's hard to distinguish between hard and soft skills requirements. A potential candidate can be requested for having both of them. The article provides the summarized overview of both skill kinds.**

Keywords—soft-skills, hard-skills, human recruitment

I. Introduction

The reality for many specializations according to the requirements specified in the vacancy, increasingly includes one of the items developed set of soft-skills, while not always correlating with other requirements related to the technical requirements for the vacancy (so-called hard-skills). Sometimes, the interview stage separately includes the stage of communication in an informal environment or a separate communication with the organization's psychologist and HR specialist to determine the level of possible interaction in the team of a potential new colleague. Does the trend have a lasting rationale, or is it just a lawsuit and new fashion winds from the employment procedure?

II. Soft Skills and Hard Skills

Soft-skills terminology means skills that are not tied to a specific profession and allow you to interact normally and flexibly in a team and justify your opinion. The terminology is not new, as the term was added to the business environment only in the late 1990s, and research on the subject began in the 1960s. Currently, the need for soft skills has increased due to the rapid reduction in the relevance of a particular area of knowledge. Therefore, on the one hand, the presence of soft skills in an employee makes him more valuable, because the skills related to the speed of learning and learning new knowledge are more relevant than the accumulated knowledge. This is at first glance.

What skills should be highlighted? First, communication skills allow you to work in a team and negotiate between them. Secondly, self-organization skills and creative skills. The ability to work with information is necessary today because of its large number. Stress tolerance is currently relevant due to the speed of life processes and requires the ability to quickly maintain a normal level of performance.

III. Available Research

As for research in soft-skills fields. Back in 2008, Higher Education in Europe published an article proving that flexible skills are as much a part of professional competencies as rigid ones. The author believes that modern education should include soft skills training - so that graduates meet the requirements of the labor market. The International Journal of Managing Projects in Business has published a study showing that the main difficulties in working on a project are created by the human factor. Researchers summarize the importance of soft management skills.

Gina Watson Mitchell in her dissertation analyzes the survey data and recommends that universities include the development of flexible skills in their curricula.

However, the most complete list and categories were formed by the World Economic Forum in the Future of Jobs report. The study involved global employers-drivers of various industries and identified 35 flexible skills. All flexible skills were divided into 3 key groups: abilities, basic skills, cross-functional skills.

According to the publication CareerAddict, the TOP-20 soft-skills have been identified, which are currently relevant for a potential employee.[1] Consider a few of them:

Work etiquette - excellent work ethic is vital for success throughout working life. A constant desire to learn and progress is necessary. This does not mean that you need to dedicate your entire life to your occupation, but the need to complete your current tasks and some that are not included in the current list of job descriptions to help a teammate.

Flexibility - Being focused on one subject area, the transition between different projects will be difficult. Requires the ability to prioritize to identify pressing issues.

Leadership - Leadership is defined as the ability to take initiative when possible. It is the act of leading a group of people, delegating responsibilities, managing others, and providing guidance for the effective operation of a business or unit. Even though a colleague does not hold a leadership position (for example, he is not a manager), management itself shows a willingness to take control of the situation, effectively manage and support their colleagues.

Self-motivation ¬ despite the passion for work, there may be times when the motivation to perform it is lost. As a specialist of the 21st century, and especially in 2020-2021, everyone should have a thirst for self-motivation to complete tasks on time.

Decision making - the ability to make the right and effective decisions quickly is a requirement that can be met

by every employer. Effective decision-making is to use a combination of intuition and logical reasoning to choose a possible course of action from the proposed options. It also concerns the correct judgment of the situation, conclusions, and practical solution of the problem.

Innovation - it doesn't matter if the employee is in a managerial or a working role - creativity is the basis for a company's sustainable long-term development (also known as a company roadmap). The development of this soft skill is necessary and can be listed in the resume as one of the characteristics that can affect the employer.

IV. Hard Skills Part

Consider the concept of hard skills, and what distinguishes them from soft skills. Currently, the main hard skills that can be identified are:

- Knowledge of foreign languages.
- Speed of computer work, knowledge of typical software packages.
- Knowledge of programming languages and work automation.

Hard skills differ from soft skills in their specification of competencies within a particular specialty. If soft skills are cross-specialization knowledge (knowledge that can be applied in any specialty) and affect the movement in the company and development. As typical examples, the expected hard skills from specialists can be given. For example, for a project manager, the main skills will be the availability of communication skills and knowledge of the subject area of the product.[2] A business analyst needs knowledge of investment analysis methods, skills in working in Agile teams, the ability to process detailed reports and work with large amounts of information. A typical software developer needs knowledge of the appropriate programming language, database skills, analytical thinking, and basic knowledge of technical English.[3]

As for the requirements of a particular specialist - the interview may include separate stages, as mentioned earlier. Sometimes, this can be two or more time-separated interviews in which the specialist will also be asked to communicate with the development team and management that will accompany the colleague.

Considering the development of soft skills, for the time being, it should be noted that their number in a particular job will vary. Depending on the size of the company, product, and focus, it is possible to determine the relationship and the need for communication between colleagues. If you look at the four examples - a large company with outsourcing projects designed for large teams, a product company with small projects for 1-2 people, a large outsourcing company with small projects, and a research and production enterprise with areas related to research and individual work.

In the first example, it is necessary to have a developed set of soft skills due to the large amount of communication that can take place. In the case of a product company with small projects, soft skills may be less important and the advantage of hard skills among professionals may be significant, thus taking advantage of skills that directly affect the company's profits (more projects - more budget). In the case of a large outsourcing company with small projects, the distribution will be almost half, namely, the requirements of a specialist in soft and hard skills will be similar, perhaps with a slight advantage towards hard skills. The last example, namely NVP with scientific individual research can be a demonstration of full hard-skills enterprise, where the need for external communication is minimal, and interaction between colleagues and the transfer of test results or intermediate results can be formalized according to DSTU norms and standards.

V. Conclusion

Thus, today the development of soft skills is necessary in the case of employment in large companies, where they can directly affect the advancement in the career ladder. In the case of employment in a company where preference is given to employees who can fully meet the requirements of professional skills, the availability of soft skills can be a nice bonus, but not the main parameter in the selection of potential candidates.

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Automated Module for Product Identification by their Visual Characteristics

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***Abstract*—In this work the automated module of identification of products on their visual signs is developed. The general architecture of the automated module and algorithms of work of the client module, the program in the mode of reception of the answer from the server and a server part are developed. The distributed principle of data processing and storage was used to solve the problems. The automated software module is based on the distributed control principle. Developed software for the mobile device and the necessary scripts for the server part. Testing of the developed software is performed.**

Keywords—DART, Flutter, MySQL, MVC, OpenCV, SIFT, Automated Module, Intellectual Production, Customer, Recognition, Server

I. Introduction

The task of product identification by optical non-contact means in production is of great importance for improving product quality, reducing the percentage of waste and increasing productivity. The introduction of automated image recognition systems using modern algorithms for determining the type of components, the classification of each individual sample, regardless of its orientation in space, allows workers with lower qualifications to perform such operations. It also reduces the load on the person and reduces the number of errors when performing a particular operation.

The use of an optical system for identifying components to the warehouse makes it possible to automate such operations of the worker, which previously required only the presence of a person with a certain qualification. The integration of the automated system into the overall management system of the enterprise leads to the implementation of the requirements for the implementation of the concept of Industry 4.0 in the modern intelligent enterprise.

II. Development of Automated Module Architecture

The distributed principle of data processing and storage was used in the development of the architecture.

In the workplace, the worker uses computer vision module, which is made using a mobile device (phone or tablet) with built-in or external camera. The resulting image is transmitted to a dedicated local or cloud server through communication. A router or Internet gateway is used as a means of communication.

The server is loaded with services for accepting images from clients, analyzing images and searching for personal features in the database. If the image has already been classified and described, the characteristics of the recognized object will be found.

The characteristics found are redirected using the appropriate tools on the server to the client that sent the recognition request. This returns the description of the object displayed on the screen of the mobile device to the operator.

Thanks to the distributed architecture and the use of a dedicated server, centralized access to information is organized for all objects that may be encountered while working at the employee's workplace. Database can be filled regardless of the main process of using the program, even in real time.

In fig. 1 shows the architecture of the automated component recognition system at the production site using the developed automated module. This figure shows a separate place of the worker (expert), who fills the database with new samples of production facilities and describes them.

III. Development of Customer Module Algorithm

The algorithm of operation of the client module in the image transmission mode is shown in fig. 2. The functions of the client module.

- Get a picture of the subject with the built-in or external video camera.
- Image pre-processing.
- Connection to the server.
- Image transfer for analysis.
- Waiting for the results of the analysis.
- Display of analysis results and data about the object.

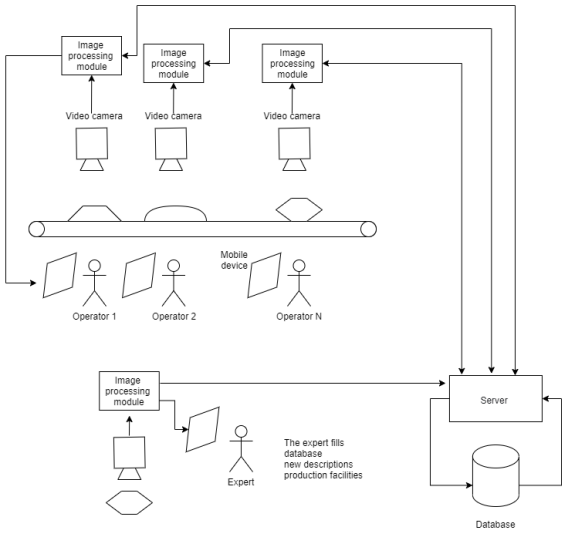

Fig. 1. Architecture of the automated system of recognition of components on a production site with use of the developed automated module

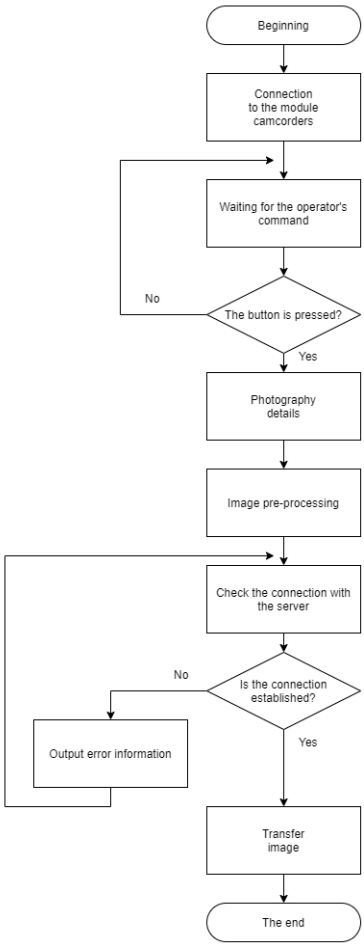

Fig. 2. Algorithm of client module operation in image transmission mode

In fig. 3 shows how the program works in the mode of receiving the image and sending it to the server. In this mode, the program is constantly configured to work with the camera and most of the time is waiting for a command from the operator. At this time, the current image of the workplace is displayed on the screen of the mobile device.

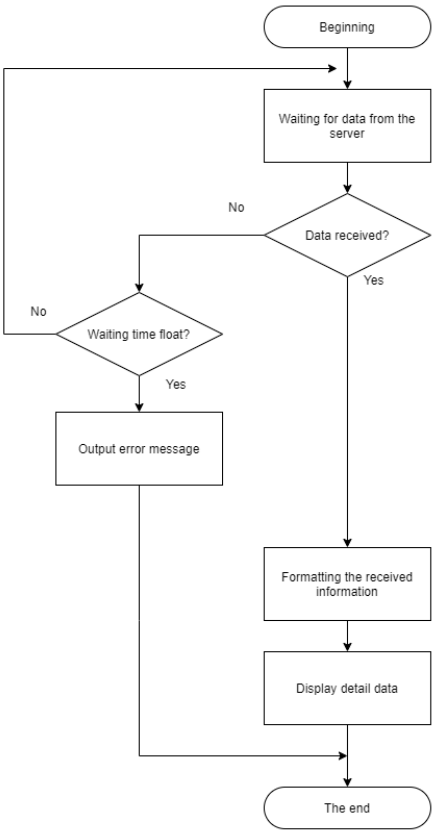

Fig. 3. Architecture of the automated system of recognition of components on a production site with use of the developed automated module

In case the operator needs to know the information about the component, he clicks on the "Recognize" button. The program takes a photo of the component that is in the workplace and pre-processes the resulting image. This removes extraneous noise and reduces the image to the specified brightness level.

After pre-processing, the connection to the server is checked. If the connection is lost, or has not yet been established, the operator displays the appropriate information window. If the connection is established, the received processed image is transmitted to the server. After that, the program goes into standby mode and receives information about the component.

In fig. 3 shows the algorithm of the program in the mode of receiving a response from the server. After sending a request to the server, the client program waits for a response. If no response is received within this time, it may indicate a connection or other problem. Thus, an error message is displayed to the operator after the set time.

If the answer is received, then before displaying it on the screen, the information is pre-formatted and only then displayed on the screen of the operator's mobile device. After these steps, the procedure of photographing and recognition is repeated.

IV. Development of the Server Part Algorithm

The functions of the server part.

- Receiving a request from the client.

- Image verification.
- Image preparation.
- Branch on the image of key points.
- Branch of key point descriptors.
- Search in the database of similar descriptors with a certain threshold of compliance.
- Formation of the answer.
- Sending a response to the client.

The above functions are in the algorithm of the server part, which is shown in fig. 4. A descriptor is a key point identifier that distinguishes it from another mass of special points. In turn, descriptors should provide invariance of finding of correspondence between special points concerning transformations of images.

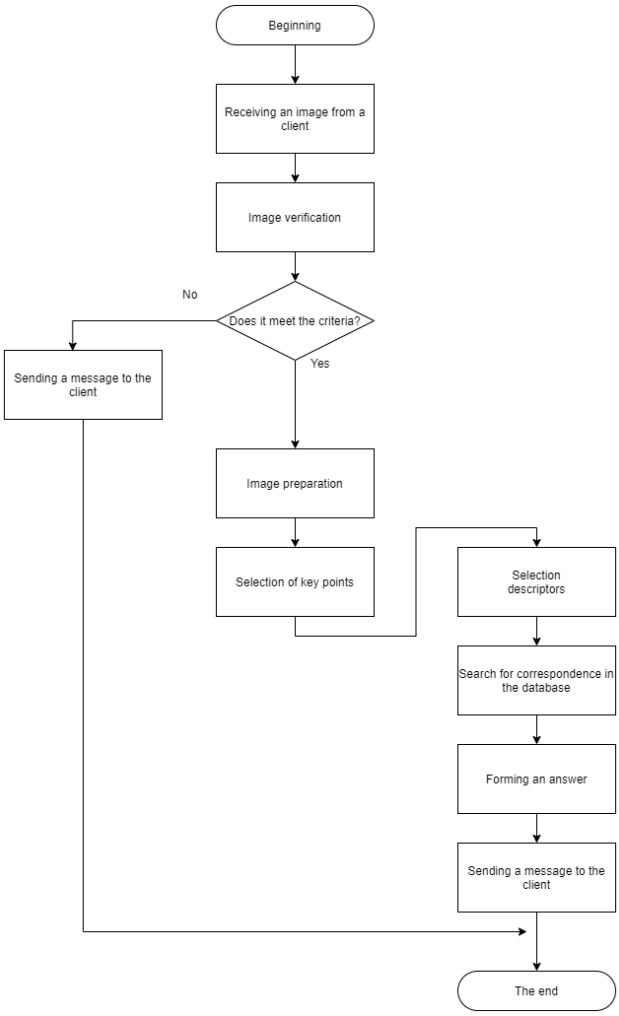

Fig. 4. Algorithm of server part operation

Preparation of the image consists in its preliminary processing on the server side. For this image is blurred by the Gaussian method with a certain radius.

Next, the image is scaled and a Gaussian pyramid is built and the difference between the obtained images is calculated. This process is shown in fig. 5.

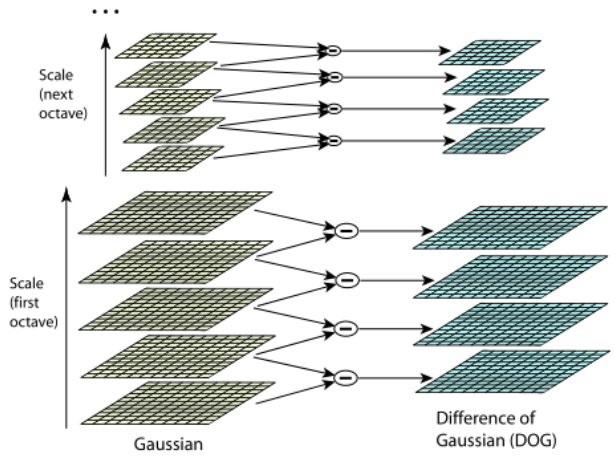

Fig. 5. Scaling and constructing Gaussian differences

This pre-treatment makes it possible to proceed to the next stage. This is the selection of special points and descriptors. The following sequence of the problem of comparison of images is used.

- Key points and their descriptors are highlighted in the images;
- By coincidence of descriptors the key points corresponding to each other are allocated;
- Based on a set of key points, an image transformation model is built, with the help of which one image can be obtained from another.

In fig. 6 shows the principle of finding descriptors in the image.

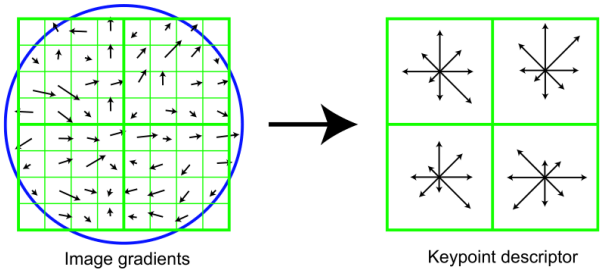

Fig. 6. Finding descriptors in the image

This figure schematically shows part of the image and obtained by the method [7] descriptor. The arrow shows the gradient of each pixel. Each descriptor gradient corresponds to three coordinates (x, y, n). x is the distance to the gradient horizontally, y is the distance to the gradient vertically, n is the distance to the gradient in the histogram. Histograms are based on the pixels of the image being processed. The value of the Gaussian nucleus is taken as a coefficient. Each occurrence of the gradient in the histogram is multiplied by all three weights of trilinear interpolation.

After processing the image and selecting the descriptors, similar descriptions are searched in the database. As a result of search the answer which is sent to the client is formed. The response may contain a description of the object, if it has been identified, or a message about the lack of information about this object, if the database does not match.

V. Software Development and Testing

Developed for a mobile device, the program has a graphical interface with the ability to view the database, download new components to the database and recognize components in real time with the presentation of information from the database.

Each component has a name, a short description, a photo from different angles, the cell number in the warehouse. The country of manufacture and the city where the production is located are also indicated. The user has the ability to add the name of the component, country of manufacture, city, specify the type of part and the city of storage in the warehouse. The user can also add the necessary additional images of the component. These can be fragments of the drawing, or additional views (fig.7).

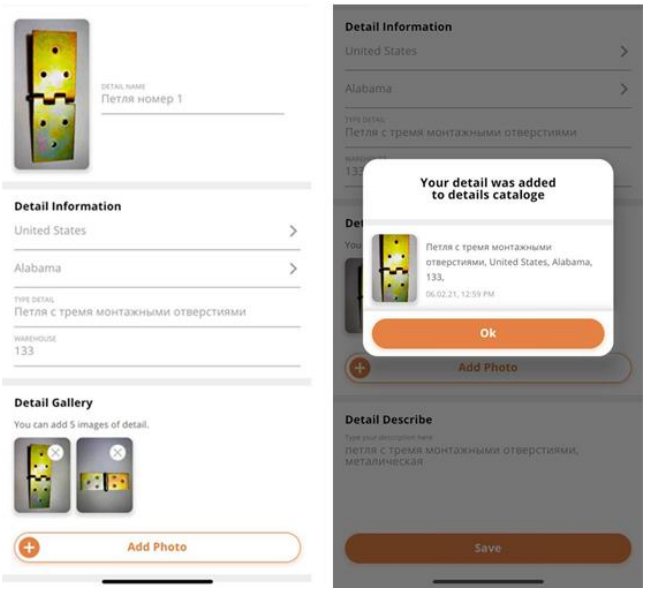

Fig. 7. Example of two software screens

To test the developed software, a database of components was created and a list of all items in the database was obtained using the appropriate window.

Next, the recognition algorithm was tested. The recognition accuracy is affected by the coefficient of the distance of special points, which is specified in the code by the server. Changing the specified coefficient, a number of test tests were performed.

In fig. 8 shows a graph of the dynamics of the number of errors from the distance coefficient of special points. As a result of the results analysis of recognition algorithm testing it is possible to define optimum value of factor of distance of special points making 0,55.

The recognition results are also affected by the color scheme of the image. So images in the format "IMREAD_REDUCED_COLOR_4" have more cases of correct recognition.

VI. Conclusion

In this work the automated module of identification of products on their visual signs is developed. The general architecture of the automated module and algorithms of work of the client module, the program in the mode of reception of the answer from the server and a server part are developed.

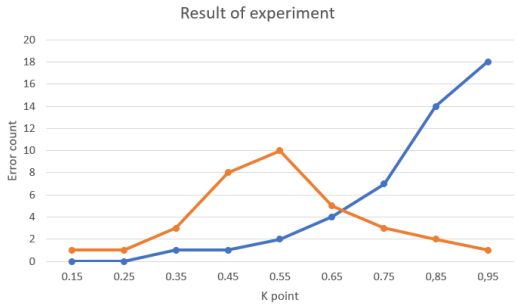

Fig. 8. The results of testing the recognition algorithm

The distributed principle of data processing and storage was used to solve the problems. The automated software module is based on the distributed control principle. The server uses the following technologies and programming languages: Laravel framework, PHP programming language, MySQL database, Open CV. The Flutter framework and the Dart programming language are used to write the program.

Developed software for the mobile device and the necessary scripts for the server part. Testing of the developed software is performed. As a result of the analysis of the results of testing the recognition algorithm, it is possible to determine the optimal value of the distance coefficient of special points, which is 0.55. It was also found that the recognition results are influenced by the color scheme of the image. So images in the format "IMREAD_REDUCED_COLOR_4" have more cases of correct recognition.

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Neuron Networks Design in Matlab and Vivado

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***Abstract*—This article is devoted to design of a measurement system based on specialized FPGA. A balance of ACD and DAC channels through output from one side and computation power of FPGA from another side is considered. Possibilities for obtaining one more tool for screening the signal processing is proposed.**

Keywords—FPGA, analog signal, digital signal processing, measurement system

I. Introduction

Computing tools, in particular for solving problems implemented in embedded execution, are currently being rapidly developed. In its development, for a highly effective solution of problems, the complexity increases and the quality is quickly reached its limit [1, 2]. In a sense, by changing the quantity it is no longer possible to obtain an adequate change in quality for reasonable money. Apparently, all such roads turn to problems of complexity theory.

Neural networks in embedded systems can be used as a universal decisive node. In this work, an attempt is made to review the current state of arts and chart a path for solution of a simple typical problem with means we can reach.

II. Neuron Networks from a Bird's Eye

A neural network is a model of a multilayer system with redundant connections in layers, with the possibility of feedback (recurrent) or without the possibility (convolutional), fully described by a wide set of dynamically changing parameters (weights) [2-4].

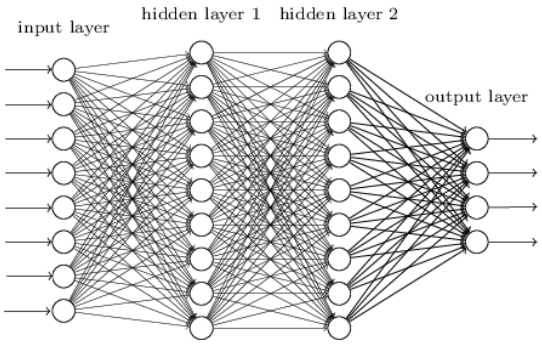


Fig. 1. Convolutional Neuron Network.

Neural network element – neuron can be described as a node with multiple inputs and a decision rule.

One can borrow some experience in implementing a neural network on analog elements [1-3], but at the same time, in addition to the complexity inherent in large systems (controllability, number of parameters, speed, cost at all stages of development), energy consumption also becomes important.

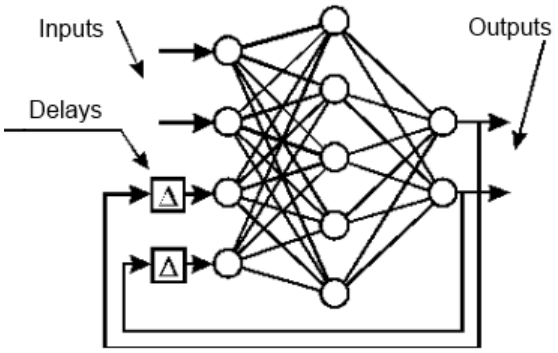


Fig. 2. Recurrent neuron Network.

Applying neural networks seems to have to go through several stages [1, 2]:

- development (on paper) and compilation of a mathematical model
- choice of element base and implementation (classic detailing and construction)
- training a neural network (a feature that is not available for alternative implementations)
- work and correction of the model (retraining)
- utilization of the neural network. Better to foresee it.

In this sense, the use of ready-made solutions can significantly reduce the time at all stages, if the ready-made solutions can be trusted to solve the required task.

III. Matlab Offers

Matlab offers all possible assistance in the neural network setting, development and training. The first version of neural network toolbox in Matlab seems to have appeared in version 4.0, 1992, under Windows 3.1. The site today has a toolbox history that stretches via time from version 2021a

to version 2018a. And no other versions, unfortunately. Though that would be interesting. Since some version, the toolbox is called the Deep Learning Toolbox [5-9].

A. *Workflow for Neural Network Design*

The work flow for the neural network design process has seven primary steps:

1) Collect data.

2) Create the network.

3) Configure the network.

4) Initialize the weights and biases.

5) Train the network.

6) Validate the network.

7) Use the network.

B. *Neuron Model*

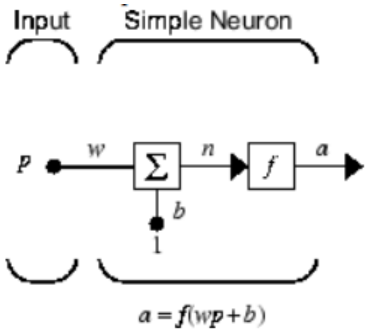


Fig. 3. Simple Neuron.

The simple neuron can be extended to handle inputs that are vectors. A neuron with a single R-element input vector is shown below. Here the individual input elements:

$$p_1, p_2, p_3, \cdots, p_R \tag{1}$$

are multiplied by weights

$$w_{,1,1}, w_{1,2}, w_{1,3}, \cdots, w_{1,R} \tag{2}$$

and the weighted values are fed to the summing junction. Their sum is simply Wp, the dot product of the (single row) matrix W and the vector p.

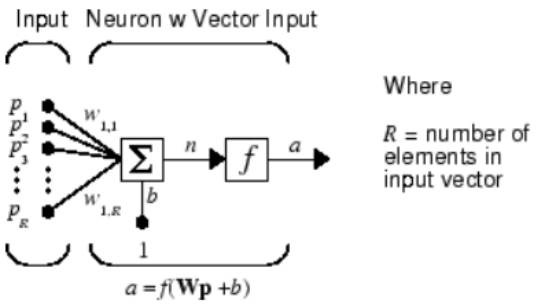


Fig. 4. Neuron with Vector Input.

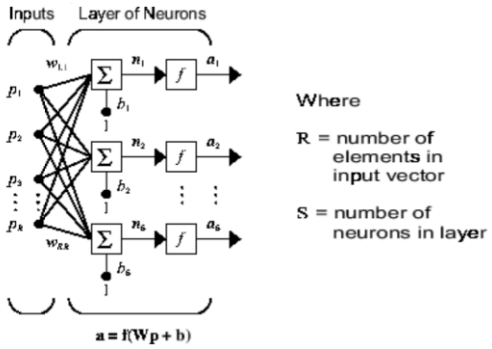
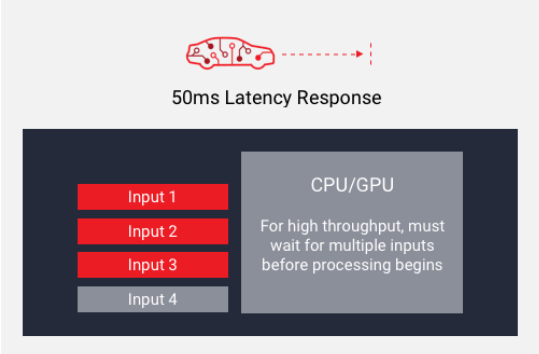


Fig. 5. Neural Network Architectures.

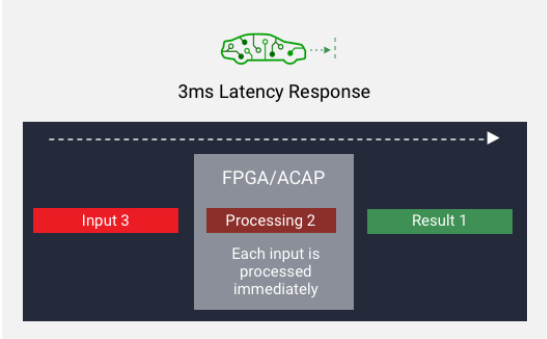
IV. FPGA Implementation

Apparently, at present, the implementation of a neural network can be performed on anything on a CPU, GPU, FPGA. Probably, somewhere there are specialized neuroprocessors that are hybrid (analog-digital). Let's consider briefly only FPGA and only Xilinx case.

Front panel of Xilinx announces lowest latency AI inference [2, 4].



High Throughput OR Low Latency Achieves throughput using high-batch size. Must wait for all inputs to be ready before processing, resulting in high latency



High Throughput AND Low Latency Achieves throughput using low-batch size. Processes each input as soon as it's ready, resulting in low latency [10].

Then the Xilinx provides DPU for convolutional neural network

Product Description The Xilinx® Deep Learning Processor Unit (DPU) is a programmable engine dedicated for convolutional neural network. The unit contains register configure module, data controller module, and convolution

computing module. There is a specialized instruction set for DPU, which enables DPU to work efficiently for many convolutional neural networks. The deployed convolutional neural network in DPU includes VGG, ResNet, GoogLeNet, YOLO, SSD, MobileNet, FPN, etc.

The DPU IP can be integrated as a block in the programmable logic (PL) of the selected Zynq®-7000 SoC and Zynq UltraScale™+ MPSoC devices with direct connections to the processing system (PS). To use DPU, you should prepare the instructions and input image data in the specific memory address that DPU can access. The DPU operation also requires the application processing unit (APU) to service interrupts to coordinate data transfer.

The DPU presume to utilize Zynq 7000 and Zynq UltraScale+ products.

TABLE I. PROCESSING SYSTEM

Features	ZU*CG	Z7000s	Z7000
Application Processing Unit	Dual-core Arm Cortex-A53 MPCore up to 1.3GHz	Single-core ARM Cortex-A9 MPCore	Dual-core ARM Cortex-A9 MPCore
Real-Time Processing Unit	Dual-core Arm Cortex-R5F MPCore up to 533MHz	-	-
Maximum Frequency	n/a	Up to 766MHz	Up to 866MHz or 1 GHz
Dynamic memory Interface	DDR4, LPDDR4, DDR3, DDR3L, LPDDR3	DDR3, DDR3L, DDR2, LPDDR2	DDR3, DDR3L, DDR2, LPDDR2
High-Speed periferials	PCIe® Gen2, USB3.0, SATA 3.1, DisplayPort, Gigabit Ethernet	USB 2.0, Gigabit Ethernet, SD/SDIO	
Dedicated Periferial Pins	n/a	Up to 128	Up to 128

Programmed Logic:

a) One slave AXI interface for accessing configuration and status registers.

b) One master interface for accessing instructions.

c) Supports configurable AXI master interface with 64 or 128 bits for accessing data.

d) Supports individual configuration of each channel.

e) Supports optional interrupt request generation.

f) Some highlights of DPU functionality include:

- Configurable hardware architecture includes: B512, B800, B1024, B1152, B1600, B2304, B3136, and B4096
- Configurable core number up to three
- Convolution and deconvolution
- Max pooling
- ReLu and Leaky ReLu
- Concat
- Elementwise
- Dilation
- Reorg
- Fully connected layer
- Batch Normalization
- Split

V. CONCLUSION

To see how good this idea - using a neural network to solve a typical complex problem - is, one needs to test it in practice. A fairly common task for a neural network is pattern recognition. But this will be the subject of further research.

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Study of the Method of Information Transfer to LED Matrix According to the ModBus Protocol

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***Abstract*—This paper provides an example of using the ModBus industrial protocol to control an LED information board. The developed device can be used in a laboratory workshop to study the work with industrial protocols.**

Keywords—industrial networks, Modbus, Run string, Arduino, Protocol, Automated Module

I. Introduction

Industrial networks are widely used in production processes because they meet the following requirements: work in real time; lack of large arrays of transmitted information; increased reliability of data transmission in industrial conditions; work in different physical environments; coverage of large distances between network nodes; reinforced construction of network equipment; implementation of safe operation of devices in an explosive environment

Features of modern technologies of industrial networks are:

- use of multivariate field devices (they can be used together with several parallel connected circuits 4 ... 20 mA);
- no additional analog-to-digital and digital-to-analog transformations on the communication barrier and in the control system;
- exclusion of calibration of the measuring circuit (the measured value will be converted only once from the analog value to a digital value).

Modbus is one of the most common industrial protocols for data exchange between different devices (machine-to-machine, M2M). The popularity is due to many factors, including ease of implementation, no need to use additional chips, and, of course, the openness of the protocol.

The advantages of the Modbus protocol include:

- reliable error control;
- mass prevalence;
- openness;
- the ability to include in the network a large number of subordinate devices, followed by access to any of them using the address allocated to him.

II. Modbus Protocol Structure

The Modbus structure consists of queries and answers. They are based on a simple protocol package, the so-called PDU (Protocol Data Unit).

The structure of the PDU does not depend on the type of communication line and includes the function code (FCode) and the data field (Data), which is presented in fig. 1.

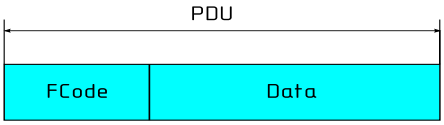

Fig. 1. PDU package structure

To transmit a packet over physical communication lines, the PDU is placed in another packet that contains additional fields. This package is called ADU (Application Data Unit). The general structure of the ADU package for the ModBus RTU is shown in fig. 2.

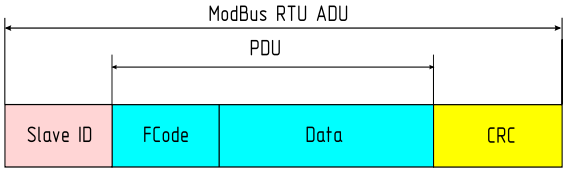

Fig. 2. General ADU package structure for Modbus RTU

The Modbus RTU ADU packet in addition to the PDU packet also includes the Slave ID – the address of the slave device and the checksum CRC16 to verify the correctness of the packet.

This implementation of the Modbus protocol uses the following data types:

- flag – one bit, the register of flags is available for both reading and writing. The flags are stored in the RAM of the microcontroller. 1 byte is allocated for flags, so you can access up to 8 flags;
- discrete register – one bit, read-only. The discrete register is the input port. Discrete registers are a microcontroller status register, so 8 bits are available;

- storage register – a 16-bit register available for reading and writing. Selected cells in the RAM of the microcontroller act as storage registers. 32 bytes are allocated for storage registers, thus access to 16 registers is possible;
- input register – a 16-bit read-only register.

The query consists of the address of the first element of the table, the value of which you want to read, and the number of read elements. The address and amount of data are specified in 16-bit numbers, the high byte of each of them is transmitted first.

The requested data is transmitted in response. The number of bytes of data depends on the number of requested items. One byte is transmitted before the data, the value of which is equal to the number of bytes of data.

The command consists of the element address (2 bytes) and the value is set (2 bytes). For the storage register, the value is just a 16-bit word.

If the command is successful, the slave returns a copy of the request.

The Modbus module interface is the interface from the Modbus server to the user program, which is determined by the program objects. The main functions of the Modbus server are to wait for a Modbus request on the TCP port 502, to process this request, and then to generate a Modbus response depending on the device context.

The principle of message exchange is shown in fig. 3.

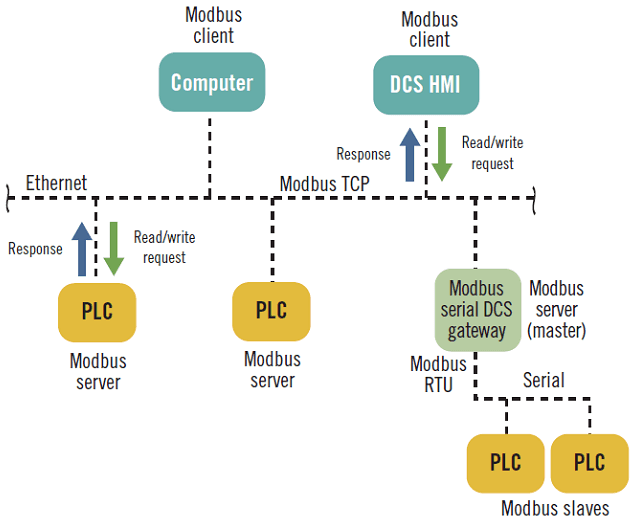

Fig. 3. The principle of messaging exchange

III. Development of the Module for Research of Methods of Transmission of Information

As a module for displaying information we will use an LED matrix of 8 × 8 points. There are various modules of this format. They differ in size, color, principle of management. To create compact devices, there are small modules of a dot-matrix LED matrix of 8 × 8 pixels with red LEDs.

The size of the matrix is 32 mm × 32 mm. The supply voltage of such modules is 1.8 V - 2.3 V. Type of modules 1088AS, connection option - common cathode. The appearance of the modules is shown in fig.4.

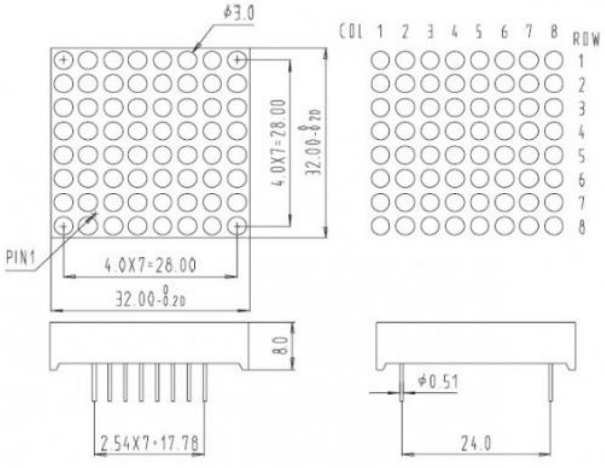

Fig. 4. Appearance of 1088AS modules

Various connection schemes are used to control LED arrays. This can be a variant with a main controller and powerful output transistors (Fig. 5.), or a variant of control via a high-speed bus based on the SPI interface (fig. 6.).

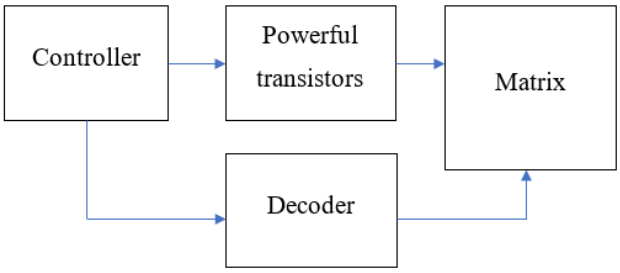

Fig. 5. Control with main controller and powerful output transistors

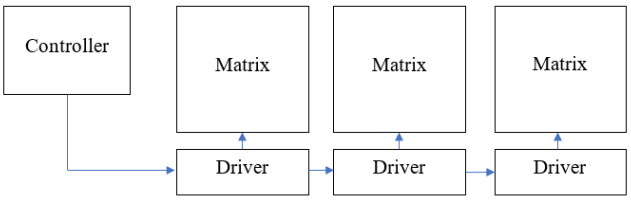

Fig. 6. Control based on the SPI interface

To display the image on the LED matrix, we will use the library Adafruit_GFX. With it, you can organize the output to the LED screen of any image or text.

The library has many features for working with images and text. For example, the "drawChar" function is used to display text.

This function uses the following parameters:

- x and y are the coordinates of the symbol;
- color – the color of the symbol (in the case of a monochrome matrix, the value HIGH, LOW is used);
- bg – background color (in the case of a monochrome matrix, the value HIGH, LOW is used);

- size – scaling factor.

Example of use:

matrix.drawChar(1, y, 'K' HIGH, LOW, 1)

In this example, the "K" symbol will be displayed from the first position of the LED screen.

An example of the application of this function in the program is shown in fig.7.

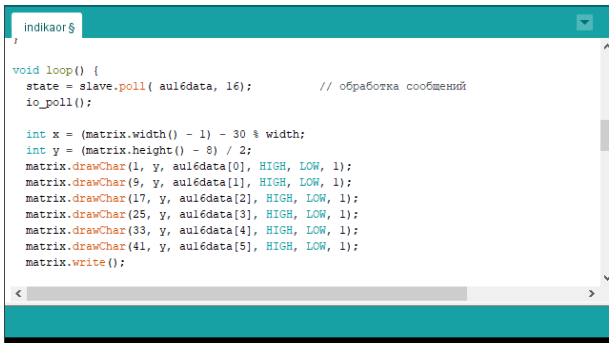

Fig. 7. Example of using the drawChar function

In this example, each character is displayed in a specific character space indicated by the X coordinate. To cycle the text and create the effects of a running tape, you must create a loop and sequentially change the coordinates of the text output each iteration of the loop.

In fig. In Fig. 8 shows an example of creating the effect of a running string.

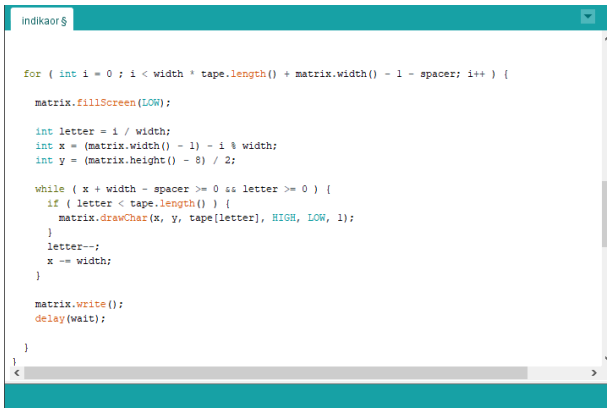

Fig. 8. Example of creating a running string effect

As you can see, the X coordinate in the loop changes with each iteration per unit.

The Max72xxPanel library is used to work with the MAX7219 drivers. This library is designed for the interaction of 8 × 8 LED arrays with a common anode on the chip MAX7219 and Arduino (Fig.9).

The Max72xxPanel library has a setRotation function that sets the orientation of the image on the matrix. For example, if we want to rotate the text 90 degrees, we need to call setRotation with the appropriate arguments immediately after calling the setIntensity function:

matrix.setRotation (0, 1)

The first parameter is the index of the matrix, in our case it is zero; the second parameter is the number of turns by 90 degrees.

The library uses the SPI interface to control the drivers, so the program must also connect the module "SPI.h".

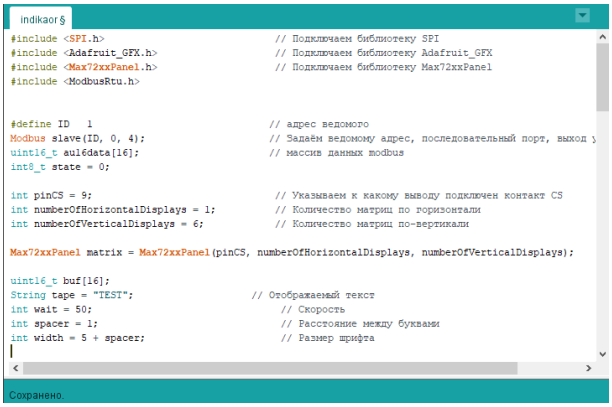

Fig. 9. An example of using this library

The ModBusRtu library was selected to work with the ModBus protocol. To interact with it, the program must create an object by specifying in its ModBus constructor address, serial port number, output number that controls the transmission (for RS485):

ModBus slave (ID, 0, 0)

Then define an array of ModBus registers:

matrix.drawChar(1, y, 'K' HIGH, LOW, 1)

After that, when starting the program, configure the serial port of the slave

slave.begin (9600)

In the main cycle of the program it is necessary to call the function of processing of ModBus messages:

state = slave.poll (au16data, 11)

You can then process the data and save the required variables in the ModBus registers.

The standard provides a separate table for each data type, but a feature of the applied library is that all registers are stored in one array in the form of overlapping tables.

The structure of the registers of the controller will look as follows, as shown in table 1.

TABLE I. STRUCTURE OF REGISTRIV CONTROLER

Register	Bit	Name	Type	ModBus Address	Access
Au16data[0]	0 1 2 3	DT0 DT1 DT2 BTN	discrete	0 1 2 3	read
Au16data[1]	0 1 2 3	CL16 CL17 CL18 LED	coil	16 17 18 19	read/write
Au16data[2]		INPT3	input	2	read
Au16data[3]		INPT4	input	3	read
Au16data[4]		INPT5	input	4	read
Au16data[5]		HOLD6	holding	5	read/write
Au16data[6]		HOLD7	holding	6	read/write
Au16data[7]		HOLD8	holding	7	read/write

During the operation of the program, the data transmitted by ModBus is written to the registers au16data []. The register number is defined in the data packet transmitted by the RS-485 interface.

According to the standard, information is written to the Holding Registers – 16-bit outputs of the device, or internal values.

Available for reading and writing. Range of addresses of registers: from 40001 to 49999. Contain functions: "03" – reading of group of registers, "06" – record of one register, "16" – record of group of registers. Each character is transferred in HEX format. The character number is taken from the ASCII table.

For example, to transmit the word "ModBus" to the screen, you need to create the following data packet:

01 10 00 00 00 07 00 00 4D 00 6F 00 64 00 42 00 75 00 73 00 72 AC

The following parameters are specified in this package:

- device number: 01;
- function number: 10h (function 16 is used for writing in several registers at once);
- starting address: 00 00;
- number of registers: 00 07 (7 registers);
- bytes "00 00 4D 00 6F 00 64 00 42 00 75 00 73 00 72 AC" form the word "ModBus" (the first two bytes are ignored by the library).

Figure 10 shows an example of the interaction of the ModBus protocol.

Fig. 11 shows an example of the transfer of the word "KITAM" on the board.

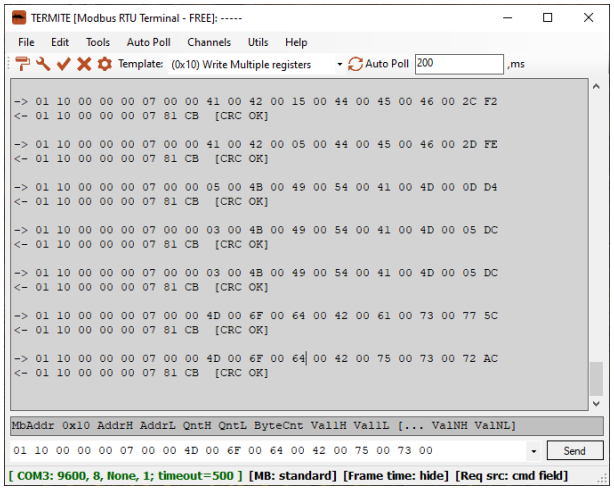

Fig. 10. Interaction of the ModBus protocol with the developed layout

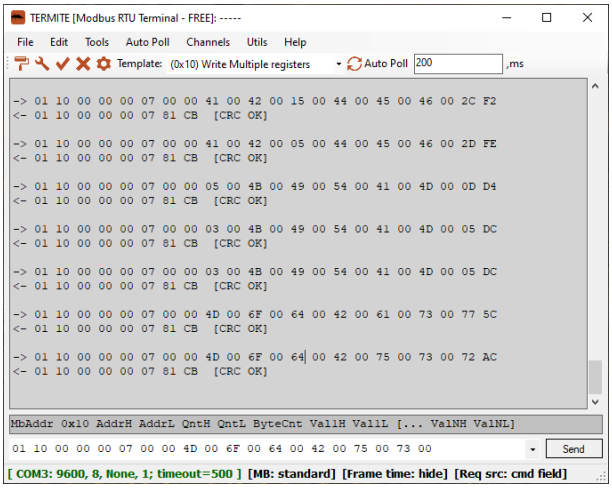

Fig. 11. Example of passing the word "KITAM" on the board

After transferring the data to the layout, the text will be displayed on the screen as shown in fig.12.

Fig. 12. Display the transmitted characters on the scoreboard

Fig. 13. The result of displaying information

CONCLUSIONS

This paper provides an example of using the ModBus industrial protocol to control an LED information board. The developed device can be used in a laboratory workshop to study the work with industrial protocols.

To control the layout via the RS-485 interface using the Modbus protocol, you need to select two modules:

- USB-to-RS-485 interface converter on the PC side;
- RS-485 to TTL converter on the layout side.

The protected USB-RS485 adapter module on the FT232 chip is selected as the USB to RS-485 interface converter on the PC side.

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Development of a Telegram Bot for Receiving Data from OPC Servers

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***Abstract*—It is important to develop programming of the embedded control system which allows the real-time system to change and actually program the built-in control system based on the PLC. Chatbot is a computer program developed on the basis of neural networks and machine learning technologies, which can be used to communicate in audio or text format , but chatbot can also be used to program embedded systems without changing the PLC program itself. The purpose of the work is to develop a chatbot in the Telegram service, which can be used to obtain information from embedded systems based on the OPC server and send the necessary information at the request of the user.**

Keywords—OPC, PLC, Telegram bot, Chatbot, embedded control system, data, servers, IoT, IIoT, machine learning technologies.

I. INTRODUCTION

Embedded system - a specialized computer system or computing device designed to perform a limited number of functions, often with real-time constraints. The purpose of the work is to develop a chatbot in the Telegram service, which can be used to obtain information from embedded systems based on the OPC server [1] and send the necessary information [2] at the request of the user. An analysis of platforms and technologies was conducted [3-9]. Among other representatives of chatbots this development is unique, among the Internet in free access there was no similar implementation of the chatbots programmed for this purpose which transferred information from the PLC[3] through the OPC server[4].

Development of telegram-bot for OPC-technology of programming of the embedded control system on the basis of the PLC. Thus, it is advisable to develop a programming system for built-in control system based on PLC.

II. DEVELOPMENT OF THE SCHEME OF DATA EXCHANGE THROUGH THE OPC SERVER

Data exchange of embedded systems based on the OPC server is as follows (fig. 1).

- the configurator itself is configured;
- information from the controllers is sent to the OPC server;
- SCADA-system receives data from controllers by reading data via OPC.
- the telegram bot connects directly to the OPC server and on the command receives data, rewrites necessary variables, controls all process of work.
- he telegram bot sends data to the user, and sends the results of changes.

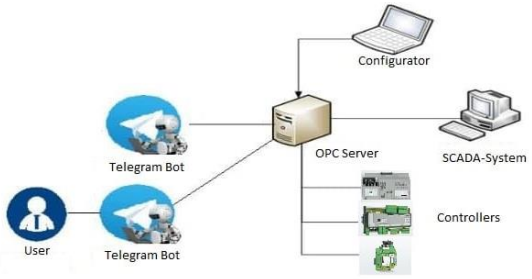

Fig. 1. Scheme of data exchange via OPC server.

The system must perform the task of programming the built-in control system in the following sequence: Bot> server> telegram network> OPCUA server> PLC network.

III. BOT DEVELOPMENT

The first step in programming a chatbot is to obtain its personal token. The personal token is a unique number that the chatbot works on, without it the program will not know through whom requests will be processed. The first step in programming a chatbot is to obtain its personal token. The personal token is a unique number that the chatbot works on, without it the program will not know through whom requests will be processed (Fig. 2).

The token is registered with the command "bot = telebot.TeleBot (" * ")", where "*" is your token. This command sets the token for our telegram bot, without it it will not work.

When we need something from the chatbot, we prescribe a command in the chat and the result is displayed to us. "@ Bot.message_handler (commands = " start '])" with this command we set the necessary condition to start working with the bot, namely, when the user types in the chat "/ start".

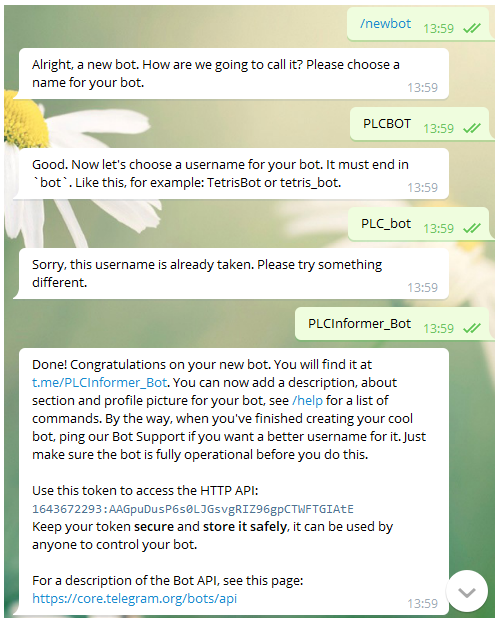

Fig. 2. Example of a conversation with "BotFather".

Next, we specify what will be executed when the user enters the required command (Fig 3).

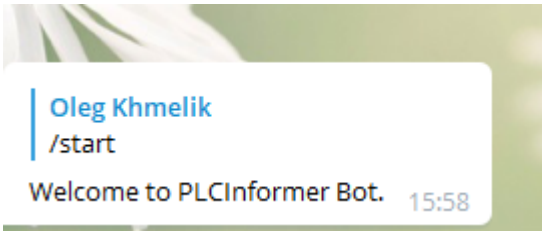

Fig. 3. The reaction of the bot to "/ start".

To read our variables from an embedded system based on OPC, there is a function "opc.properties ('*')", where "*" is the name of our variable, which we learn thanks to the OPC Client utility. To output data from the OPC, we use the binding of the variable to the command. After receiving the data at the end of the function it is necessary to prescribe "opc.close ()" to optimize the use of the connection to the OPC server, without this command after performing the function of connection to the embedded system based on the OPC server does not stop, and re-execution of the command will add more 1 connection without disabling the past. Therefore, it is better to close the communication channel (Fig 4).

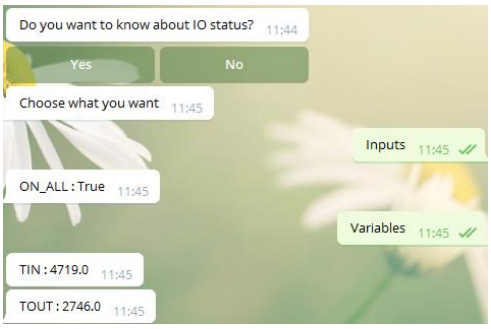

Fig. 4. The result of command processing and information output.

The basis for testing our development of a chatbot for embedded systems based on OPC will be a project in PC WORX with emulation thanks to PC WORX SRT software (Fig. 5).

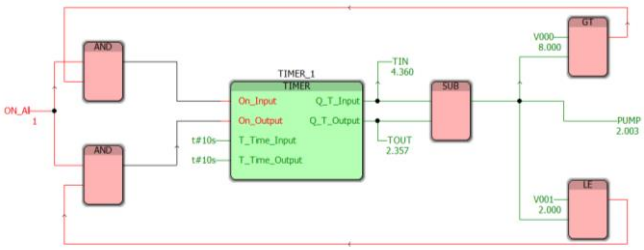

Fig. 5. Emulation thanks to PC WORX SRT in PC WORX

IV. Conclusion

This development Telegram bot is a unique way of user interaction on programming by embedded control systems and exchange of information between them. In the future, the development of this technology can provide remote work for both users and developers of embedded systems for their programming, monitoring and debugging.

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Development of the testbench base on STM32 microcontroller and expansion module

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***Abstract*—The purpose of the development is to create a test layout on the STM32 microcontroller F103C8 series and expansion module. Performing this work had to consider the following steps: analysis of similar devices and expansion modules; develop the spatial structure of the device and its layout; develop the design of the printing module; conduct testing; integrate the test layout and expansion module.**

Keywords—STM32, microcontroller, expansion module, testbench, F103C8, SPI, I2C, GPIO, testing

I. Introduction

A test bench or testing workbench is an environment used to verify the correctness or soundness of a design or model [1]. The Wireless sensor networks (WSN) systems have a lot of problems like security, energy consumption, heterogeneity and other disadvantages that need be solved. Therefore, it is quite difficult to design a sensor network node so that it satisfies the necessary criteria for optimality. If such a node is also used for testing and training, then additional requirements for the construction will be propose to, for example, as in articles of designing microprocessor systems [2] or embedded control systems [3]. Energy monitoring [4] is a key factor for the successful prolongation of life times each nodes in wireless sensor network, for examples reducing the power consumption of nodes [5]. Therefore, can set the task to optimize the structure of the node for as one of approach to designing a wireless sensor network node. One approach is shown in the literature [6].

STM32 is a family of 32-bit microcontrollers from STMicroelectronics. STM32 chips are grouped in series, each using the same 32-bit ARM core.

Performing this work had to consider the following steps: analysis of similar devices and expansion modules; develop the spatial structure of the device and its layout; develop the design of the printing module; conduct testing; integrate the test layout and expansion module.

II. Analysis of Similar Devices and Expansion Modules

We analyzed various approaches to the design of such stands - with the presence of a scheme for additional installation (fig.1) and without it (fig. 2).

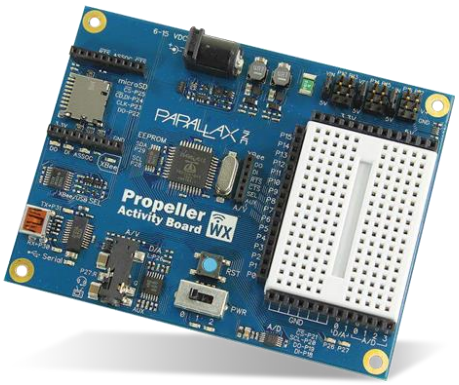

Fig.1 PCB testbench board with additional installation

The stand (fig. 2) is built on a modern element base. The stand includes two standard RS-232C ports, serial Flash memory with I2C interface, program memory and 64KB data memory. The presence of system and peripheral interfaces allows using the stand for debugging any systems.

Fig.2 PCB testbench board with expansion module

III. Development of the Module Structure

Were analyzed STM32 microcontroller F103C8 series (fig. 3).

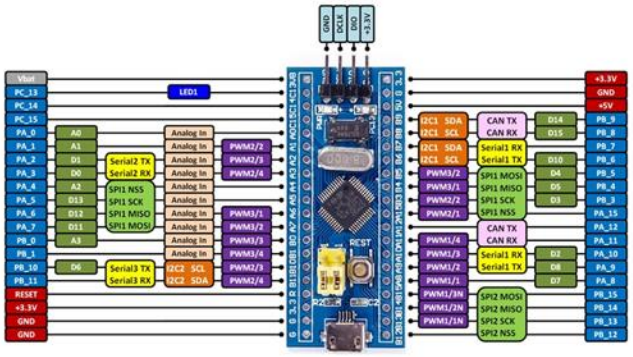

Fig.3 STM32 microcontroller F103C8 series with pireferals

As a result of the analysis and design, a printed circuit board was developed and the module was assembled. The figure 4 shows the appearance of the text layout and its layout.

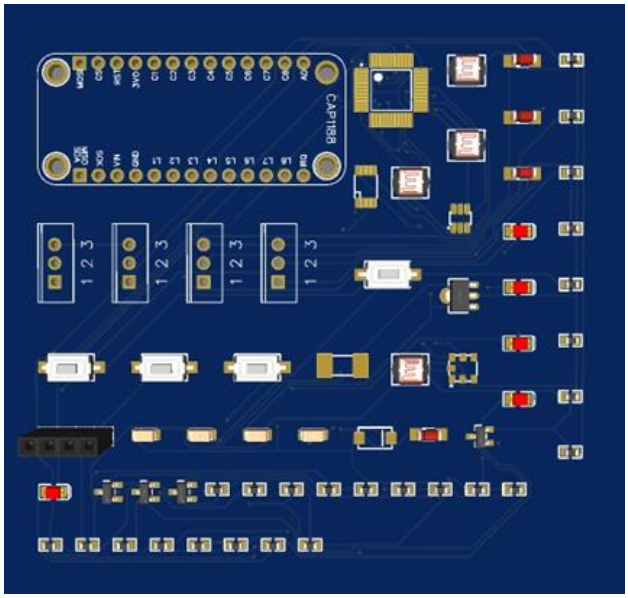

Fig.4 STM32 testbench base on STM32 microcontroller F103C8 series

The developed expansion module is shown in the fig. 5.

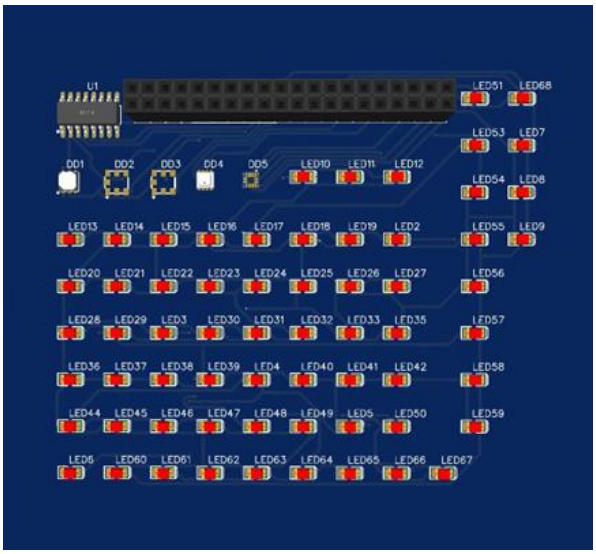

Fig.5 Developed expansion module

The proposed model defining defines different levels of system interaction. Each level performs certain functions in such interaction (fig. 6).

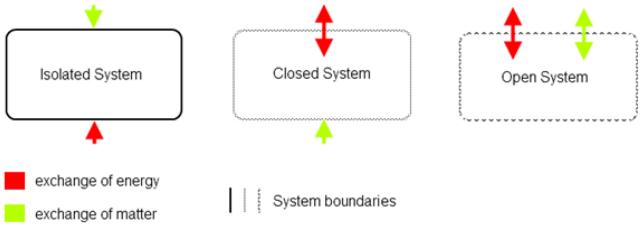

Fig.6 Proposed model for testbench

IV. Conclusion

Similar constructions and modules are analyzed[1,3,6-8]. A test layout based on the STM32 microcontroller has been developed. An extension module for test layouts has been developed. Three different models for testing embedded systems have been proposed.

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Features of the design of a telemedicine complex of a wide profile based on FPGA

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***Abstract*—The article discusses the relevance of the development of a telemedicine complex for the rehabilitation of athletes for the removal of various biological characteristics and data transmission over a distance. The block diagram of the device being developed is presented. The choice of the FPGA component for solving the problems of digital signal processing has been substantiated.**

Keywords—FPGA, biological signal, digital signal processing (DSP), medical complex

I. Introduction

In modern society, taking into account the current epidemiological situation caused by COVID-19, telemedicine has become widely used, both in the world and, in particular, in Ukraine. The main purpose of using telemedicine methods is to ensure equal access to medical services of appropriate quality. For example, providing medical care to a patient in cases where distance and time are critical factors. Also, the use of telemedicine will ensure the formation of the integrity of medical information about the health of patients and contributes to the creation of a single medical space. The functional purpose of the telemedicine complex is determined in accordance with the necessary and sufficient requirements for monitoring the patient's condition. And for patients with chronic diseases and the elderly, this is extremely important. Also, the telemedicine complex can be used to monitor the condition of athletes during training, fitness training, rehabilitation and so on.

The rehabilitation process after injuries and fractures is long and difficult. In accordance with this, the rehabilitation program should be specific, and a necessary aspect in the system of complex rehabilitation of athletes is the use of non-drug methods [1]. Based on the importance of using such rehabilitation methods, it is advisable to develop a device for automated control and restoration of body reactions during rehabilitation.

II. Designing the Structure of a Telemedicine Complex for the Rehabilitation of Athletes

When analyzing patent searches and products of leading companies, it is urgent to develop a wearable device for recording biological indicators of athletes, which are basic for the restoration of the musculoskeletal system, with subsequent automatic signal processing and data transmission to various devices.

One of the variants of this device implementation “Fig. 1” may include:

1) Patient.
2) Control unit.
3) Reader.
4) Block of sensors.
5) Signal processing device.
6) Bluetooth interface or NFC interface.
7) Power supply (such as ultra-thin battery).
8) Memory block.

The device, using the sensor unit (4), reads the biological characteristics of a person (1) with which the sensor device comes into contact. Then it transmits the information to the signal processing device (5), which is programmed using a PC. After digitization, the analysis of the data obtained is carried out. The calculation results are stored on a data carrier (8), and during further examination are compared with the initial results to assess the effectiveness of therapeutic measures and adjust the treatment plan. With the help of the wireless data transmission unit (6), the processed biological information is transmitted to the reader (3). The reader can display to the user and / or transmit sensor data to a remote location for further processing. The physician may revise the data or conduct further analysis and use the data or information to assist in treatment. The power supply unit of

the device (7) ensures the operability of the device and voltage stabilization.

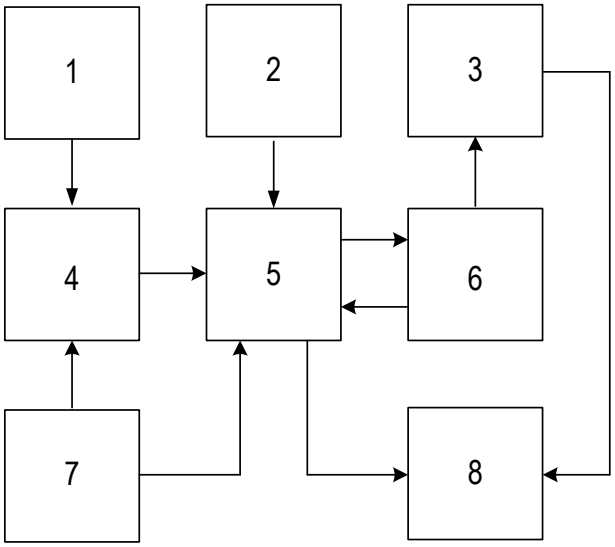

Fig. 1. Block diagram of a portable telemedicine complex.

III. Selection of a Device for Signal Processing

Data processing in such systems requires intensive solution of DSP problems and a large number of channels. When choosing a device for signal processing, it is also worth considering a number of parameters:

- system performance;
- energy consumption;
- number of components and form factor of the system;
- the possibility of upgrading the system;
- economic parameters.

Building on the dynamics of healthcare to deliver superior patient care at a lower cost, enhanced imaging, transmission medical imaging and video data there is a tendency to implement tasks on PLC [1].

The peculiarity of the FPGA structure is that each logical block usually has a small number of inputs and one output. This allows more complete use of the internal resources of the microcircuit. At the same time, for FPGAs, the term "maximum clock frequency" refers to the most favorable conditions for chip tracing - all connections are made using short circuits, connected programmable cells are located side by side, the maximum length of accelerated transfer circuits is limited. Unsuccessful routing reduces the allowable clock speed accordingly, but it is very important that after the design is completed, it remains constant [2-6].

A typical logical block is built on the basis of a ROM, in the cells of which the truth table of the combinational circuit is written. The performance of FPGAs on DSP tasks is the higher, the higher the parallelism of processing is used in the algorithm, which accordingly leads to an increase in the amount of logic on the chip. In addition, an important advantage of FPGAs is their ability to provide not only high processing speed, but also continuous processing and stable speed [5-11].

IV. Conclusion

In FPGA, it is also possible to implement processors (for example, a processor on logical cells such as MicroBlaze), however, it is absolutely not necessary to pass the entire stream of processed data through this processor. Moreover, it is recommended to implement high-performance digital processing using DSP resources operating without direct and constant control of the processor [5]. The processor core can perform interface organization, tuning, monitoring, loading coefficients and other operations that are too difficult to implement in hardware. At the same time, a single processor core can control several hundred DSP-blocks of FPGAs, which constantly process the incoming stream even without the participation of the processor. The proposed option for using, in this complex, an FPGA board can be quite advantageous for parallel processing of different biological signals. It seems promising to continue research in the field of FPGA application in medical systems.

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Digital System for Customs Inspection of Baggage in High Security Areas

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***Abstract*—This article discusses the development of a three-energy digital system for customs inspection of luggage and hand luggage in airports and high-security areas, which will provide not only easy monitoring of luggage and hand luggage, but also security screening. The peculiarity of such a system is the use of scintillation crystals in the control systems of customs baggage inspection. And also the scheme of three-energy digital radiographic system has been developed, which gives the possibility of fast and safe luggage monitoring.**

Keywords—digital customs control system, scintillation crystals, detector, security, controlled area.

I. INTRODUCTION

The Ukrainian customs service plays an important role in the regulation of the country's foreign trade. Its main task is to ensure compliance with the measures of customs and tariff regulation, as well as to create conditions conducive to accelerating the turnover of goods across the customs border. Accordingly, the customs border is one of the places with a high concentration of people, which leads to the need for increased vigilance and increased safety measures. Thirst for profit, unemployment, the opportunity to earn "easy money", all this encourages people to commit crimes, to illegally import and export prohibited goods across the border. Which, in particular, may entail damage not only to an individual entity, but also lead to an international conflict. For example, careless, inept work at the customs border can lead to the hijacking of aircraft and the death of people. In contrast to the activities of intruders and military groups, the customs services present a set of measures and means to protect the border from unauthorized import and export of contraband. The complex includes the latest developments in engineering and technical means, regulatory legal acts, the work of the reaction forces, the work of operators of detection devices and much more, which in total makes it possible to timely detect, seize and dispose of contraband.

The globalization of the economy, the possibility of using modern information technologies induce the Ukrainian customs service to change its procedures and rules for conducting customs control, taking into account the ongoing changes and determine the strategy of customs control based on the system of risk assessment measures.

To conduct the study, the goal was set - to determine the current state, problems of use and directions for the further development of technical means of customs control.

Therefore, the tasks of the study are:

- determination of the range of problems associated with the development and implementation of the developed system { {1}} - analysis of the modern technical means of customs control;
- calculation of the preamplifier;
- development and calculation of the economic component and the safety of human life.

In modern conditions, the customs service, on the one hand, it should ensure the interests of the state in the field of foreign trade, counteract threats to national security, and on the other, create favorable conditions for participants in foreign economic activity. These principles are laid down in the Concept for the development of customs authorities, which leads to constant modernization and replacement of existing equipment, which in turn confirms the relevance of development in the field of information security, in particular, scanning systems.

II. TYPES OF SCANNING INTROSCOPES FOR BAGGAGE INSPECTION

When transporting prohibited and dangerous goods for their inspection at borders and at airports, scanning X-ray nitroscopic systems are used to control baggage and carry-on baggage. At the same time, the requirements for this device are highly sensitive electronics, efficient radiation detectors, precision mechanics, and modern software. A line of detectors of the STs-FD type is used as a receiving device. A distinctive feature for most types of Ukrainian scanners is their dual energy with the use of two lines of detectors. The low-energy line contains exclusive crystals.

Considering digital radiography using only X-ray and Y-radiation, three most common and widely used types of systems can be distinguished.

- Digital radiographs using luminescent screens with subsequent transformation of light through an optical system and registration on a CCD matrix
- Digital flat panel radiographs based on amorphous silicon.
- Digital radiographs using a line of detectors of the STs-FD type - up to 1024 detectors in the line.

The table (p. 356) shows the comparative parameters of these systems. It can be seen from the table that the system with a line of SC-PD detectors, being significantly inferior to the first two types in terms of resolution, is much superior to them in contrast sensitivity, as well as in the linear portion of the dynamic range (4-5 orders of magnitude). different types of objects - from miniature microcircuits, the equivalent of a steel thickness of several hundred microns, to heavy vans with the possibility of shining through in the equivalent of a steel thickness of 350-400 mm.

III. Features of Dual- and Multi-Energy Digital Radiography

The use of the principle of two-energy detection opens up new possibilities for digital radiography. Increasing the information content due to the identification of areas with a given chemical composition in the controlled object. This is achieved due to the definition of.

IV. Appointment of Scanning Introscopes for Inspection OF Baggage, Hand Luggage

The baggage screening system is designed for customs control of hand luggage and passengers' baggage in order to identify items prohibited or restricted for movement across the state border, and provides:

- High-quality visual inspection of the contents of the baggage without opening it, distinguishing between organic and inorganic substances.
- Radiation level safe for humans, close to the natural background.
- High control performance.
- Radiation dose safe for photosensitive materials.
- A wide range of services for the operator.

V. The Principle of Operation of the Scanning System for Inspection of Baggage, Hand Luggage

The X-ray introscopic complex for transport and baggage control is designed to control the operational display on the monitor screen of the shadow image of the controlled object and the items inside it, to identify prohibited attachments. A shadow X-ray introscopic image is formed as follows:

- The object of control (container or van) with the help of a transport platform moves through one plane of X-ray beams in a direction perpendicular to these planes, the radiation source is a linear electron accelerator with a target-type device.
- X-rays, attenuated depending on the properties of the material and its thickness, falling on the detectors located in the horizontal and vertical rulers, are converted into electrical signals.
- Electrical signals are amplified, converted and digitally transmitted to a PC.
- The PC, according to a special program, processes the information received and forms a shadow image of the inspected object of control (OC).

VI. The Composition of the Scanning System for Inspection of Baggage, Hand Luggage

X-ray introscopic complex for control and inspection of customs cargo includes:

- Radiation system (SR).
- Detection and information processing system (SDOI).
- Object transportation system (STO).
- Radiation monitoring system (SRM).
- Control system (CS).
- Power supply system (SES).

Radiation system functions. An image of the controlled object is formed in Y-rays with the maximum possible equivalent of the thickness over steel.

Functions of the system for detecting and processing information. In the system for detecting and processing information, X-ray radiation, attenuated depending on the properties of the material and its thickness, falling on the detectors located in the horizontal and vertical rulers, are converted into electrical signals. Then, using the control system, synchronizing signals for polling the detector lines and the amplification factor of the signals taken from the detectors are generated.

Functions of the object transportation system. The controlled object is moved through the aspect planes of X-ray beams along the transport platform.

Functions of the radiation monitoring system. Requirements for the safety of operation of the X-ray nitroscopic complex and the presence of a high level of hard X-ray radiation make it necessary to include a radiation monitoring system in the complex. The control PC through the control system collects information from the sensors of direct and scattered Y-radiation, sensors of neutron radiation and radiation of the object, and, if necessary, through the sound and light alarm system, makes the appropriate notification.

Functions of the control system. The control system of the X-ray introscopic complex provides control of the operating modes of the complex, monitors the functioning of the complex and ensures safe operation:

- Control of impulse power supply of the X-ray accelerator
- Control and control of the rotation of the forming X-ray beam of the collimator.
- Control of vacuum maintenance in the accelerator.
- Control of the auto-tuning of the frequency of the accelerator pump magnetrons.
- Monitoring and control of the power supply system of the radiant installations.

All systems of the complex are connected by means of a local information and computer network with centralized control. The control system is organized in the form of a network with parallel connection of controlled devices to the

control processor based on the RS-485 serial data exchange interface.

The block diagram of the hardware is shown in the figure

It consists of the following structural units: { {1}} :

- Control PC.
- Controllers of management (KU) of peripheral devices (PU).
- Matched active plugs (AZ).

VII. Features of Dual- and Multi-Energy Digital Radiography

The use of the principle of two-energy detection opens up new possibilities for digital radiography. Increasing information content by identifying areas with a given chemical composition in a controlled object. This is achieved due to the determination of the attenuation coefficients of the test object materials for two different radiation energies. There is one emitter, but the supply of two different voltages to the tube is modulated. The line of detectors is one, but the signal is registered synchronously for different voltages per emitter. This technology provides high detection rates with good throughput.

Five independent fan-shaped X-rays shine through each piece of baggage. Three x-ray sources, mounted in a specific position, generate x-rays at five different angles. These five radiation angles provide the information you need to provide the highest level of detection. Connection to a common computer network unites all the necessary system components of the system and provides a variety of information in the shortest possible time. Since it is about security, decisions must be made immediately.

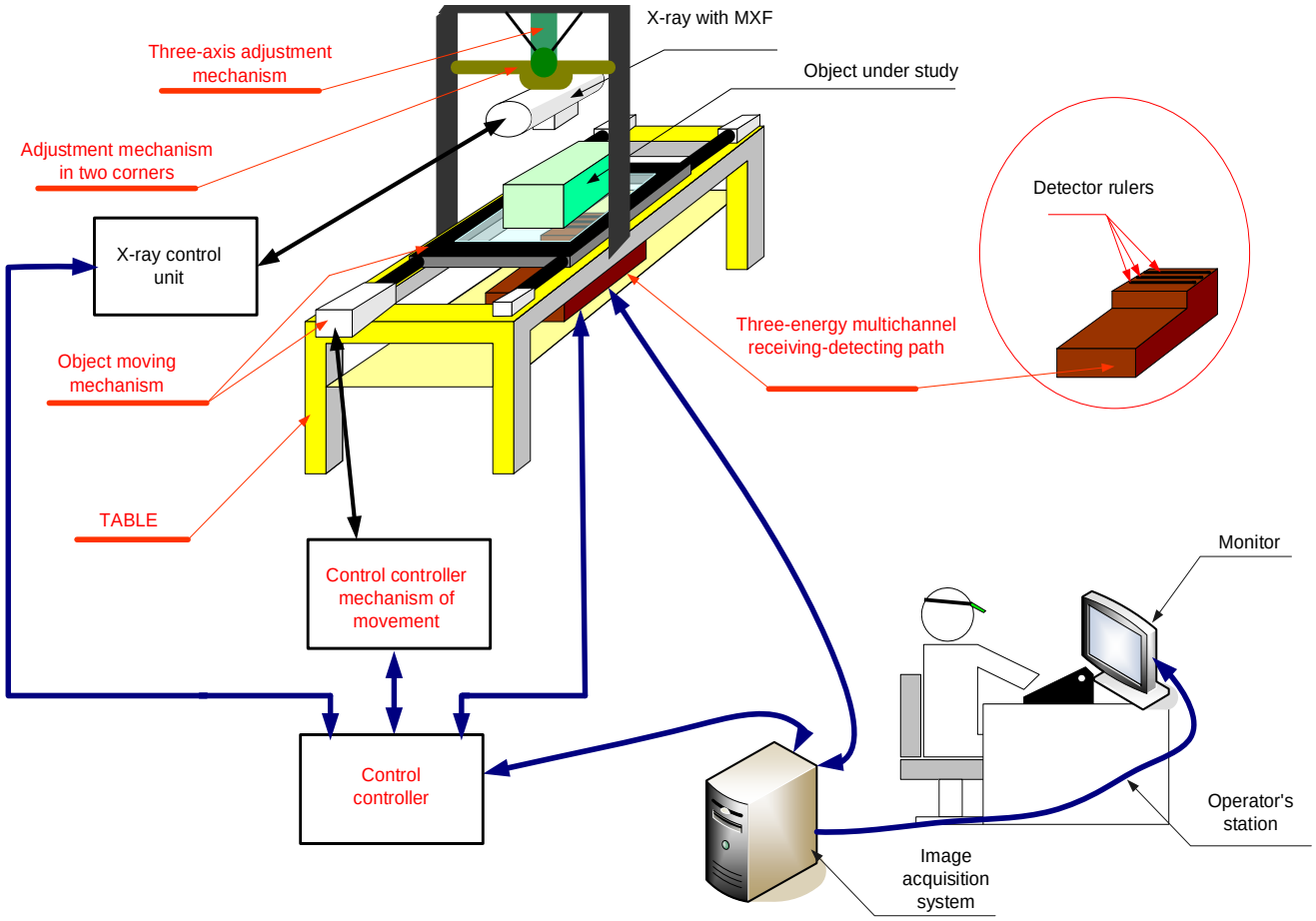

Fig. 1. Block diagram of a three-energy digital radiographic system.

VIII. Conclusions

At the present stage of development of society, people have not yet learned to restrain their passion for easy money, so the number of violations of the customs code will only grow.

The hard work of ensuring security falls on the shoulders of ordinary border and customs officials. The lives of many people depend on their immediate actions and efficiency.

In the conditions of the market and competition, entrepreneurship and technology keep pace with the times.

The leakage of classified information leads to catastrophic consequences, so in the new conditions there is a mass problems associated with ensuring the safety and transportation of baggage.

Technical means of information protection come to the rescue in the difficult struggle for the preservation of borders.

Science and technology does not stand still and the capabilities of attackers practically do not have borders, the latest technologies allow them to come up with all the more perfect methods of smuggling. That is precisely why workers in the field of developing technical means of protecting information will always have a job.

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Designing the Structure of a General-Purpose Telemedicine Complex

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***Abstract*—Taking into account modern trends, the analysis of the construction principles of telemadic systems, networks and complexes is presented in the work. The general structure of providing telemedicine services is developed. Structures of realization of portable and mobile telemedicine complexes are offered. Infocommunication systems and networks for implementation in mobile telemedicine complexes are analyzed. The advantages of using the sensor mobile body area network of the IEEE 802.15.6 WBAN standard in mobile telemedicine complexes are justified.**

Keywords—telemedicine, telemedicine complex, medical services, device structure, microcontroller, sensor network , wireless sensor body area network

I. INTRODUCTION

In modern society, taking into account the current epidemiological situation caused by COVID-19, telemedicine has become widely used, both in the world and, in particular, in Ukraine.

Telemedicine is a new direction of medical services, which is rapidly developing and being implemented in everyday life. Telemedicine covers several diverse areas - medicine, telecommunications, information technology. This field of medical services allows the patient and the doctor to save time and effort, because communication takes place online. This is relevant both for residents of megacities and for people living in rural areas. This approach provides equal access to quality health care for patients in all parts of the country. Also, in general, telemedicine significantly reduces the cost of treatment, improves the quality of diagnosis and realizes the possibility of remote monitoring of health, which in turn is economically proven, both for the patient and for the country as a whole [1-3].

As part of the World Health Organization's (WHO) telemedicine policy in 1997, the following definition was proposed. Telemedicine is a method of providing health care services where distance is a critical factor. Services are provided by health professionals using information and communication technologies to obtain the information necessary for the diagnosis, treatment and prevention of diseases [1-5].

II. DEVELOPMENT OF THE TELEMEDICAL COMPLEX STRUCTURE

The functional purpose of the telemedicine complex is determined in accordance with the necessary and sufficient requirements for monitoring the patient's condition. And for patients with chronic diseases and the elderly ones, this is extremely important. Also, the telemedicine complex can be used to monitor the condition of athletes during training, fitness training, rehabilitation period and so on.

Monitoring can be classified by purpose, including: heart monitoring; hemodynamic monitoring; respiration monitoring; neurological monitoring; monitoring of blood glucose levels; body temperature control and more.

The telemedicine complex can have a mobile or portable structure. The proposed general structural schemes for the construction of portable / mobile telemedicine complexes are shown in Fig. 1 and Fig. 2.

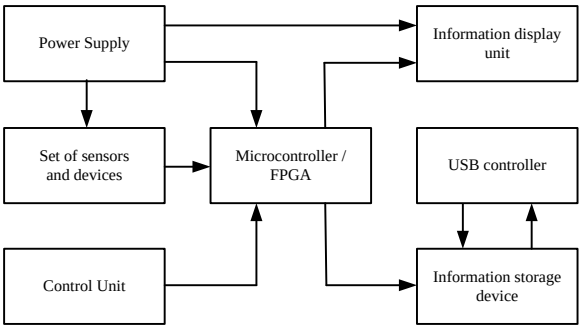

Fig. 1. Portable telemedicine complex.

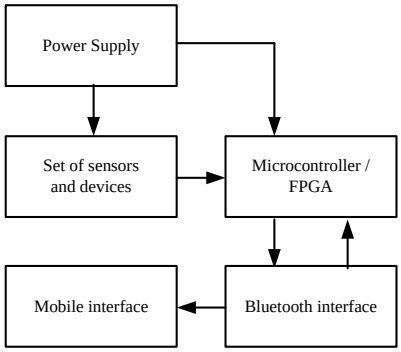

Fig. 2. Mobile telemedicine complex.

According to the analysis conducted, it is advisable to use FPGA and sensor network to develop a telemedicine complex or system [6-11].

In the given structure of a mobile telemedicine complex (fig. 2) it is offered to use a sensor mobile body network of WBAN technology.

WBAN is a sensor mobile body network of the IEEE 802.15.6 standard. The goal of IEEE 802.15.6 standard is to provide an international standard for low-power, short-range, and highly reliable wireless communications within the human body environment, while maintaining a wide range of data rates for a variety of applications. This standard describes short-range wireless communication near or inside the human body (but not limited to humans). It uses existing industrial scientific medical (ISM) bands as well as frequency bands approved by national medical and/or regulatory authorities. It is necessary to maintain quality of service (QoS), extremely low power consumption and data transfer speeds of up to 10 Mbps, while adhering to strict rules of non-interference if necessary. This standard considers the effect on portable antennas due to the presence of a person (depending on the man, woman, slim, fat, etc.). The form of the radiation pattern is used to minimize the specific absorption coefficient (SAR) required in the body, as well as changes in characteristics as a result of user actions.

The IEEE 802.15.6 standard aims to ensure confidentiality, authentication, integrity, protection against interference and protection against reproduction. All nodes and hubs must select three security levels: insecure connection (level 0), authentication but without encryption (level 1), and both authentication and encryption (level 2). In the security matching process, the node and the hub must jointly select the appropriate security level. In unicast, the previously shared or new shared key (MK) is activated. Then a paired temporary key (PTK) is created, which is used only once per session. Multicast creates a temporary group key (GTK) that is used in conjunction with the corresponding group. All nodes and hubs in the WBAN must go through certain steps at the MAC level before exchanging data. The procedure used is the security association. This is a procedure to identify the node and the hub for each other; to setup a new shared key (MK) that was shared between them, or to activate an existing MK previously shared between them. The IEEE 802.15.6 security association is based on four key negotiation protocols.

In the IEEE 802.15.6 standard as information carriers it is offered to use pulse signals of three types: pulses with linear frequency modulation (chirp pulses), 58 chaotic pulses (chaotic pulses) short pulses (short pulses shape).

While building IEEE 802.15.6 sensor networks, as for similar IEEE 802.x networks, there is an urgent problem - the energy efficiency of the sensors used, which depends on the parameters of the sensor life cycle, network reliability (the probability of data exchange between two nodes in a certain time interval) and the radius transition of the message.

III. Conclusion

Telemedicine systems implement modern trends in the development of medical services. But they fulfil an important function of real-time biological indicators monitoring in various spheres of medicine and sports by means of telemedicine complexes. It is the fact that indicates the urgency of the tasks for the development of a telemedicine complex of automated control. Such a complex based on a modern microcontroller system or FPGA is going to measure a wide range of biometric indicators and is able to record, transmit and store the collected information. In this complex it is offered to use a sensor mobile body network of the IEEE 802.15.6 standard as a quite reliable wireless communication utility supporting a wide range of data transfer speeds.

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Aspects of Quality Assurance of the Educational Process of Higher Technical Education

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***Abstract*—The principles of quality assurance of higher education are considered in the work. The analysis of aspects of quality assurance of the educational process of higher technical education on the example of Kharkiv National University of Radio Electronics is given. Measures to develop a quality system of higher education at the university level are proposed as well.**

***Keywords—higher education, technical education, quality of education, educational process, microcontroller, FPGA, educational laboratory, remote laboratory*.**

I. INTRODUCTION

Improving the quality of higher education is a challenge today. As part of the increase in the development of the industrial revolution, the requirements for the level and quality of higher technical education are increasing.

Maintaining the appropriate level of quality of the educational process of higher technical education is, on the one hand, compliance with legislation and regulations [1, 2], on the other hand, the reputation of the university, public relations, demand for specialists, interest of employers, etc. This problem is also actual with the transition to distance learning due to the epidemiological situation.

Regarding the construction of the appropriate level of quality of education in higher education institutions, a number of normative documents, decisions, regulations, projects, measures, regulations, etc. have been developed [2]. But these are general decisions and proposals that require an authentic approach in each specific institution of higher education.

All efforts of the university community should be aimed at avoiding, preventing and stopping the manifestations of academic dishonesty through teaching, leadership and mentoring, as well as by creating a positive, favorable and virtuous educational and scientific environment [2].

On the example of Kharkiv National University of Radio Electronics, by approximating the existing experience and taking into account the specifics of the institution of higher education, a number of normative administrative documents for internal use have been developed [3-6].

According to the analysis, the following problematic issues can be identified to ensure the quality of the educational process of higher technical education: complex, cumbersome, high-cost technical equipment; technical equipment with specific operating conditions; unique technical equipment; equipment without the possibility of full-fledged remote connection; availability of highly qualified scientific and pedagogical staff; introduction of modern scientific and technical solutions in the educational process, etc..

II. GENERAL PRINCIPLES OF QUALITY ASSURANCE OF THE EDUCATIONAL PROCESS

Quality assurance policy and related processes are the basis of a coherent institutional quality assurance system, which forms a cycle of continuous improvement and contributes to the development of the university. The policy supports the development of a culture of quality, within which all internal parties take responsibility for quality and are involved in quality assurance at all levels of the institution. In order to facilitate this process, the policy should have an official status and be available to the general public [2].

Quality assurance policy is most effective when it reflects the link between research, teaching and learning, and takes into account both the national context in which the institution operates and its institutional context and strategic approach [2]. This policy supports: the organization of a quality assurance system; faculties, departments and other structural units, as well as management, teachers and students to take responsibility for quality assurance; academic honesty and

freedom, watching for demonstrations of academic fraud; prevention of any manifestations of intolerance or discrimination against students or teachers; involvement of external parties in quality assurance.

The policy is implemented through a number of internal quality assurance processes that ensure the participation of various parties within the institution. The ways of implementation, monitoring and revision of the policy are guided within the autonomy of the university. The quality assurance policy covers all aspects of the university's activities.

III. Particular Qualities of the Educational Process of Higher Technical Education

Let's consider the features of the educational process of higher technical education on the example of Kharkiv National University of Radio Electronics (NURE). Within certain autonomy, the university has developed a number of basic administrative documents that regulate the educational process [7-11].

A regulation on the organization of the educational process in NURE is the main normative document governing the organization and conduct of the educational process in NURE [7].

The normative basis of the organization of the educational process at the university is: the Constitution of Ukraine; laws of Ukraine "On education"; "On higher education", "On scientific and scientific-technical activities"; administrative normative and legal documents of the President of Ukraine, the Cabinet of Ministers of Ukraine, the Ministry of Education and Science of Ukraine, other ministries and departments; NURE Charter; NURE administrative documents, etc.

In the content of the Regulation on the organization of the educational process in NURE is presented [7]: Regulatory framework for the organization of the educational process; Degree system of education; Higher education standards and educational programs; Curricula, working curricula, individual student curricula; Schedule of the educational process for the academic year; Timetable; Language of instruction; Forms of organization of the educational process and types of educational classes; Features of the organization of the educational process; Transfer, renewal and expulsion of higher education applicants; Quality assurance system of the educational process; Rights and responsibilities of participants in the educational process; Educational time of applicants for higher education; Working hours of scientific and pedagogical, pedagogical and scientific workers.

Peculiarities of the educational process in NURE have been developed by the best scientific and pedagogical workers using the accumulated experience of the university and new scientific and technical trends of today.

The result is the developed methods of ensuring: the distribution of time for theoretical and practical training of higher education; conducting laboratory and practical classes in accordance with the educational components; etc.

Based on the results of the analysis, it can be concluded that the educational process in NURE for technical specialties is provided at a high level according to the results of accreditation and licensing activities within the university [12].

IV. Proposals for Ensuring and Developing the Quality of the Educational Process of Higher Technical Education

The main principles, proposals and guidelines for the quality assurance system of educational activities in NURE are set out in [4], which can be generally described in the structure (Fig. 1).

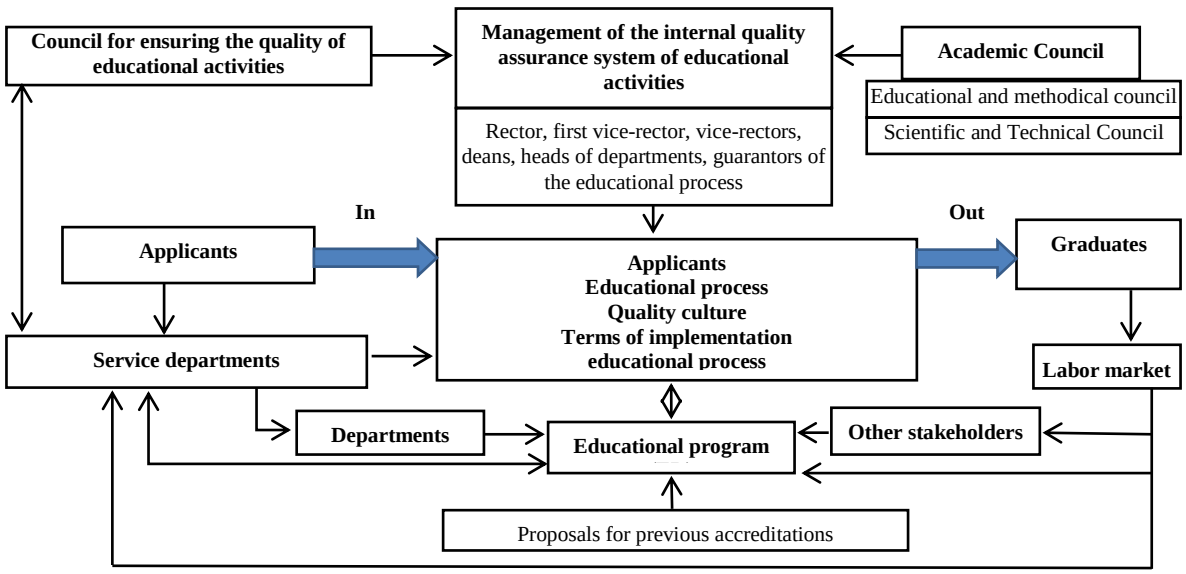

Fig. 1. The structure of the system of internal quality assurance of educational activities.

The University provides transparent and defined rules for participants in the educational process at all stages of education.

At the level of scientific and pedagogical workers, as participants in the educational process, there is a constant work to ensure the quality of educational activities within the competences and taking into account the guidelines of the university [13-20].

In order to develop the system of quality assurance of educational activities in NURE University joins the study of world best practices. For example, the university joined the Academic IQ Academic Integrity and Quality Initiative Project [21, 22]. The Academic IQ project is implemented by the American Councils for International Education in cooperation with the Ministry of Education and Science of Ukraine, the National Agency for Quality Assurance in Higher Education and with the support of the US Embassy in Ukraine.

One of the key tasks of the Academic IQ Project is to create an effective model for monitoring the quality of education, identifying key problems and causes of violations of the principles of academic integrity by participants in the educational process, and, as a result, improving the quality of education at the university [21].

V. Conclution

Ensuring the quality of the educational process of higher technical education is an integral and key factor in training a qualified and in-demand specialist in the labor market. According to the analysis of best practices for quality assurance in higher education, this is a process that should demonstrate the positive dynamics of building a quality assurance system for the educational process as a whole and have the support and adherence of all stakeholders in the educational process. Also, ensuring the appropriate level of quality of the educational process is not possible without institutional support at the level of society and the state.

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