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Miniaturization of Control Devices on Programmable Logic Chips

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***Abstract*—The paper is devoted to solving the topical scientific problem of developing the structures and methods for synthesis of the combined finite state machines (CFSM), aimed at reducing equipment costs when implementing the CFSM logical scheme in the basis of programmable logic integrated circuits such as FPGA and CPLD.**

Keywords—combined FSM, FPGA, CPLD, logic circuit, embedded memory, pseudo-equivalent states.

I. INTRODUCTION

In the modern process of designing digital systems on the basis of programmable logic chips (PLC), automated design systems are widely used. At automatic allocation scheme implemented on PLCs, different algorithms of Boolean functions decomposition, which, studies show, do not provide optimal resource utilization chip, which explains the urgency of optimization problems in the implementation of Boolean functions in the PLC structure. The result of this optimization is not only possible reduction of cost and reduction the size of the circuit, but also power consumption and power dissipation minimization, reducing the time of signal propagation, which generally increases the efficiency of the designed circuit.

II. ANALYSIS OF LITERATURE

An overview and analysis of the methods and models of control devices (CD) representation in modern digital systems have been performed. On the basis of the analysis, the systematization of the resulting structures has been carried out and the direction of research has been allocated. According to the direction of research, structures and techniques of synthesis of CFSM that already exist and which are oriented to implementation in the basis of programmable logic are considered.

An overview of the element base and the analysis of the architectural features of FPGA and CPLD programmable logic chips of such well-known manufacturers as Xilinx, Altera (Intel) and Microsemi has been conducted. The technical characteristics of microcircuits are distinguished, due to which it is possible to reduce the hardware costs in the logical circuits of CFSM. A comparison of the characteristics of modern series of FPGA and CPLD chips has been performed.

In the paper, the classification of methods for optimizing the costs of equipment in the implementation of CD in the form of a machine with "hard" logic on programmable logic circuits such as CPLD and FPGA has been considered. Based on the analysis of these methods, it has been concluded that it is expedient to use structural reduction methods for optimizing the CFSM circuits on the basis of the use of hardware resources.

III. METHODS AND RESEARCH RESULTS

You can use such a feature of the FPGA as a heterogeneous structure in the design of the CFSM scheme. This means that three FPGA components can be used to implement the scheme: UT LUT (Look Up Table) elements, Embedded Memory Block (EMB) and programmable interconnects [1 - 4].

We analyzed the ways and models of representation of control devices in modern digital systems. The systematization of control device structures is carried out and the approach of realization of a part of signals of the control device on EMB on the basis of the analysis is offered.

According to the results of the research, it can be noted that the largest reduction in allocated resources is observed for Microsemi chips, the least - for Altera (Intel) chips. The application of the developed structure is most expedient if the number of Moore output signals exceeds the number of Miles output signals [5].

The necessity to implement complex functions (functions of many variables) in the basis of programmable logic circuits, which has design limitations on the number of inputs / terms / outputs, causes the problem of decomposition. To solve it, the use of such methods of structural reduction as the method of replacing logical conditions, the use of pseudo-equivalent states in the graph-

scheme of the algorithm (GSA) of the control device [6] and their combinations is proposed.

The structure and methods of synthesis of CFSM, which save hardware resources in the implementation of the FPGA and based on methods of replacing input conditions (G-structure) and the presence of pseudoequivalent states (B-structure) and integrated use of methods of replacing input variables and pseudoequivalent states (GB-structure) developed. Conditions of expediency of its use are formulated for each structure.

A number of studies have been conducted for the G- and GB-structures to assess the degree of effectiveness of each structure in the implementation of the CFSM scheme in different families of FPGA chips from common manufacturers Xilinx, Altera (Intel) and Microsemi.

Thus, the application of the method of replacing input variables (G-structure) can reduce the area by an average of 26%, 4% and 14% for chips from Xilinx, Altera and Microsemi, respectively. The integrated use of structural reduction methods (GB-structure) reduces the occupied area relative to the base structure by an average of 33%, 24% and 20% for Xilinx, Altera and Microsemi chips, respectively.

Based on research, it can be argued that the use of a heterogeneous FPGA structure to optimize the CFSM scheme gives the best results for Microsemi chips. The use of structures based on the method of replacing the input conditions and using the presence of pseudo-equivalent states is most effective for Xilinx chips. For Altera (Intel) chips it is proposed to choose a GB-structure, and for Microsemi the best result will be obtained by converting the base structure of the CFSM to G-structure.

The systematization and generalization of the main characteristics of CPLD chips that affect the hardware costs in the implementation of logic circuits CFSM was also carried out. The CPLD structure is a set of functional blocks connected by a programmable switching matrix. For most CPLDs, the function block has a PAL-like structure and is characterized by q programmable circuits "I" having s common inputs. If the number of terms in the expression that is part of the CFSM function system is greater than q, then the implementation of the scheme of this expression will take more than one macrocell.

Based on the analysis of the internal architecture of the CPLD, it was concluded that reducing the number of terms in the functions describing the CFSM leads to a reduction in the required number of macrocells in the implementation of the circuit in the chip.

The use of a pseudo-equivalent state algorithm in the graph scheme allows to reduce the number of terms in the memory excitation functions and the output functions of the Mile automaton. State coding can be performed to reduce the number of terms in the original functions of the Moore automaton. The use of the state coding method with priority in relation to pseudo-equivalence classes makes it possible to reduce the number of direct structure table rows, which, in turn, reduces the number of terms in the memory excitation functions and the original functions of the Mealy automaton [7].

Studies have shown that to reduce the number of terms in the systems of output functions of the Miles machine and memory excitation functions, you can use the method of synthesis of CFSM with coding of sets of output variables, which reduces the number of rows in a direct structural table. In this method, the state encoding is separated from the output set encoding, which allows the state encoding to be performed so as to reduce the number of terms in each of the memory excitation functions and the output functions of the Mile machine, and the encoding of the output signal sets, in turn, to reduce the number of terms in each of the original functions of the Moore automaton.

Based on these methods, four CFSM structures have been proposed for implementation in CPLD chips.

CONCLUSION

As a result of the research, recommendations were formulated for the selection and use of the developed structures and synthesis methods for the element base of various manufacturers.

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