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FPGA Hardware Resources Reduction for Implementation of the Tabular Component of the Information Entropy Estimates Calculation

Iryna Manuliak
ORCID 0000-0002-0072-1532
line 3: *dept. of Computer Systems and Networks*
Ivano-Frankivsk national technical university of oil and gas
Ivano-Frankivsk, Ukraine
manulyak-iryna@ukr.net

Volodymyr Gryga
ORCID 0000-0001-5458-525X
dept. of Computer Engineering and Electronics
Vasyl Stefanyk Precarpathian National University
Ivano-Frankivsk, Ukraine
v.dr_2000@ukr.net

Stepan Melnychuk
ORCID 0000-0002-6973-4235
line 3: *dept. of Computer Systems and Networks*
Ivano-Frankivsk national technical university of oil and gas
Ivano-Frankivsk, Ukraine
stenni@ukr.net

Roman Manuliak
ORCID 0000-0002-6749-6632
Center of Scientific Support of Measurements
SE "IVANO-FRANKIVSKSTANDARTMETROLOGY"
Ivano-Frankivsk, Ukraine
manulyakroman@gmail.com

***Abstract*—The possibility of using linear interpolation in the calculation of intermediate values of information entropy estimates is considered, which practically reduces the amount of data of the computational component of the tabular type.**

Keywords—information entropy, interpolation, digital components.

I. INTRODUCTION

The implementation of specialized computational components of the tabular type is traditionally characterized by high productivity, because the formation of the result is carried out as a choice of the appropriate option from the set of previously calculated results. A significant disadvantage such approach is necessity to store large amounts of data, which leads to unproductive use of FPGA hardware resources. One of the options for solving this problem can be using of interpolation methods, in particular linear, power, etc., to calculate intermediate values as a result of interpolation of two neighbors.

II. OVERVIEW OF EXISTING SOLUTIONS

According to the results of conducted studies in [1], using information about entropy estimates of the amplitudes of pulse signals converted to binary form, which is easy to implement using comparator, allows to ensure efficient allocation of information at lower computational costs compared to other statistical estimates.

In [2], analytical, algorithmic and circuit solutions of digital signal pulse processing devices of primary gas flow converters, represented by successive binary implementations, based on their entropy estimation in information-measuring channels of computer systems are proposed. The implemented approach does not require using of analog-to-digital converters, which simplifies hardware implementation, especially in software development. A digital device (special processor of tabular type) has also been developed, which provides information entropy calculation, which allows to expand the functionality, while maintaining compactness, digital means of processing channel level signals, in particular in the presence of distortions caused by man-made interference.

So, the implementation of the HTable100 block in the AlteraHDL language is shown in Fig. 1 [3].

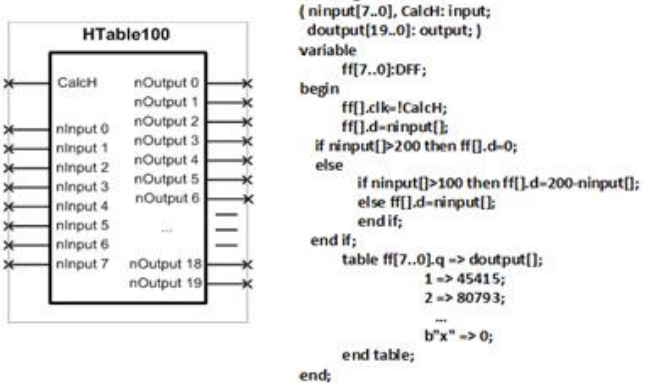

Fig. 1. HTable100 special processor component in Altera AHDL.

The result is formed on the original 20-bit data bus nOutput [19..0], which represents the information entropy, for the corresponding ratio of the probabilities of zero and one value of the signal, in integer form [4].

In fact, the considered digital component is designed for processing data samples, in particular signals, up to 200 elements. So, it is necessary to keep a table of results with 200 calculated estimates of information entropy, which is 800 bytes. Alternatively, linear interpolation of intermediate values can be used to reduce the amount of memory required to 400 bytes.

III. Implementation of the Proposed Approach

In [1] is shown that the choice of the appropriate entropy value is made if it is presence of a logic zero signal on the control line ena of the CntControl unit, which is fed to the CalcH - the permission line to start the calculation of the HTable100 block.

The signal is generated after the value of the reference pulse counter, which actually sets the scan frequency of the signal line, reaches n = 200.

The number of received single pulses from the signal line is fed to the eight-bit data bus nInput [7..0] of the HTable100 unit, is charged by another meter, the operation of which must be coordinated with the reference pulse generator and signal line.

As a simulation result of signals at the respective inputs of the mentioned digital component, it was found that negative and positive error values do not exceed the aperture 10-5 and they are almost symmetrical, which confirms the acceptability of the proposed implementation of such digital component [5].

Characteristics for absolute error of the obtained simulation results of the developed digital component are given in Figure 2.

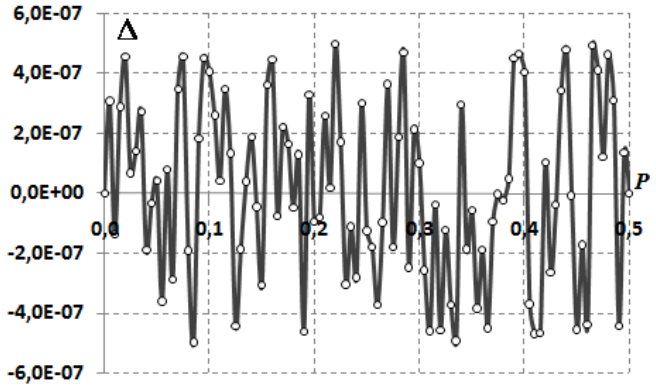

Fig. 2. Absolute error in calculating the information entropy of the developed special processor.

In order to reduce the FPGA hardware resources required to store the information entropy estimation table, it is advisable to consider the possibility of using linear interpolation of intermediate values, which allow to reduce the size of the table by 50%. In this case, the corresponding part of the FPGA resource will be used to perform two arithmetic operations, in particular the operation of unsigned addition and division into two.

It is worth noting that the last operation is easy to replace with a shift operation to the right, which further reduces the computational load.

As a result of simulation signals at the corresponding inputs of the mentioned digital component, it was found that the negative error values do not exceed 10-3 and the positive ones do not exceed 10-5. The result of the absolute error is shown in Figure 3.

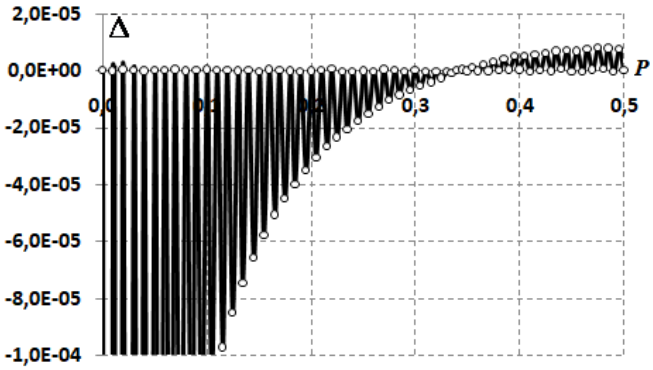

Fig. 3. Absolute error of information entropy calculation for optimized data.

From Figure 3 we can conclude that negative part of the error, the interval [0.0,0.3[, is not acceptable. However, the calculated intermediate values on interval [0.3,0.5] do not actually exceed the errors given in Fig.2.

In this situation, during further conducting research, it is advisable to divide the set of calculated values into separate subsets and use linear interpolation separately for each of the subsets.

Conclusions

Studies have shown that replacing memory resource with a computing resource allows to halve the hardware cost of memory, but requires further research because it does not provide an acceptable error in the calculation of information entropy estimates. The use of arithmetic operations of addition and shift will increase the delay in obtaining the result of such a digital component.

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