

Implementation of the Fibonacci method in AHDL

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Abstract—The paper shows that the method of successive approximation is a variant of Fibonacci sequences. The relation by means of which the sequence of quaternacci numbers can be described is presented. The algorithm of operation of the register of sequential approximation for its further realization on FPGA is offered. The text of the Logic block program describing the 8-bit sequential approximation register in AHDL is presented.

Keywords—AHDL, Fibonacci, FPGA.

I. MAIN PART

The Fibonacci sequence is one of the most famous formulas of mathematics. The Fibonacci sequence is defined as a series of numbers in which each subsequent number is equal to the sum of the previous two [1]. So, for example, if the usual sequence of Fibonacci numbers will look like

0, 1, 1, 2, 3, 5, 8, 13, 21, 34, ...,

then the triple sequence of Fibonacci numbers (tribonacci) will have the form

0, 1, 1, 2, 4, 7, 13, 24, 44, 81

Accordingly, the sequence of quatrains numbers will look like:

0, 1, 1, 2, 4, 8, 16, 30, 58, 112

If we analyze the last sequence of Fibonacci numbers (quaternacci), we can explicitly determine the five numbers that correspond to the set of numbers that can be obtained using the method of sequential approximation. Accordingly, it can be noted that the method of successive approximation is a variety of Fibonacci sequences. The sequence of quaternacci numbers can be described by a recurrent relation [2]:

$$a_{n+1} = a_n + a_{n-1} + a_{n-2} + a_{n-3}, \quad (1)$$

where $a_1 = 1, a_2 = 1$.

Currently, there are chips that work on the method of sequential approximation: 8-bit serial approximation register MC14549B [3]. At the same time, there is a need for registers with smaller or larger bits, not a multiple of 8, and implemented on FPGA.

The inputs of such a register must be provided with data on the iteration number and the need to increase or decrease the output data. The algorithm of the sequential approximation register is presented in Fig.1. Oscillograms of the sequential approximation register are presented in Fig. 2. The simulation was performed in Quartus Prime Lite Edition 18.0. The operation of this algorithm is as follows:

1. The inputs of the sequential approximation register receive data on the ITR iteration number, and the need to add or subtract data D.
2. If a high logic level is set at input D, a certain number will be added to the previous result, the value of which depends on the iteration number.
3. If a low logic level is set at input D, a certain number will be subtracted from the previous result, the value of which depends on the iteration number.

It is possible to implement the method of sequential approximation using the branching algorithm and the selection operator. The text of the Logic block description program of the 8-bit sequential approximation register in AHDL is as follows.

```
IF D==VCC THEN
  CASE ITR[] IS
    WHEN 0 => RG[].D = 128;
    WHEN 1 => RG[].D = (Q[]+64);
    WHEN 2 => RG[].D = (Q[]+32);
    WHEN 3 => RG[].D = (Q[]+16);
    WHEN 4 => RG[].D = (Q[]+8);
    WHEN 5 => RG[].D = (Q[]+4);
    WHEN 6 => RG[].D = (Q[]+2);
    WHEN 7 => RG[].D = (Q[]+1);
  END CASE;
ELSE
  CASE ITR[] IS
    WHEN 0 => RG[].D = 128;
    WHEN 1 => RG[].D = (Q[]-64);
    WHEN 2 => RG[].D = (Q[]-32);
    WHEN 3 => RG[].D = (Q[]-16);
    WHEN 4 => RG[].D = (Q[]-8);
    WHEN 5 => RG[].D = (Q[]-4);
    WHEN 6 => RG[].D = (Q[]-2);
    WHEN 7 => RG[].D = (Q[]-1);
  END CASE;
```

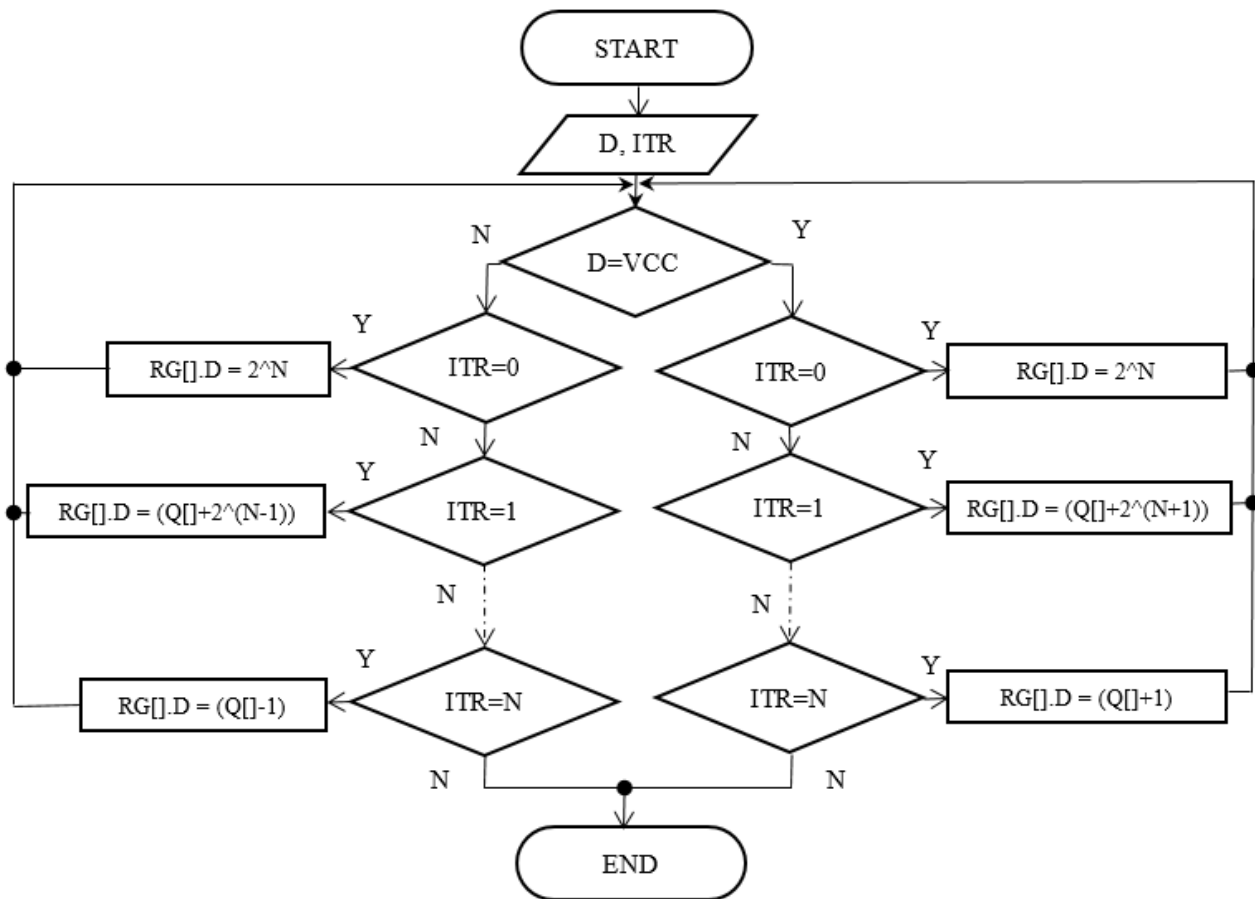


Fig. 1. Algorithm for sequential approximation register operation.

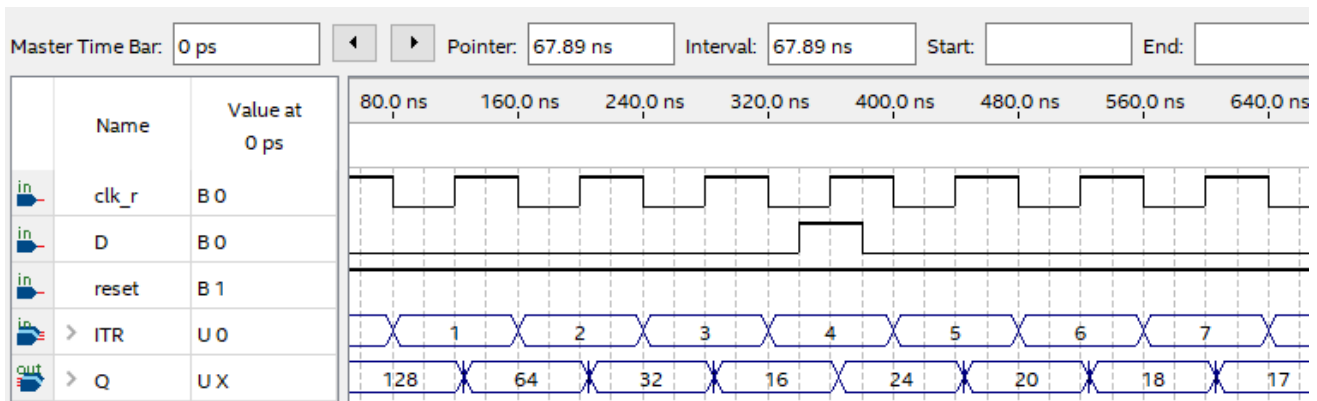


Fig. 2. Oscillograms of the sequential approximation register.

CONCLUSION

From the oscillogram of Fig. 2 shows that as soon as a high-level logic signal appeared at input D, a numerical sequence increased at output Q []. 113 logical elements of FPGA were used to implement the 8-bit sequential approximation register. Similarly, you can implement a register of any bit, which will form any sequence of numbers: Fibonacci, Mersenne and others.

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