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There proceedings depict: mathematical modeling of information signals and systems; hardware description languages; systems of computer aided design of devices on microcontrollers, microprocessors and FPGAs; features of device development on microcontrollers and microprocessors; aspects of the development of devices in the FPGA; architecture and microarchitecture of specialized computing systems; modern trends in the design of microprocessor technology; the problem of improving the quality of training specialists.

Papers are presented in authors' edition.

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Features of the Implementation of an Over/Under Voltage Relay on STM 32 Microcontrollers

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***Abstract*—The purpose of the research is to analyze the effectiveness of the STM32 microcontrollers usage of in the implementation of the load relay protection from mains voltage surges based on the analysis of the root mean square value of the mains voltage and the detection of impulse noise. The research included: development of a projects group for various compilers, microcontrollers and software writing algorithms, as well as performance measurements of all program blocks. As a result of the research, requirements were presented for the value of the microcontroller clock frequency, which is sufficient to detect impulse noise with a duration from 10 µs. An algorithm is also proposed to reduce the requirements for the value of the clock frequency and the amount of RAM.**

Keywords—relay, microcontroller, algorithm, root mean square voltage, performance.

I. INTRODUCTION

For trouble-free operation of electronic devices, strict compliance with the requirements for the operating voltage range and the absence of impulse noise is necessary. Protection is provided by circuit solutions of electronic devices and special protection devices (relays), which turn off the power to electronics when the operating voltage exceeds the upper limit or the voltage drops below the lower limit, as well as when impulse noise is detected [1, 2]. An example of an emergency load shutdown relay is MP-63 DigiTOP. Overvoltage, undervoltage and time delay limits are configurable. The lower limit can be set within 120-200 V. The upper limit is within 210-270 V. The maximum response time to a voltage drop below the lower limit is up to 1s, and above the upper limit is up to 0.06s. It also provides protection by the value of the current in the load. The values of voltage limits, time delays and reaction times in such relays are set by the standards IEC60898-2, IEC 61850, etc [3].

These devices are implemented on hard logic or using microcontrollers [4-7]. If microcontrollers are rarely used in cheap household devices, then they are always used in industrial protection relays. The SIEMENS 3UG4617-1CR20 industrial relay has a built-in Profibus interface for logging network parameters and emergency situations on the server of the automated control system. The usage of microcontrollers makes it easy to reconfigure the protective relay parameters: voltage values, time delays, measurement results averaging time. Protective relays use microcontrollers from various manufacturers TI, Atmel, etc. In recent years, STM32 microcontrollers from ST Microelectronics have been widely used in industry [7, 8]. The STM32 family of microcontrollers contains several popular series that differ significantly in performance, features and price. The purpose of the research was to evaluate the usage effectiveness of the various series of STM32 microcontrollers for the implementation of protective relays as well as the development of optimal algorithms for measuring and processing the results of these measurements in modern environments for compiling program code [9, 10].

II. CALCULATION A ROOT MEAN SQUARE VOLTAGE

A. Methods for calculating the root mean square voltage value

Variable mains voltage is characterized by such parameters as [11-13]: peak value V_p and root mean square value V_{RMS} (fig.1). The main parameter that the protective relays control is the root mean square voltage.

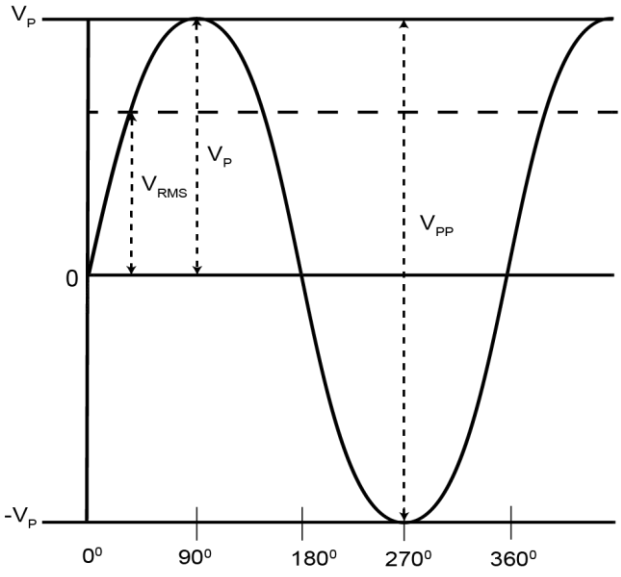

Fig. 1. Frequency response of the synthesized low-pass filter.

A simple formula can be used to calculate V_{RMS}

$$V_{RMS} = \frac{V_p}{\sqrt{2}} = \frac{V_{pp}}{2\sqrt{2}}. \quad (1)$$

When calculating V_{RMS}, it is enough to measure the peak value of the positive half-wave voltage. However, in order to eliminate errors when the negative half-wave disappears, the difference between the peak values of the positive and negative half-waves is used. But this method also gives a significant error when the shape of the sinusoidal voltage is distorted [7, 11]. Such distortions occur when using generators or during the on-off processes of a powerful load. In this case, the formula is applied

$$V_{RMS} = \frac{1}{T}\int U^2(t)dt, \quad (2)$$

where T – is the time multiple of the mains voltage period. When using an analog-to-digital converter to measure the input voltage at a sampling interval, a discrete formula for calculating V_{RMS} is obtained.

$$V_{RMS} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} U_i^2}, \quad (3)$$

where N is the number of measurements for 1 period of mains voltage. Since the mains frequency has a certain instability and may differ from the fixed value of 50/60 Hz, the mains voltage zero selection schemes are used. Having information about the moments when the mains voltage passes through 0, it is possible to accurately determine the number of samples N, which corresponds to 1.2 ... periods of the mains voltage.

Modern protection relays disconnect the load based on the analysis of the effective voltage for 1-10 periods of mains voltage [7, 13]. Some of them can analyze impulse noise and turn off the load when the impulse amplitude exceeds a predetermined value. In such relays, the analysis time is usually 0.1 ms. Based on studies [4] pulse duration can be from 10 μs. From the analysis of the characteristics of existing protection relays and scientific research, it follows that the sampling rate of the analog signal should be from 10 kHz to 100 kHz, which corresponds to the analysis times of 0.1 ms and 10 μs.

With a mains voltage frequency of 50 Hz and a sampling rate of 10 kHz to 100 kHz, one period of the mains voltage will correspond to from 200 to 2000 input voltage samples. The STM32 microcontrollers use a 12-bit analog-to-digital converter and 2 bytes are needed to store one reading, and up to 4 kB to store the conversion results. Even microcontrollers of the cheapest STM32F0 series satisfy this requirement for the amount of RAM. To calculate V_{RMS} according to (3) in one period (20 ms), it is necessary to perform N multiplications and additions, one division and calculation of the square root. It is also necessary to perform N multiplications to convert the code at the output of the ADC to a voltage value. All operations must be performed with floating point numbers. In the STM32 line of microcontrollers, only starting with the rather expensive F4 series, floating-point calculations are implemented at the hardware level.

B. Measurement and calculation algorithm

In STM32 microcontrollers, when converting an analog signal into digital form, the mode of periodic ADC measurements was selected. In this mode, the ADC conversions are started by a timer. Also, interrupts from this timer were used to compare the last measurement result with a threshold value corresponding to the amplitude of the detected impulse noise. When this threshold was exceeded, the load was turned off. To speed up the transfer of measurement results from the ADC to the RAM, a direct memory access controller was used. An interrupt from the DMA controller at the end of the array filling was used to start the V_{RMS} calculation. Since the calculation of V_{RMS} takes a significant amount of time, when the array is cyclically filled with ADC measurement results, the old values are overwritten with new ones. This led to calculation errors. To solve the problem, 2 options were analyzed. In the first case, the elements of the array of measurements were copied to the array by which V_{RMS} is calculated. In the second case, 2 arrays were used. After filling the first array, the operation of the ADC was suspended and the ADC was started with the transfer of the measurement results to the second array. Then the first array was used again. That is, writing to the arrays was performed in turn.

III. RESEARCH RESULTS

For research, 2 identical hardware configurations were created based on cheap STM32F030 and STM32F102 microcontrollers with clock frequencies of 24 and 48 MHz. To compile the developed programs, two popular platforms IAR Embedded Workbench 9.1 and STM32CubeIDE 1.6 were used today. The V_{RMS} calculation was performed in the body of the main calculation loop with the lowest priority. The calculation time for V_{RMS} based on 200 measurements for a period of mains voltage in IAR Embedded Workbench was 8092 cycles without optimization and 7504 cycles with a low level of performance optimization. In STM32CubeIDE these times are 8230 and 7612 respectively. Thus, the calculation time does not exceed 0.4 ms at a clock frequency of 24 MHz and 0.2 ms at a clock frequency of 48 MHz. To detect impulse noise with a duration of 10 μs or more, the sampling period is 10 μs, which corresponds to 240 cycles at a clock frequency of 24 MHz and 480 cycles at a frequency of 48 MHz. During this time, the microcontroller must process the interrupt from the ADC and turn off the load if necessary. According to the results of the study, it takes up to 21 cycles to enter the interrupt handler subroutine. In an interrupt, it is imperative to reset the interrupt flag, since it does not automatically reset itself. This operation requires 22 cycles. Another 32 cycles are needed to compare the last ADC measurement result with the threshold and turn off the load if necessary. Thus, from 15% to 31% of the sampling interval is used for the detection of impulse noise and load control, depending on the clock frequency of the

microcontroller. At the end of the filling of the array of measurements of the mains voltage for the period of this voltage, an interrupt from the DMA controller occurs. If in the handler of this interrupt to copy 200 array elements, then 374 cycles are required. If you restart the ADC and change the array in which the measurement results are stored, then 270 cycles are required.

CONCLUSIONS

STM32 microcontrollers with a clock frequency of 48 MHz or more make it possible to implement a surge protection relay. At this clock frequency, the microcontroller has time to analyze impulse noise with a duration of 10 μs, copy 200 measurement results or restart the ADC when working alternately with two buffers. When using microcontrollers with a clock frequency of 24 MHz, the method of working with two buffers is inefficient, since it takes a fixed number of cycles to restart the ADC. The method of copying an array of values is more efficient, since the size of the buffer can be reduced to 100 dimensions. This will cut the copying time in half. Disconnecting the load when the V_{RMS} threshold is exceeded is a lesser priority. The V_{RMS} calculation time is no more than 2.5% of the mains voltage period and fully complies with the requirements for this parameter for such devices. The best performance when compiling a program is provided by the IAR Embedded Workbench compiler. Thus, even on the simplest STM32F0 microcontrollers, it is possible to implement a load protection relay, which ensures the economic competitiveness of such devices.

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Large Integrated Circuit of a Linear Interpolator Based On a Basic Matrix Crystal

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***Abstract*—Peculiarities of construction of a large integrated circuit for a linear interpolator based on a basic matrix crystal are considered.**

Keywords—graphic primitives, linear interpolator, large integrated circuit, Basic Matrix Crystal.

I. INTRODUCTION

Line segments have the greatest weight in the set of graphical primitives. In this regard, the algorithms of linear interpolation are paid special attention in the development of graphics devices [1-8]. Vector generators (linear interpolators) are widely used in computer graphics tools and numerically controlled machines.

The authors developed and manufactured a large integrated circuit (LIC) of a linear interpolator (Fig.1) using a basic matrix crystal (BMC) 1515XM. The integrated circuit has been introduced into serial production in a number of devices.

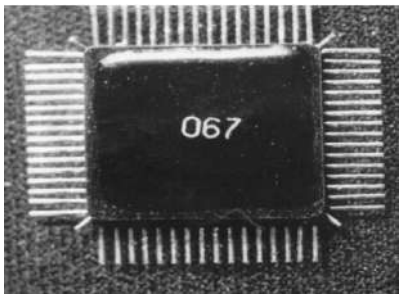

Fig. 1. Appearance of a LIC of a linear interpolator.

The main advantages of BMC: has a fixed geometric structure, which greatly simplifies the automatic placement and tracing of elements; developing LIC using BMC is performed with a small number of photo templates, which significantly reduces the cost of production of LIC; developed library of logical elements and standard circuit solutions significantly simplifies the process of developing a logical project, reduces design time; LICs based on BMC do not require qualification tests.

II. DESCRIPTION OF THE LIC OF A LINEAR INTERPOLATOR

The LIC of the interpolator, which is implemented using the BMC 1515XM1, provides the following functionalities: formation of step increments of the coordinates of the line segment given by the coordinate increments; receiving of the initial coordinate of the line segment and formation of unit increments of the coordinates of the line segment, given by the coordinates of the end point; receiving and shifting the mask code with its issuance in the sequential code; equalization of the speed of segment formation depending on the slope of the line; control of issuance frequency of single increments of coordinates; receiving coordinates (increments) in different formats; receiving coordinates (increments) in direct or inverse codes; controlled suspension of line segment generation.

The developed linear interpolator is characterized by the following main parameters: power supply voltage - 4.5… 5.5 V; information retention time at information inputs relative to strobe signals - 100 ns; the minimum period of input sync pulses is 200 ns; bit rate - 12 binary digits; maximum current consumption in static mode - 1 mA.

Consider the algorithm and block diagram (Fig. 2), which was implemented in the LIC.

In the vast majority of cases, the method of estimating function [1, 8] is used to form straight line segments, the sign of which determines the position of the trajectory point relative to the straight line segment. The most common use of the method of estimating function for the formation of vectors is also due to the simplicity of the computational process, as well as the lack of "long" operations. The method provides maximum accuracy and uses as a basic microoperation of acumulative addition. The most common algorithms of the estimating function are the algorithms of Brezenham and Pietukh-Obidnyk [1, 2]. The algorithm of Pietukh-Obidnyk is the best because it provides a simpler calculation of the initial value of the estimation function and lower bit rate of the operating unit.

The formation of a segment of a straight line using algorithm of Pietukh-Obidnyk [1, 2] is conducted according to the formulas:

$$F_{i+1} = \begin{cases} F_i - SI, \; if \;\; F_i \geq 0, \\ F_i + \Delta, \; if \;\; F_i < 0, \end{cases}$$

where $F_0 = \lfloor LI/2 \rfloor$, $\Delta = LI - SI$, LI is the larger coordinate increment of the segment, SI is the smaller coordinate increment of the segment.

If $F_i \geq 0$, then the step on the main coordinate is performed. When $F_i < 0$, a combined step is performed (in both coordinates). This algorithm provides maximum accuracy (maximum error is equal to half the sampling step).

The block diagram of the operating part of the linear interpolator is shown in Fig. 2.

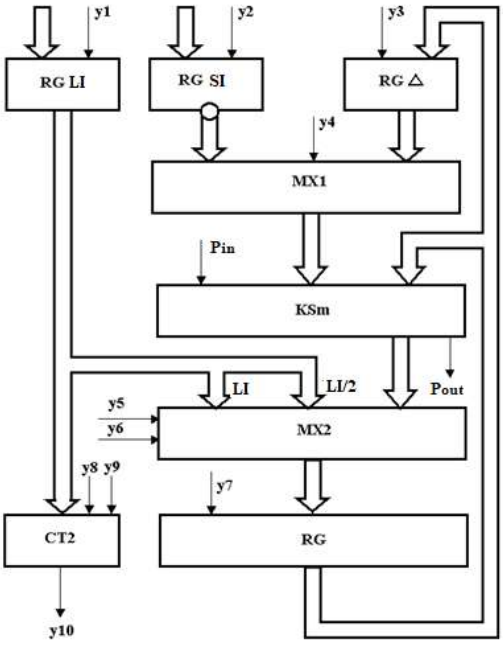

Fig. 2. Block diagram of the operating part of the linear interpolator.

The device includes registers RG for storing LI, SI and Δ, acumulative adder, which consists of a combination adder KSm and register RG , multiplexers MX , counter $CT2$. Larger (LI) and smaller (SI) increments are entered in the registes $RG\,LI$ and $RG\,SI$ from the input data bus D , respectively.

The value of LI via the multiplexer $MX2$ is entered in the RG of the acumulative adder (formed by the combination adder KSm and the register RG). Through the multiplexer $MX1$ the value of SI in the inverse code is fed to the input of the acumulative adder (since the subtraction operation for this case is performed in the supplementary code, the level of the logical unit is fed to the input of the acumulative adder), i.e. the data is read from the inverse outputs of the triggers that form the specified register. The value of $LI - SI$ from the output of the adder KSm is entered in the register $RG\,\Delta$. The value of the larger increment is fed to the counter $CT2$ from the output of the register $RG\,SI$, which is recorded in the counter under the action of the signal $y8$.

The value $\lfloor LI/2 \rfloor$ is fed to the RG register of the acumulative adder, which is obtained by assembing at the output of the multiplexer $MX2$. This completes the preparation cycle.

In the interpolation cycle the value of the estimating function is calculated in each tact. To do this, value Δ or SI is fed from the output of the multiplexer to the input of the acumulative adder.

The sign of the estimating function determines the transfer signal P_{out} of the adder. With each interpolation tact, the value of the counter decreases by 1. When the counter reaches zero, the interpolation process ends.

CONCLUSION

The developed LIC of the linear interpolator provides the maximum possible accuracy of reproduction of segments of lines in discrete coordinate space and formation of step increments in each tact.

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Miniaturization of Control Devices on Programmable Logic Chips

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***Abstract*—The paper is devoted to solving the topical scientific problem of developing the structures and methods for synthesis of the combined finite state machines (CFSM), aimed at reducing equipment costs when implementing the CFSM logical scheme in the basis of programmable logic integrated circuits such as FPGA and CPLD.**

Keywords—combined FSM, FPGA, CPLD, logic circuit, embedded memory, pseudo-equivalent states.

I. INTRODUCTION

In the modern process of designing digital systems on the basis of programmable logic chips (PLC), automated design systems are widely used. At automatic allocation scheme implemented on PLCs, different algorithms of Boolean functions decomposition, which, studies show, do not provide optimal resource utilization chip, which explains the urgency of optimization problems in the implementation of Boolean functions in the PLC structure. The result of this optimization is not only possible reduction of cost and reduction the size of the circuit, but also power consumption and power dissipation minimization, reducing the time of signal propagation, which generally increases the efficiency of the designed circuit.

II. ANALYSIS OF LITERATURE

An overview and analysis of the methods and models of control devices (CD) representation in modern digital systems have been performed. On the basis of the analysis, the systematization of the resulting structures has been carried out and the direction of research has been allocated. According to the direction of research, structures and techniques of synthesis of CFSM that already exist and which are oriented to implementation in the basis of programmable logic are considered.

An overview of the element base and the analysis of the architectural features of FPGA and CPLD programmable logic chips of such well-known manufacturers as Xilinx, Altera (Intel) and Microsemi has been conducted. The technical characteristics of microcircuits are distinguished, due to which it is possible to reduce the hardware costs in the logical circuits of CFSM. A comparison of the characteristics of modern series of FPGA and CPLD chips has been performed.

In the paper, the classification of methods for optimizing the costs of equipment in the implementation of CD in the form of a machine with "hard" logic on programmable logic circuits such as CPLD and FPGA has been considered. Based on the analysis of these methods, it has been concluded that it is expedient to use structural reduction methods for optimizing the CFSM circuits on the basis of the use of hardware resources.

III. METHODS AND RESEARCH RESULTS

You can use such a feature of the FPGA as a heterogeneous structure in the design of the CFSM scheme. This means that three FPGA components can be used to implement the scheme: UT LUT (Look Up Table) elements, Embedded Memory Block (EMB) and programmable interconnects [1 - 4].

We analyzed the ways and models of representation of control devices in modern digital systems. The systematization of control device structures is carried out and the approach of realization of a part of signals of the control device on EMB on the basis of the analysis is offered.

According to the results of the research, it can be noted that the largest reduction in allocated resources is observed for Microsemi chips, the least - for Altera (Intel) chips. The application of the developed structure is most expedient if the number of Moore output signals exceeds the number of Miles output signals [5].

The necessity to implement complex functions (functions of many variables) in the basis of programmable logic circuits, which has design limitations on the number of inputs / terms / outputs, causes the problem of decomposition. To solve it, the use of such methods of structural reduction as the method of replacing logical conditions, the use of pseudo-equivalent states in the graph-

scheme of the algorithm (GSA) of the control device [6] and their combinations is proposed.

The structure and methods of synthesis of CFSM, which save hardware resources in the implementation of the FPGA and based on methods of replacing input conditions (G-structure) and the presence of pseudoequivalent states (B-structure) and integrated use of methods of replacing input variables and pseudoequivalent states (GB-structure) developed. Conditions of expediency of its use are formulated for each structure.

A number of studies have been conducted for the G- and GB-structures to assess the degree of effectiveness of each structure in the implementation of the CFSM scheme in different families of FPGA chips from common manufacturers Xilinx, Altera (Intel) and Microsemi.

Thus, the application of the method of replacing input variables (G-structure) can reduce the area by an average of 26%, 4% and 14% for chips from Xilinx, Altera and Microsemi, respectively. The integrated use of structural reduction methods (GB-structure) reduces the occupied area relative to the base structure by an average of 33%, 24% and 20% for Xilinx, Altera and Microsemi chips, respectively.

Based on research, it can be argued that the use of a heterogeneous FPGA structure to optimize the CFSM scheme gives the best results for Microsemi chips. The use of structures based on the method of replacing the input conditions and using the presence of pseudo-equivalent states is most effective for Xilinx chips. For Altera (Intel) chips it is proposed to choose a GB-structure, and for Microsemi the best result will be obtained by converting the base structure of the CFSM to G-structure.

The systematization and generalization of the main characteristics of CPLD chips that affect the hardware costs in the implementation of logic circuits CFSM was also carried out. The CPLD structure is a set of functional blocks connected by a programmable switching matrix. For most CPLDs, the function block has a PAL-like structure and is characterized by q programmable circuits "I" having s common inputs. If the number of terms in the expression that is part of the CFSM function system is greater than q, then the implementation of the scheme of this expression will take more than one macrocell.

Based on the analysis of the internal architecture of the CPLD, it was concluded that reducing the number of terms in the functions describing the CFSM leads to a reduction in the required number of macrocells in the implementation of the circuit in the chip.

The use of a pseudo-equivalent state algorithm in the graph scheme allows to reduce the number of terms in the memory excitation functions and the output functions of the Mile automaton. State coding can be performed to reduce the number of terms in the original functions of the Moore automaton. The use of the state coding method with priority in relation to pseudo-equivalence classes makes it possible to reduce the number of direct structure table rows, which, in turn, reduces the number of terms in the memory excitation functions and the original functions of the Mealy automaton [7].

Studies have shown that to reduce the number of terms in the systems of output functions of the Miles machine and memory excitation functions, you can use the method of synthesis of CFSM with coding of sets of output variables, which reduces the number of rows in a direct structural table. In this method, the state encoding is separated from the output set encoding, which allows the state encoding to be performed so as to reduce the number of terms in each of the memory excitation functions and the output functions of the Mile machine, and the encoding of the output signal sets, in turn, to reduce the number of terms in each of the original functions of the Moore automaton.

Based on these methods, four CFSM structures have been proposed for implementation in CPLD chips.

CONCLUSION

As a result of the research, recommendations were formulated for the selection and use of the developed structures and synthesis methods for the element base of various manufacturers.

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Subject-Information Environment Deployment of Heat Press Operation Hardware Emulation

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***Abstract*—The architectural diagram and deployment stages the laboratory learning bench of heat press operation hardware emulation as a component of production line in operational printing are given. The analytical apparatus of project on Arduino Uno computing platform basis receives the parameters of printing order and determine the control signal for actuators, mimicing of system general behavior.**

Keywords—laboratory bench, computing platform, learning experiment environment, operative printing, JDF, Industry 4.0.

I. INTRODUCTION

Training of engineering profile personnel is focused on professional skills formation with permanent use of topical industry content. The applying of technological resources of branch enterprise has a positive effect on the development of necessary critical competencies of engineering students. The introduction of the practice of organizing learning experiments as close as possible to the production conditions plays a key role in the apprehension of engineering-oriented disciplines and the amplification of sustainable professional acquirements.

Gaining experience in working with subject area equipment and regular experimental consolidation of acquired theoretical knowledge improve the competitiveness of graduates in market conditions and guarantee the productivity of placemented engineers. Appropriateness the requirements of modern production environment contribute to furtherance of successful professional career.

The transition to remote learning mode, caused first by coronavirus pandemic and widespread leading in quarantine restrictions, and later by the open full-scale russian invasion and the mass appearance needy for academic refuge, led to the search to alternative pedagogical solutions in the educational process. Computer-mediated learning provides advanced technological toolkit for acquiring knowledge and competencies in asynchronous environment using mobile and stationary devices.

Previous experience the institutions of higher engineering education in information technology use and cognitive flexibility development was formed in determining strategies improve the effectiveness qualified professionals training, including sustainability trends in automation and exchange of target data of production situations. Therefore, the implementation of the principles of Industrie 4.0 in the educational process of teaching engineers is inextricably rearrangement with goaled restructuring of academic courses in the direction focused on modern information and communication technologies. Consequently, it is important to study the ways of deploying computerized media platforms of learning experiment, which on production data analytics basis are able to emulate typical processes behavior by profile industry.

II. PROBLEMATICS IN DEPLOYMENT OF CYBER PHYSICAL SYSTEMS FOR EXPERIMENTAL RESEARCHES

According to Fourth Industrial Revolution's leading strategy for cyber-physical systems (CPS), computerized full-scale and analytical components work closely together, representing a virtually perfect network combination. At the same time, means provided by the CPS allow to combine research efforts related to the subject areas of different engineering disciplines. High functionality and adaptability of such systems provides increased efficiency in the comprehensive appliance of information technology.

A. Expanding the application areas of industrial data

Integration of disparate cyber-physical modules into a unified hardware and software complex guarantees the expansion of computing resources through third-party servers, expert agents, knowledge bases, cloud storage and more. However, for a long time, the spread of the CPS concept has been hampered by insufficient activity in the introduction of corporate channels between branch enterprises and higher engineering education institutions. Meanwhile, unexpected synergistic effects can be achieved by analyzing the indication of industrial sensors in generating scenarios for academic laboratory cyber-physical systems.

The productive technique of fault prediction [1], which provides input data for forecast maintenance of industrial equipment, will also increase the influence of pedagogical models in the formation of professional skills of applicants of higher engineering degree. In general, by accelerating production processes, a large amount of industrial data can also be used in an alternative way. For example, such multiple-choiced targeted application of enterprise resources is proposed to be used in the deployment of virtual learning experiment environments. As organic instrumental means of the academic space, they are suitable for studying the features of branch machines fleet configuration and the situational solution of number typical production problems [2].

B. *Categorization of learning experiment environments*

Within the engineering specialties context, one of main way of the subject area cognition is the ability to operate with the research means of typical for the industry transitional processes. In nowadays realities of remote learning, *infocommunicative environments* have become especially widespread in the organization of distance engineering education, offering toolkit of virtual space with adequate implementation of simulation fragments and surrogate models of the subject area [3]. Although in general the given decision saved the practical component of educational process and provided an understanding the learning experiment based stages, but acquisition of skills in working with professional equipment here focuses only on interaction with a computer manipulator. Being physically absent from the higher education institution campus, the student cannot directly operate with the material components of the laboratory bench, measuring devices, hardware base of the model-object, etc. Thus, due to the lack of classroom *natural-spatial environment* of experimental research, the practical and cognitive activity of the applicant is generally deprived of the possibility of enlargement [4].

A certain compromise in this state of affairs is the *subject-information environment* of the learning experiment, which includes cyber-physical systems with a constructive interface for telemetry inconnecting. One of the means of implementing such solution is passive monitoring of remote mechanisms via webcams and obtaining individual experimental results in the form of graphs, tabular data and the like [5]. The obvious disadvantage the following remote laboratory organization is the need for costly industrial equipment that not all engineering institution can afford. Also, the lack of feedback has nihilistic consequences, giving the student only the role of an observer. The presence of a campus operator-instructor [6] does not particularly save the situation, although it can bring the negative impact of the human factor.

Thus, there is a need to deploy an automated *subject-information environment* of a remote laboratory, which would not require constantly present service personnel and provide emulation of industrial equipment based on information the parameters of the job task and about the current course of the technological process in real time. The effectiveness of such a cyber-physical media platform of the learning experiment is determined primarily by the adequacy of the conceptual model of the subject area. Therefore, when implementing remote laboratory workshops, special attention should be paid to the formalization of the structural components of the platform and relationships between them.

III. Design Stages the Laboratory Bench for Emulation of Heat Press Operation

The presented research shows the stages of designing the cyber-physical environment of the learning experiment for the study of technological processes of operational printing, in particular the hardware emulation of the automated control system of the heat press when performing a printing order. Modern heat presses are used for personalized decor of clothing, utensils, stationery, textiles, trinkets, etc. under the action of pressure and elevated temperature for a clearly defined time.

A. *Determining the architecture of laboratory learning bench*

To clarify the components of cyber-physical system for hardware emulation of the head press and explain the sequence of its design, an architectural diagram of the media platform for remote support of laboratory workshops was built (Fig. 1). As a result, the hierarchy of modules was formalized, the features of their interaction were determined to implement the coordinated functioning of integrated environment for studying the heat press operation.

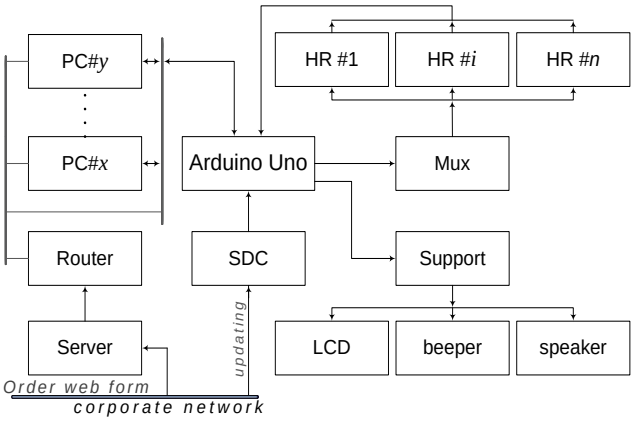

Fig. 1. Architecture diagram of heat press environment emulation

It was decided to choose the Arduino Uno computing platform [7] as the analytical apparatus of the designed cyber-physical system, respectively, the conceptual models of the conditioned expansion boards [8] are located as building on. The circulation of data in the environment of our remote laboratory begins with the receipt of a package of job tasks through network devices for information transmission.

Another module of the system is the memory card drive (SDC), which is implemented on the controller board and stores the corporate database with the parameters of raw materials and consumables. The content of the database is synchronized through the corporate network using the extended end-to-end production format xJDF [2].

For the supporting visualization of the transition processes of the printing order, the project provides a liquid crystal display. Audio support of production stages or emergency situations is provided by a speaker (headsets) with Bluetooth data acquisition A separate primitive alert can also be provided by a piezoelectric beeper integrated into the controller periphery (Fig. 2).

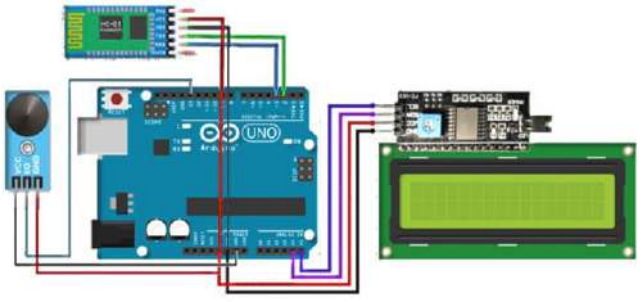

Fig. 2. Connecting peripherals for accompanying notification

To connect the models of actuators of industrial equipment in the control system introduced a multiplexer [9] located on the architectural diagram in the control area (Fig. 3). Models of actuators are implemented on hardware registers (HR), which emulate the temperature setters of heat presses. A folding device is also made on one of the registers that simulates a heat press group with a flat-panel heating element.

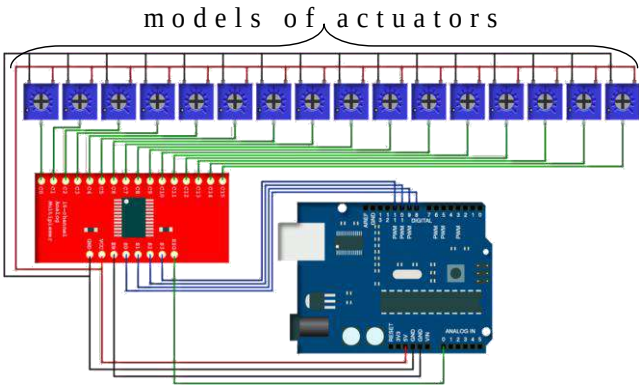

Fig. 3. Implementation of a multiplexer on CD74HC4067 shield

The procedure of fulfilling a printing order begins with combining the characteristics of raw materials obtained from the order web form. These characteristics determine the course of further technological process. After receiving information about the features of intermediate product for order, the analytical apparatus in the calculation area initiates a query to the database.

As a result of processing the industrial content of database, the cyber-physical system receives the parameters of terminal actuators. Such parameters in the presented project include the temperature and time required for manufacture of quality products, as well as the ID of the target heat press, which covers a group of relevant registers (Fig. 4).

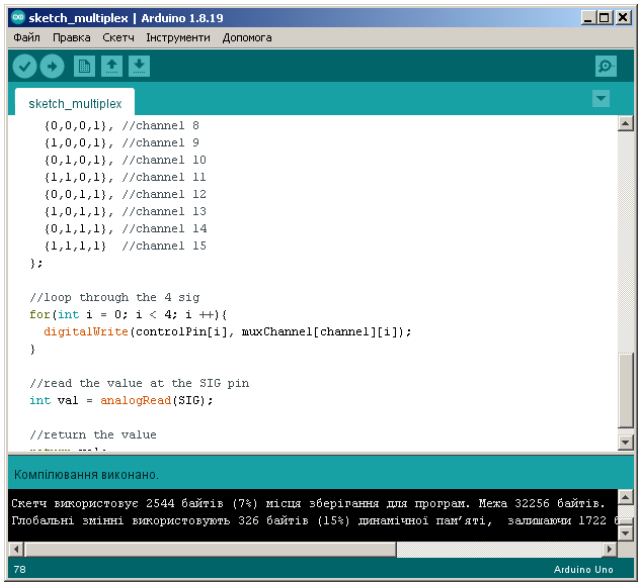

Fig. 4. Fragment of sketch for actuator initiation

The end user terminal in the presented project is a personal computer. An ordinary desktop, laptop, tablet, etc. can serve as such a device. The corporate network through the academic server delivers to end terminal information with the characteristics of registered printing order, obtained through the client web form of the operational printing institution.

The applicant as a user of the laboratory bench can view, analyze and clarify this information. It can also identify further work scenarios for the cyber-physical platform. As a result of such intervention of an incompetent operator, there may be discrepancies due to inconsistencies in the parameters of the transition process. Such discrepancies can be observed in the information regions of the display of the end terminal and the LCD supporting visualization module. The student must draw his own conclusions from the abnormal situation [3].

B. Accompanying information on the production stage of thermal-transfer process

To further attract the student's attention when performing laboratory exercises to study the work of the heat press, a list of reasons for the accompanying notification within the designed system was organized (Table 1).

TABLE I. PRODUCTIONS SITUATIONS OF ACCOMPANYING NOTIFICATION

Event	Information	Bipper duration
Order	Receipt of the order	Delay(200)
Warming	Start heating the element	Delay(200)
Readiness	The heat press is ready to work	Delay(200)
Beginning	The timer started	Delay(200)
Completion	The heat press has finished its work	Delay(200)
Error#255	Heating element error	Delay(30)×3
Error#E0	Low temperature	Delay(1800)
Error#E1	Sensor error	Delay(40)×4
Error#E02	Failure of the temperature control unit	Delay(30)×1
Error#E03	Control unit failure	Delay(30)×2
Error#E19	Sensor short circuit	Delay(100)×3
Error#E20	Breakdown of the sensor	Delay(100)×2
Error##P01	Breakdown of the folding mechanism	Delay(100)

A series of information on production errors attracts special attention here. The fact is that when building electronic devices, the producer hopes for quality and smooth operation of its components, providing "protection from fools" and maximizing the human factor removing. But electronics also has the property of making mistakes, breaking, certain components may fail, which can interfere with the smooth operation of the entire system.

However, electronics have an advantage – each of the errors can be predicted in advance, and therefore the producer sews in the SPD of the device instructions for notification of the occurrence of a fault to eliminate it in time [1]. The error base is based primarily on the intended purpose of the end device. Secondly, such databases are turn out on the actual common errors of electronic devices, which is also important to ensure good system performance. Electronics errors can occur anywhere, regardless of device purpose. Such errors can be the failure of main components of electronic part of the system, coding problems, program errors, and wear of parts. Therefore, before talking about specific errors of a particular device, it should first review the general errors when working with electronic devices.

As mentioned earlier, such errors are usually fragments of the electronic part, connecting wires, etc., which have failed. Also here can be contribute programming errors. Error codes are designed to report a specific problem and are abbreviated to save volume and speed up transmission. The analytical device converts the received code into the inscription clear to the operator for which it is also possible to generate audio messages or simply to reproduce by a beeper sequence. In some cases, the analytical apparatus itself can determine a set of measures to correct the error identified by the received code. In this case, depending on the mode of the laboratory workshop, the student is asked to choose the option of troubleshooting.

Thereby, the given list of production situations (Table 1) is quite suitable for operative computing and dynamic administration of the active subject-information environment of the emulation of the heat press. The main scenario of the workshops is implemented on the basis of requests and subsequent decision-making, when the student independently builds a strategy for researching the subject area using the available toolkit of the laboratory bench, while developing skills to predict the adequacy of the expected result.

CONCLUSIONS

In this research the technique of deploying the components of the academic cyber-physical system as a "device shadow" was tested on the basis of information about the parameters of the job task and the current state of industrial equipment from the production line in real time. The proposed corporate channel based on the end-to-end JDF production format within the IIOT concept coordinates the efforts of local nodes of the profile learning experiment environment throughout the value chain of the printing order, emulating missing resources beyond the subject area.

Further development of the project will be to formalize the mechanism of virtual laboratory scenarios, clarification of the means of accompanying visualization, in particular the selection of information regions of the end terminal, and sample of optimal protocols for forecasting, self-tuning and adaptation in the interaction of disparate professionally oriented cyber-physical systems and industrial strategic planning processes.

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Designing the ACS of Cutter Winding Section

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***Abstract*—Functional diagram of automatic control of rolled material winding with realization of target winding modes on various tension phases according to production needs is constructed. Based on the ATmega328P microcontroller, the automatic control system (ACS) was designed that provided reliable and trouble-free work of winding section of roll material on SummaCut D120R wide-format cutting machine for acceleration of production line in operational printing.**

Keywords—automatic control system, technological process, large-format cutting machine, winding mechanism.

I. INTRODUCTION

The rapid development of printing market has contributed to formation of large number different types of advertising products, and this in turn led to emergence of new printing-oriented technologies, which aimed to accelerate the execution of individual orders of varying complexity. In addition to wide-format printers, auxiliary equipment is also actively used in operational printing institutions, in particular for post-printing processing of printing orders. Among such machines, cutting plotters stand out favorably as devices for clipping any stencils or images from different materials, under which cutter knife is adapted: billboards, shop windows decor, signs, as well as pattern from heat-transfer film on various surfaces from clothes to consumer goods [1].

It should be noted that most productive work the operational printing institution is possible only with a carefully selected of equipment skeleton, taking into account all factors, including its maintenance. However, branded solutions use in machines fleet is not always possible in conditions of small printing, because not all devices are able to work with maximum efficiency on a flexible technological routing order map. This state of affairs, in turn, pushes such institutions to find and implement their own solutions for optimizing key components of machines fleet [2].

Due to the increased requirements for the timing of production and quality of advertising manufactures by the customer and the specifics of small business in limiting financial costs there is a need to improve the efficiency of existing production resources. This, in turn, encourages institutions to improve the components of printing equipment or to develop original new ones that can significantly improve the devices performance. Which will obviously allow a small business to reduce the number of shortages and the cost of the finished product and increase safety at work [3]. Therefore, the need to design new and optimize existing automated control systems integrated into production lines is seasonable and relevant.

II. DETERMINING THE OPTIMIZATION DIRECTIONS OF CUTTING PLOTTER

Wide-format plotter cutting is the basis for creating a variety of polygraphically orders [4]. It is due to the introduction of wide-format cutting in the list of services of the institution that a number of bold atypical ideas become realistic, which distinguishes an extraordinary goods between the current standards and the use of ordinary products. Cutter hew out provides a virtually limitless range of options that make advertising more multifaceted and unique.

Plotter hew out in the printing industry involves a whole complex of tasks to create a finished product using special wide-format cutters. The process of plotter hew out (actually, cutting) is to cut the raw material along the contour so that the blade cut nick the vinyl layer of the film only, while the base of the product remained intact. Making a printing order on a plotter consists of a number of stages. First of all, the machine operator lays the necessary material, orienting relative to the guide line on the desktop to maintain maximum symmetry.

This is done to reduce the likelihood of mowing the material during cutting. Next, selected the desired layout in a graphics editor suitable for integration into service software built into equipment by the manufacturer company. Finally, using the functionality of the cutting device, the operator uses the test to determine the depth of slit at which the plotter will cut the film and the adhesive layer, and will not damage the base (substrate).

Despite the versatility and other significant advantages of SummaCut D120R wide-format cutting plotter researched in project, during the execution of the printing order against background of design features at high loads revealed a number of significant shortcomings that directly damage for main units and elements and do not allow to qualitatively organize the production process, and sometimes cause failure of key components. In turn, this leads to an increase in production time, obtaining a higher percentage of substandard goods - and as a result of excessive costs due to unprofitability.

Given the pricing policy of spare parts manufacturers and attendant details, it will not be advisable for a start-up company to replace spare item often enough, as this will lead to unprofitable use of equipment. The solution to such problems and ways to correct the identified shortcomings in the operation of printing equipment is exactly targeted optimization or construction of original key components in accordance with the principles of economic activity of small businesses with a limited number of jobs [5].

III. Expansion of Winding Modes for Rolled Material

Almost everything that produces a wide-format cutting plotter is wound with the representation on the outside, because it does not allow the carved order to peel off from the base [1]. This prevents the deformation of the self-adhesive goods and the ingress of dust particles into its mucilage layer, to wit avoids the creation of defective products. However, study of technological processes at cutting stage revealed a number of exceptions, which include in particular the thermal transfer film. Due to its structure, such a film is able to stretch in the winding process the representation outwards, which is why there is a need to wind the dissected side into a roll. The novel introduced reverse mode will also allow to quickly unwinding the material from tube [5] without having to remove it from winding mechanism and ensure the adjustment of system by matching the winding parameters with the dissecting speed of the wide-format cutting plotter for ensuring the stability of the deployed production line.

The calculation of the rated power of the DC motor (DCM) of the winding section [4] is carried out relative to the specified mass of the filled tube m=25 *kg*:

$$P=M\times V/\mu_m=218\ W, \qquad (1)$$

where the nominal weight of the cargo
$M=m\times g$=25×9,81=245,24 *N*;
energy conversion efficiency of winding mechanism μ_m=0,9;
cargo rotation speed V=0,8 *rps.*

According to the obtained characteristics, DCM MY1016 with power P=250*W*, voltage U=24*V* and rated current I_n=13,7*A* was selected. To further simplify the scheme and increase the energy conversion efficiency of finished mechanism, it was decided to use the pulse-width modulation (PWM) method to control the DCM [7]: by changing the filling factor of the PWM regulates the average voltage on motor, namely speed. To set the speed used potentiometer.

Since the direction of rotation DC-motor shaft depends on the polarity, to regulate it, it was decided to use an advanced electronic circuit "H-Bridge" with a conjunctive control unit (Fig. 1: A, B, C, D), which makes it impossible to close two keys in one branch and prevents short circuits.

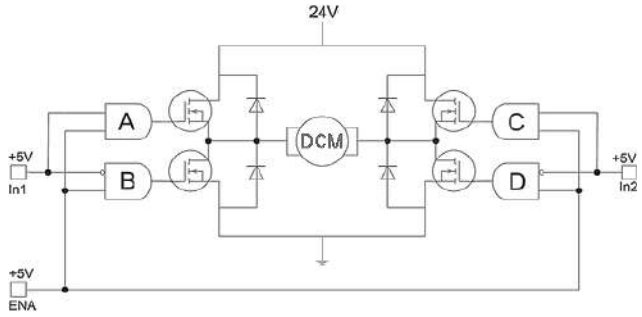

Fig. 1. Functional diagram of material winding modes control

In this way, the presented engineering solution allowed to achieve full control of the DCM: the direction of rotation will be responsible for advanced H-Bridge, and speed regulation will be carried out through the receipt of PWM signals from the controller-regulator [6]. To create a more compact design of the winding section, it was decided to use DC 3-36V 15A motor driver, which supports a combination of previously introduced control methods.

IV. Implementation of Analytical Apparatus the Winding Section

A number of additional components have been used to ensure performance of designed control system for direction and rotation speed of DC motor based on Arduino computing platform [7]. Thus, in addition to DCM with a nominal voltage of 24 V and Arduino UNO control module, DC 3-36V 15 A driver and 100 kΩ potentiometer, two DC sources with voltages of 5 *V* and 24 *V* were used as power.

The potentiometer is powered directly from the control board and, depending on its value, thanks to the analog connector A0, the Arduino module is able to receive an analog signal (Fig. 2). By converting such a signal into digital, the control board with the help of developed software flexibly implements DCM rotation speed control using PWM signal. The main control commands are directed from connectors 10 and 11 (on Arduino) to PWM 2 and DIR 2 pins (in DC 3-36V 15A motor driver).

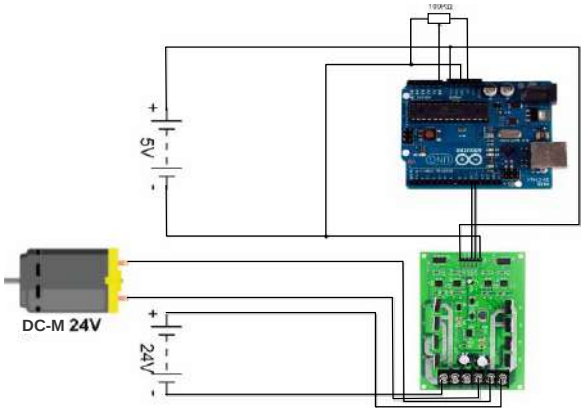

Fig. 2. Assembly diagram of analytical apparatus the winding section

Conclusion

Thus, implemented software in combination with builded analytical apparatus provides reliable and trouble-free operation of designed rolled material winding section by different sides in accordance with the production needs of small enterprises and with introduction of extended speed control modes to accelerate of production line in operational printing.

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FPGA Hardware Resources Reduction for Implementation of the Tabular Component of the Information Entropy Estimates Calculation

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***Abstract*—The possibility of using linear interpolation in the calculation of intermediate values of information entropy estimates is considered, which practically reduces the amount of data of the computational component of the tabular type.**

Keywords—information entropy, interpolation, digital components.

I. Introduction

The implementation of specialized computational components of the tabular type is traditionally characterized by high productivity, because the formation of the result is carried out as a choice of the appropriate option from the set of previously calculated results. A significant disadvantage such approach is necessity to store large amounts of data, which leads to unproductive use of FPGA hardware resources. One of the options for solving this problem can be using of interpolation methods, in particular linear, power, etc., to calculate intermediate values as a result of interpolation of two neighbors.

II. Overview of Existing Solutions

According to the results of conducted studies in [1], using information about entropy estimates of the amplitudes of pulse signals converted to binary form, which is easy to implement using comparator, allows to ensure efficient allocation of information at lower computational costs compared to other statistical estimates.

In [2], analytical, algorithmic and circuit solutions of digital signal pulse processing devices of primary gas flow converters, represented by successive binary implementations, based on their entropy estimation in information-measuring channels of computer systems are proposed. The implemented approach does not require using of analog-to-digital converters, which simplifies hardware implementation, especially in software development. A digital device (special processor of tabular type) has also been developed, which provides information entropy calculation, which allows to expand the functionality, while maintaining compactness, digital means of processing channel level signals, in particular in the presence of distortions caused by man-made interference.

So, the implementation of the HTable100 block in the AlteraHDL language is shown in Fig. 1 [3].

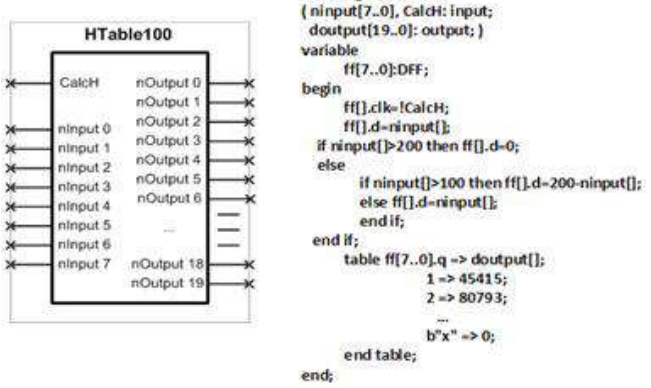

Fig. 1. HTable100 special processor component in Altera AHDL.

The result is formed on the original 20-bit data bus nOutput [19..0], which represents the information entropy, for the corresponding ratio of the probabilities of zero and one value of the signal, in integer form [4].

In fact, the considered digital component is designed for processing data samples, in particular signals, up to 200 elements. So, it is necessary to keep a table of results with 200 calculated estimates of information entropy, which is 800 bytes. Alternatively, linear interpolation of intermediate values can be used to reduce the amount of memory required to 400 bytes.

III. Implementation of the Proposed Approach

In [1] is shown that the choice of the appropriate entropy value is made if it is presence of a logic zero signal on the control line ena of the CntControl unit, which is fed to the CalcH - the permission line to start the calculation of the HTable100 block.

The signal is generated after the value of the reference pulse counter, which actually sets the scan frequency of the signal line, reaches n = 200.

The number of received single pulses from the signal line is fed to the eight-bit data bus nInput [7..0] of the HTable100 unit, is charged by another meter, the operation of which must be coordinated with the reference pulse generator and signal line.

As a simulation result of signals at the respective inputs of the mentioned digital component, it was found that negative and positive error values do not exceed the aperture 10-5 and they are almost symmetrical, which confirms the acceptability of the proposed implementation of such digital component [5].

Characteristics for absolute error of the obtained simulation results of the developed digital component are given in Figure 2.

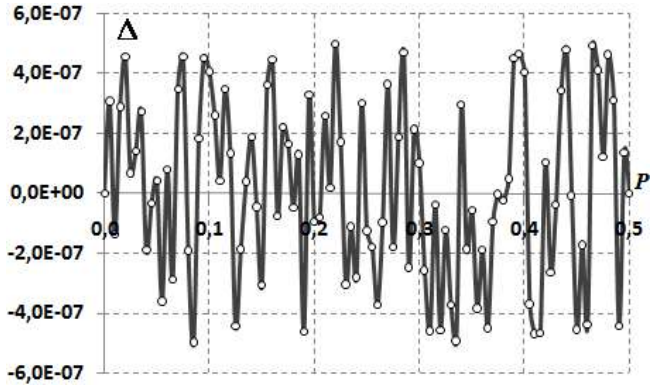

Fig. 2. Absolute error in calculating the information entropy of the developed special processor.

In order to reduce the FPGA hardware resources required to store the information entropy estimation table, it is advisable to consider the possibility of using linear interpolation of intermediate values, which allow to reduce the size of the table by 50%. In this case, the corresponding part of the FPGA resource will be used to perform two arithmetic operations, in particular the operation of unsigned addition and division into two.

It is worth noting that the last operation is easy to replace with a shift operation to the right, which further reduces the computational load.

As a result of simulation signals at the corresponding inputs of the mentioned digital component, it was found that the negative error values do not exceed 10-3 and the positive ones do not exceed 10-5. The result of the absolute error is shown in Figure 3.

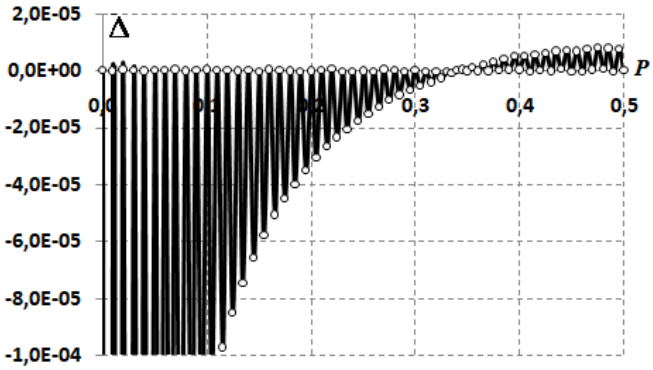

Fig. 3. Absolute error of information entropy calculation for optimized data.

From Figure 3 we can conclude that negative part of the error, the interval [0.0,0.3[, is not acceptable. However, the calculated intermediate values on interval [0.3,0.5] do not actually exceed the errors given in Fig.2.

In this situation, during further conducting research, it is advisable to divide the set of calculated values into separate subsets and use linear interpolation separately for each of the subsets.

Conclusions

Studies have shown that replacing memory resource with a computing resource allows to halve the hardware cost of memory, but requires further research because it does not provide an acceptable error in the calculation of information entropy estimates. The use of arithmetic operations of addition and shift will increase the delay in obtaining the result of such a digital component.

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Algorithm for Finding the Optimal Way to Move a Mobile Platform Among Indefinite Obstacles

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***Abstract*—Abstract. The paper describes a method for determining the trajectory of a mobile robot inside a production room among obstacles. To determine the path of movement, a navigation system is used, which determines the robot's own coordinates, plans the trajectory at the current time and controls its movement. A software tool for modeling the behavior of a mobile robot taking into account the properties of its mechatronic platform is proposed. The model of the adaptive control system of the mobile platform is described. The block diagram of the program for modeling the method of finding the optimal way to move a mobile platform among uncertain obstacles is considered. The simulation results are given.**

Keywords—mobile robot, navigation system, optimal way, model, program.

I. INTRODUCTION

To implement the concept of Industry 4.0 in production, the use of mobile robots to combine industrial equipment into one integrated production process is of particular importance. The task of using robots in a human environment is very difficult. First, it is necessary to pave the way for mobile vehicles to move among objects whose positions are changing dynamically. Secondly, it is necessary to ensure the safety of workers who service the equipment through the use of intelligent sensors.

This paper considers the solution of an important problem - determining the method of optimizing the trajectory of the transport robot in the production site among the inhomogeneous obstacles to reduce the duration of transport operations [1-4].

II. METHOD OF DETERMINING THE TRACTION OF MOTION IN AN UNDEFINED ENVIRONMENT

The proposed method is a combination of the method of finding the optimal trajectory of movement, when all obstacles are identified, and the method of visual odometry to determine changes in the surrounding space [3]. By combining these two methods, we get the opportunity to constantly search and analyze the location of new obstacles that appear in the surrounding space, and quickly respond to changes in real time.

Tasks of the adapted visual system [6]: determination of the location of the robot in the initial position and when moving; orientation of the work in space and relative to the starting point; identification and tracking of objects in the workspace; allocation of impassable areas.

For the analysis of the environment the method of visual odometry is used, the essence of which is stated in the previous sections. This method allows you to link obstacles to a local map. The found changes are immediately applied to the map and then used to lay the optimal route [2-5, 8]. Laying the route according to the map is done using the algorithm A * [5].

Thus, we have three independent processes: obstacle search, map modernization and route planning. The proposed method is similar to the well-known principle of moving robots in space, which is called SLAM (method of simultaneous navigation and mapping). The difference is that in the traditional method, the robot has no idea about the surrounding space and the first step is to study space and build a map.

In our method, the map is already known and loaded into the mobile device's memory. For example, this is very often the case when the robot is working on a production site where the location of the equipment is known in advance.

At the first stage there is a fast paving of a way from a starting point to the set purpose. In the process of moving the work, he constantly scans the simple and monitors changes in the surrounding space. Changes can be caused by the appearance of a person in front of a mobile device, the appearance of another mobile robot, or the movement of products.

Thus, having determined the location of a new obstacle or its disappearance, the robot control module adjusts the trajectory of movement, and determines the optimal route for

this current situation. The proposed algorithm is embedded in the following model of the adaptive control system of the mobile platform in an indeterminate environment, shown in Figure 1.

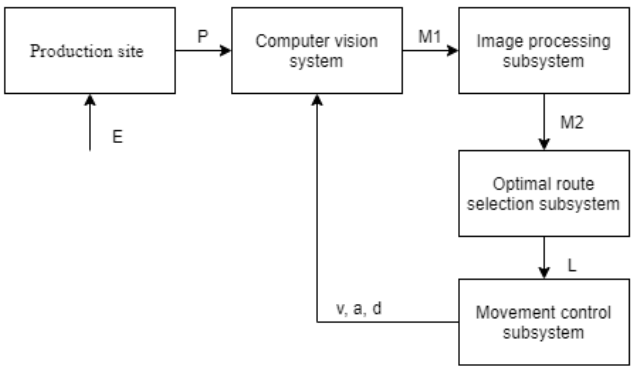

Fig. 1. Model of adaptive mobile platform management system.

The environment consists of objects that do not move and are elements of equipment (O) or room structures, as well as moving objects such as humans or other mobile robots (U).

Thus, each point in space can be represented:

$$P^* \{[O1, O2...], [U1, U2...]\}. \quad (1)$$

The environment can be described by a set of reference points that make up the spatial background that hinders or does not hinder movement:

$$P = \{P^*1, P^*2, \ldots P^*n\}, \quad (2)$$

where P^* – is coordinates of reference points of objects in the room; n – is the number of reference points in space.

$$M1 = \{S, W\}, \quad (3)$$

where S – is method of determining visual coordinates; W – is method parameters.

The parameter L is described as:

$$L = \{\Delta X, \Delta d\}, \quad (4)$$

where X – is the localization of the mobile platform; d – is the direction of movement of the platform.

At the output of the motion control subsystem we get the parameters of influence on the movement of the mobile platform, and hence on the displacement of the computer vision system, which is rigidly connected to the platform (v, a, d). The parameter v describes the change in platform speed. Parameter a describes the angular displacement, and parameter d is the direction of motion.

III. Program for Modeling an Adaptive Mobile Platform Management System

Based on the preliminary analysis, the software tool for modeling the method of finding the optimal way to move the mobile platform among uncertain obstacles has the following independent processes: a) TraceRoute, which is used to build a trajectory based on data about the obstacles found; b) TimerProces – an independent complex process that runs the following functions: space scanning and obstacle search; visualization of the effect of the scanner of the surrounding space; restructuring of the virtual map; c) moving the digital duplicate on the virtual map of the production environment in the found way.

Figure 2 shows the structure of the software.

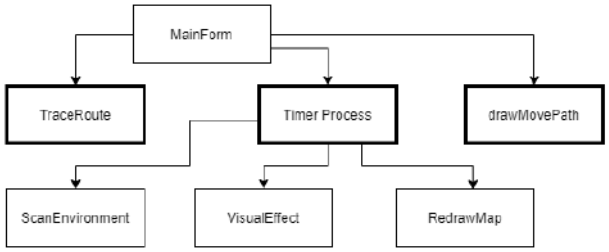

Fig. 2. Block diagram of the program for modeling the method of finding the optimal way to move the mobile platform among uncertain obstacles.

The drawScan () function is used to visualize the space scanning process. To combine all processes, a timer model time calculation function has been developed.

When the movement of the mobile platform is completed and the end point is reached, the timer is turned off and the drawMovePath function is called to visualize the path traveled.

The path is drawn from the data stored in the MovePath array. In this array are entered all the points at which the mobile robot was in the process of movement. The MovePath array changes the mobile platform offset feature. Figure 3 shows an example of the algorithm in the first steps and the result of paving the way.

Fig. 3. Example of the algorithm in the first steps and the result of paving the way.

The path may pass through existing obstacles because at the time of the previous passage they did not exist, but they appeared when changing the trajectory and were taken into account when laying a new path.

CONCLUSIONS

In this work, experimental studies of the practical use of the proposed method of laying the optimal path of movement among uncertain obstacles were performed. Simulation (software) modeling was used for this purpose.

The block diagram of the program for modeling of a method of search of an optimum way of movement of a mobile platform among uncertain obstacles was developed. The program is written in the C # programming language in Visual Studio. The developed method of finding the optimal trajectory was tested in practice and the result of the simulation model showed its efficiency. Algorithm A * is used to route.

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Training of Highly Qualified Specialists in the Electronic Industry Market on an Adaptive Basis

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***Abstract*—The publication is devoted to the study of the main aspects of professional training of highly qualified specialists in the market of electronic industry by substantiating and implementing innovative technologies of forming their competencies on an adaptive basis. The analysis of the peculiarities of professional implementation of electronic industry specialists in constantly changing conditions has been carried out.**

Keywords—professional competencies, specialist, electronic industry market, educational space, adaptability to changing conditions, basics, professional higher education.

I. Problem Statement

Domestic experience shows that the main driving force behind the transformation of the educational process is the process of qualitative transformation of the educational environment for students and other learners. The goal of this is to increase the autonomy and critical thinking ability of applicants through a performance-based approach. This approach involves the use of new methods for the design of learning programs, the teaching process, and the acquisition of knowledge. So, preparing high quality professionals in the electronic industry market involves developing students' ability to think critically, be competitive, solve professional problems effectively, and apply new methods in mastering knowledge and personal development. Therefore, this problem is much broader, and the search for new methods for training future specialists is extremely relevant in the context of modern world educational trends and allows them to be competitive in the labor market.

II. Analysis of Recent Research and Publications

The problems of training specialists in the field of electronic industry, differentiated issues of functioning of the system of professional (vocational) education, issues of development of adaptive systems management and adaptive technologies in the educational process were studied. Monitoring studies on the level of implementation of adaptive processes in education and the formation of a number of mandatory professional competencies in future specialists have been conducted by such scientists as G. Azgaldov, A. Asherov, A. Bagdueva, S. Batyshev, V. Boichuk, T. Borova, Z. Varnaliy, R. Vainola, V. Geyets, A. Dubasenyuk, G. Elnikova, N. Eroshina, L. Zaitseva, M. Klarin, I. Kozlovskaya, M. Koryagin, O. Mazur, A. Maximovich , T. Matsevko, I. Mishchenko, O. Nazarova, G. Polyakova, S. Strizhak, V. Sumtsov, N. Tkacheva, P. Tretyakov, M. Chik, K. Chuyko, T. Shamova, V. Shakhov, L. Shevchenko, V. Yachmeneva and others. However, in this paper we will refer to the works of those scientists who are aimed at researching the level and formation of the intellectual potential of specialists for the adaptive-digital environment.

III. Formulating the Goals of the Article

The aim of the publication is to find new methods, based on the performance approach, to improve the quality of professional training of specialists in the market of electronic industry through the allocation, justification and practical implementation of educational components on an adaptive basis in higher education institutions.

IV. Statement of the Main Material

The current state and trends of active growth of indicators of intellectual development of Ukrainian society, scientific and technological progress and the transition to a new technological mode requires a certain transformation both in society and in the organization of the educational process in particular. Transformation should be aimed at the development of integration processes with advanced European institutions of higher education, taking place against the backdrop of progressive development of qualitative indicators of society. Expansion of international business-social relations should create prerequisites for educational activities in order to increase the human resource potential of specialists in all sectors without exception. In turn, this will not only help to determine the direction of the process of reform and transformation of the educational

sector, but will bring the quality of training specialists in line with the European labor market and thereby strengthen the competitiveness of the education system. The growth of the electronic industry market share in the country's economy requires a gradual increase in the supply of specialists with a certain set of general competences or even universal and narrowly specialized ones.

Taking into account the possibility to study in a dual form and get a second, third education and specialty, general competencies necessarily contain: the ability to think abstractly, analyze and synthesize; the ability to apply acquired knowledge in practical situations; skills to use information and communication technologies, the ability to communicate in a foreign language, etc. And such competences as the ability to work in a team, to show initiative and enterprise, to act responsibly and consciously, in our opinion, in general, are mandatory for a modern person regardless of his profession, education level and place of residence. The ability to preserve and multiply moral, cultural, and scientific values and achievements of society, to realize one's rights and obligations as a member of society, and to realize the values of civil society are universal human values that must be formed starting in pre-school education. But special competences, such as the ability to choose and use appropriate methods, tools to justify decisions in the digital environment and enterprises of electronic industry, can be formed and brought to the demanded level, depending on certain conditions, only in the process of receiving appropriate professional education. The modern labor market on the one hand needs the training of highly qualified and highly specialized specialists, and on the other hand, versatile, perfectly performing tasks, possessing modern professional knowledge and practical skills, but if necessary, quickly and efficiently adapting to the requirements of employers. And the ability to be ready to solve problems in changing and uncertain conditions are considered super competencies. This approach of the employer to the assessment of the specialist forces him/her to constant self-development and self-fulfillment. This is the main motive of an electronic industry specialist to maintain competitiveness.

Interconnection of the subjects of market relations, internationalization of innovative development at the present stage increases the relevance of revision of interaction between education and labor market, guided by the needs of society. In particular, the proper level of professional competences of electronic industry, possession of several qualifications within the profession; ability to effectively interact with specialists from other countries; aspiration to continuous self-development ensures the own competitiveness of an industry specialist, indicates his/her flexibility, mobility, adaptability, ability to self-development.

The development of electronic equipment and software, networks of Internet resources provide great opportunities for their use and application in the educational process of higher education institutions (universities and institutes), and modern innovative methods and means of learning allow to interest students and form an appropriate motivational mechanism with elements of research. Thus, the segment of applying one's competences expands, and reinforcing them with information technology allows one to be confident in one's place in the labor market.

Modernity and development of the educational process in Ukraine shows that education should be carried out and transformed at a certain time, it is necessary to conduct it more intensively, to create conditions for the disclosure of creative and non-standard ideas of students to achieve better results in learning, in addition, it is necessary to create adapted educational and methodological support to prepare high-quality professionals, which met modern conditions of the educational process and the labor market requirements.

The introduction of innovative solutions in the educational process, new methods and teaching technologies require special skills and focus of scientific and pedagogical staff of higher education institutions on personal and professional development, using additional opportunities for international mobility, participation in international scientific events, continuous professional development and use of best practices. Free access to Internet resources, innovative software solutions, information technologies provide additional opportunities both for the applicant and for teachers. It is not only about preparing educational and methodological packages, but also about collecting information and preparing for classes, creating new forms of knowledge acquisition through the introduction of hackathons, business games, theatrical performances, etc. Not only students are trained, but also teachers, who through active forms of learning together acquire the traits of independence and responsibility, flexibility and adaptability, variability, critical thinking.

The development of abilities and their adaptation to the changing working conditions in the digital environment, the definition of own professional interests and intellectual contribute to a constant search for yourself as a person and as a professional. Working in the electronics industry requires a constant search and study of innovative technologies, focusing on the latest electronic components (microcontrollers and FPGA). They are a mandatory component of highly complex, high-performance compact digital systems. Integrated software environments for the design of systems based on these components contain everything you need to develop multi-level verification of digital systems based on a programmable logic integrated circuit (FPGA) and microcomputer (MC). Digital systems are created by programming using serial microcomputers (MC) and parallel programmable logic integrated circuit languages and allow technical devices to acquire a new competitive level, significantly reduce the size and cost. Consequently, the result of their functioning is real and takes the form of profit from the activities of the company-manufacturer.

The application of modern educational and electronic technologies allows universities to be ahead in technical equipment and on its basis to train highly qualified specialists for current and future market needs. This is possible only with a high level of professional competence of scientific and pedagogical staff, capable of solving and teaching practical problems using mathematical methods, laws of physics and principles of electrical engineering. Ability to solve complex specialized problems, to identify and raise problematic issues related to the functioning of electrical systems and information networks, power supply stations and electrical substations; ability to develop projects of electric, electrical and electromechanical equipment in

compliance with the requirements of legislation, standards and technical specifications; to perform professional duties in compliance with the rules of safety, labor protection, industrial hygiene and environmental protection and others - this is only a short list of requirements for specialists in the electronic and electrical engineering industry.

Orientation to rapid changes in the educational process of higher education in Ukraine forms new goals and objectives in the process of educational training. Highly qualified specialist in the market of electronic industry should have adaptive skills to rapid changes and transformations together with fast-flowing requirements of labor market, among them not only knowledge of the basics of electromagnetic field theory and electrical circuit calculation methods, but the ability to use them to solve innovative practical problems; analyze processes in electric power, electrical and electromechanical equipment, related complexes and systems; be able to assess the energy efficiency and reliability of such systems; search for the necessary information, assess its relevance and reliability, and others.

The level of education and the level of personal development of a high-quality specialist on the basis of constantly changing requirements for him/her is a consequence of scientific and technological progress, appearance of new technologies, new methods of organizing business structures in electronic industry, connections between departments in the process of production. Employment of specialists and their work in the process of training will allow to be sure in future employment and willingness of employer to pay money for the result of competence usage for economic development of company. Reduction of social tension on the labor market; decrease of unemployment level; prevention of employee dismissal due to discrepancy between their educational and professional qualification level and new requirements of labor market will lead to fundamental changes in economy of the country. The introduction of competence-based approach to the content of higher education on the basis of educational reforms was fixed in the following legal documents: National Strategy of Education Development of Ukraine (course for the development and implementation of educational standards); Strategy of Sustainable Development Ukraine - 2020 (the right of citizens to have access to education, European standards of living); Individual Priority Action Plans of the Government of Ukraine (creation of favorable conditions for the training of competitive professional staff), the Laws of Ukraine "On Higher Education", "On Education", "On Vocational (Professional) Education" and others.

V. Conclusions and Directions for Further Research

Transformation of modern education imposes new requirements to the process of education, acquisition of knowledge and professional competences. The efficiency of practical activity of a modern highly qualified specialist in the market of electronic industry depends on the level of formation of his thinking, degree of readiness for professional activity, level of developed intellectual and creative personality, ability to make reasonable decisions and adaptability to labor market requirements. Under such conditions, training specialists in higher education institutions requires the introduction of innovative technologies that develop students' competencies.

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Mentoring in IT – the Way to Improve the Skills of a Young Specialist

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***Abstract*—Nowadays, young professionals, graduates of technical universities, often face a lack of professional experience when looking for their first job. In this case, IT companies offer them mentors – their employees for training. What are the benefits and impact of this on the future development of the specialist is discussed in detail in the article.**

Keywords—mentor, tutoring, collaboration.

I. Introduction

During your studies (or after graduation) at the university, the task becomes to find a job in your specialty. A young specialist may be theoretically competent to pass an excellent interview, but lack of practical experience can play a bad role. Companies are understanding of this, and always appoint new employees as mentors.

II. Who is a Mentor and What is Mentoring

To begin with, let's define the concept:

- Mentor – a person who shares his knowledge, becomes a mentor;
- Mentee – person who learns from a mentor.

Mentors are usually needed by people who already have experience, but it is not enough to move to a qualitatively new level. A mentor with his experience and advice acts as a catalyst for growth.

A new developer, a graduate of the Technical University, comes to the company. The company supports mentoring, so beginners are assigned a mentor. Together they go through four phases [1-3]:

A. Acquaintance and definition of tasks

The newcomer gets acquainted with the mentor, talks about his experience and a lot of tasks for which he needs help. The format of interaction is discussed – for example, daily hourly meetings. They decide how to measure the results – in a week or a month the ward has to close the bags, initiate rallies and conduct a code-review.

They agree on the boundaries and topics, the discussion of which will remain between them. The purpose of this stage is to discuss and record agreements between the parties.

B. Development and analysis

At this stage, the ward independently draws up a plan for its development. The mentor analyzes the plan, adjusts it, gives advice based on the strengths and weaknesses of the ward.

C. Work and intervention

The ward starts working on the project according to the plan he previously discussed with the mentor. If necessary, seek advice and clarification. The mentor supports the ward, helps him achieve his goal. And that's why he uses different methods: conducts code reviews, gives advice, just listens carefully.

D. Observation

At this stage, the Mentor is less involved and more observant. He sees the results of the work: the ward takes and closes the bags without the help of colleagues; organized the first rally; performed retro and told about the new feature. Mentor and cops move to the end of cooperation, sum up. After this stage, the mentoring cycle can be repeated, but with other tasks.

Phases can change places, merge, disappear depending on the tasks, levels of mentor and ward. The format is determined by the participants. The main thing is that he arranged both a mentor and a mentee.

III. Responsibilities of the Mentor and the Mentee

The mentor has responsibilities for the mentee:

- Sets with the ward clear goals and objectives;
- Takes the initiative in the relationship, but allows the ward to take responsibility for his growth, development and career planning;
- Undertakes to develop the relationship over a period of time;
- Undertakes to meet with the ward on a regular basis;
- Actively listens to the ward;
- Provides open, honest and constructive feedback;
- Maintains confidentiality;
- Analyzes the goals and objectives of the ward;

- Recognizes conflicts and resolves them with concern, invites to discuss differences with the ward and, if necessary, involves a third party to help;
- Maintains a professional relationship, does not interfere with the personal life of the ward.

In order for mentoring to be beneficial, the mentor creates a safe and respectful environment in which the ward does not hesitate to ask questions.

The mentee also has responsibilities. Without them, there is no point in mentoring.

The responsibilities mentees:

- Defines initial learning goals and success measures together with the mentor;
- Remains open, seeks feedback;
- Takes an active part in their own learning and helps manage the process;
- Plans to communicate with mentors;
- He fulfills his commitments and takes conscious risks, trying new options and patterns of behavior.

The mentor is not responsible for the result. He shares his experience. The last decision is for the ward. He can follow the advice, take it into account, ignore it. But it is always important to explain your decision, because mentoring is a two-way learning process.

IV. How to Get the Maximum Benefits of Working with the Mentor

In the first week it is recommended to give the student full unlimited questions. It creates a sense of trust and security. Don't be ashamed to ask questions, even if they seem silly. Clarification of details, a request to once again explain the incomprehensible concept – it helps to learn more deeply than listening to the thoughts "I'll figure it out later". After the first week, it is recommended to discuss a time that is convenient for both to ask questions.

The main thing is to perform the duties of a cop before the mentor, which were mentioned above. You need to be prepared for the fact that you have to do homework, meet regularly, talk about successes and failures. It is very good to develop a rule of 15 minutes – if there is a dead end in solving the problem, the cop first tries to solve the problem for 15 minutes, and then goes to the mentor for advice. This adds dynamism and does not get “stuck”.

V. What is the Benefit for the Mentor

There are also many advantages not only for the mentee, but also for the mentor [2, 4-6].

Contribution to the company. Mentoring is a sign of your interest in long-term cooperation with your company.

Personal development. Mentoring is a personal development, because in the process such skills are practiced and strengthened as:

- Professional competence;
- Communication and empathy skills;
- Ability to clearly present information, highlight the main thing;
- Discipline and organization;
- Patience and courtesy;
- Emotional resilience.

Mentoring allows you to scale the experience. Anton Babenko, BA Director at Anadea Inc [2] notes that this “…allows me to scale the experience I have gained, because when you are a mentor, you delve into completely different domains, projects, problems and tasks. Thus, it is possible to study and apply approaches that cannot be applied in your project”.

Mentoring helps keep your brain toned. In working with mentee there is always a chance to discover something new and look at a situation from a new angle [3, 7, 8].

Conclusion

Thus, mentoring in IT is an integral part of the training of every young professional today. This approach to learning and sharing experiences has many positive consequences for all parties. Being a mentor, learning from a mentor is an extremely difficult but important job that helps the next generation of developers become better.

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Enhancement of the Laboratory Workshop on FPGA: Opportunities and Prospects

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***Abstract*—This article is a analysis on the design of systems based on FPGAs from different manufacturers based on OpenSource. Popular boards from leading manufacturers are considered. Options for creating a product using software from both FPGA developers and the developer community are proposed.**

Keywords—FPGA, SymbiFlow, F4FPGA, open source toolchain, Xilinx, Intel.

I. INTRODUCTION

The MTS department conducts remote classes for specialties from several faculties in a discipline consisting of 3 parts:

- Digital signal processing
- Microcontrollers
- FPGAs

To conduct classes remotely for the 2nd and 3rd parts of the "Designing devices on microcontrollers and FPGAs" course, laboratory works are being carried out on boards in the laboratory of the MTS department. Laboratory assistants ruler out connection - disconnection of test boards and measuring equipment. And for microcontroller part to conduct classes, everything is fine: there are enough boards for conducting classes simultaneously in 2 laboratories of the department, the software is supported by different operating systems and has an acceptable volume [1-7]. The most nimble students buy boards for experiments. Some even purchase small-sized oscilloscopes.

But to learn or use an FPGA product is a completely different matter.

II. MAIN PART

The leader in the world of FPGAs is Xilinx, and this is one of the reasons why boards of this particular line are used at the department. Artix-7-T100 is used from the model range and Zynq-7000 is chosen for the perspective of improving the laboratory practice and/or creating special courses. Though this is not the only FPGA prodictive company. And it is also not all rosy. And, of course, we wish it prosperity, although we cannot properly register on its website to download free software from the territory of Ukraine.

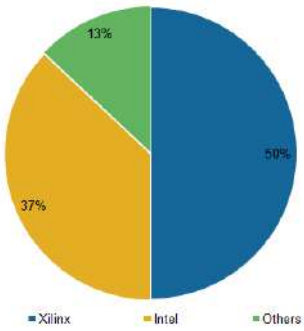

Fig. 1. Programmable Logic Devices' Vendors by Revenue in Calendar 2015.

But if you manage to register, you can use the wonderful Xilinx software. In Vivado or Vitis variants. The operating systems are either Windows or Linux. As for Vivado, in this product you can create and verify an HDL model, simulate a model, trace a project for an FPGA and create a loading sequence, that is, the entire set of tasks. And also it makes possible many other things, for example, the formation of libraries, the creation and adaptation of IP kernels, the study of its really huge documentation. Vivado includes several simulators: Vivado Sim, ModelSim, Questa Advanced Sim, Riviera Pro, Active-HDL. There are plenty to choose from.

For new products, Xilinx recommends Vitis. This product is probably even better and more by its size. In real life, a user usually does not have unnecessary space on the hard disk. And if there is, then it is a little of it. And to install Vivado, it takes about 30 GB, and Vitis is almost 2 times more.

And this is only one firm, and there is something else on the market. No, we're not going to cover everything. But we like to dream.

For relatively low range Xilinx proposes [8]:

- Spartan-6. FPGAs of the 6th family of Xilinx manufactured using 45 nm technology. Designed for use in cost-effective applications (consumer electronics, wired and wireless communications).
- Spartan-7 I/O Optimization with Highest Performance/Watt. Combining 7 series 28nm programmable logic with high I/O counts, Spartan-7 devices are ideal for any-to-any connectivity, sensor fusion, and embedded vison applications.
- Artix-7 Transceiver Optimized With up to sixteen 6.6Gb/s transceivers and DDR3 support, the Artix-7 family provides the best value for power-sensitive applications such as software-defined radio and low-end wireless backhaul.
- Zynq-7000. Hardware & Software Adaptable SoC For applications typically pairing an application processor with an FPGA, the Zynq®-7000 SoC is the single-chip solution, eliminating die-to-die latency and reducing BOM cost.

Intel in its product line proposes [9]:

- Intel Agilex FPGAs. The Intel Agilex FPGA family, built on 10 nm SuperFin technology (F-Series and I-Series) and Intel 7 technology (M-Series), enables customized acceleration and connectivity for a wide range of compute and bandwidth intensive applications, while providing an improvement in performance and reduction in power. [Intel FPGA product catalog].
- Intel Stratix. The Intel Stratix FPGA and SoC family enables you to deliver high-performance, state-of-the-art products to market faster with lower risk and higher productivity. Flagman.
- Intel Arria. The Intel Arria device family delivers performance and power efficiency in the midrange. The last word is the key.
- Intel Cyclone. The Intel Cyclone FPGA series is built to meet your low-power, cost-sensitive design needs, enabling you to get to market faster. Very interesting and widely used by enthusiasts.

Intel Max. The Intel MAX 10 FPGAs will revolutionize non-volatile integration by delivering advanced processing capabilities in a low-cost, single-chip small form. CPLD.

Intel eASIC Intel eASIC structured ASIC devices complete the gap between FPGA and ASIC by delivering lower power and lower unit price versus FPGAs and lower nonrecurring engineering (NRE) and faster time to market versus standard cell ASICs. Production.

It seems to be no system on a chip (FPGA with a processor).

Software. Quartus Prime and Quartus II are downloadable from the Intel site. There is a free version.

Other manufacturers are doing a good job of occupying a stable niche in this market and are worthy of every respect. To name a few it should be mentioned Lattice. Low power FPGA. (ICE40 Ultra, ECP5, LatticeECP3) and QuickLogic

III. Practical Aspects

And what would we like. According to the impression from communication with colleagues, ISE webpack is perceived by students better than Vivado. Because this product is smaller, more transparent, clearer, better for understanding. But it does not support Artix 7, so it is not suitable for us. More, to make a load sequence, one need to use a stand-alone utility, since there is no such function in ISE. In general, there are fewer functions. And so, returning to the command line is not our way. Although for understanding and taking into account pressing factors, everything can be possible. The general scheme of designing devices on HDL (Fig. 2).

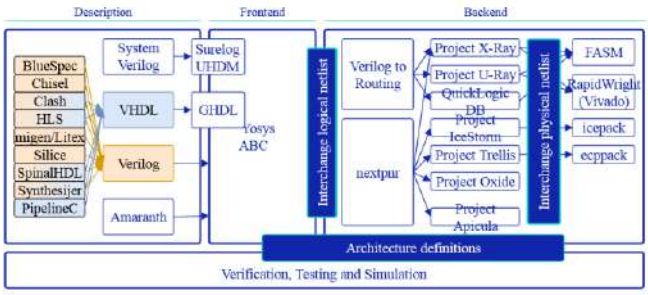

Fig. 2. The general scheme of designing devices on HDL.

But there are enthusiasts [10]. They create to make our life easier and at the same time unite efforts .The purpose of their pleasant pastime is the development of a full cycle project on an FPGA based on open source software. Platform is Linux. Includes FPGA synthesis and tools supporting design tracing for popular boards. Of course, only the lower price segments of the manufacturers' lines are considered, the review of which is higher.

SymbiFlow (now F4FPGA) is a fully open source toolchain for the development of FPGAs of multiple vendors. Currently, it targets the Xilinx 7-Series, Lattice iCE40, Lattice ECP5 FPGAs, QuickLogic EOS S3 and is gradually being expanded to provide a comprehensive end-to-end FPGA synthesis flow (Fig. 3).

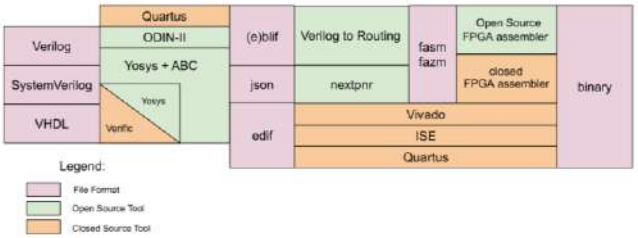

Fig. 3. F4FPGA Toolchain design flow.

The central resources are the so-called FPGA “architecture definitions” (i.e. documentation of how specific FPGAs work internally) and the “interchange schema” (for logical and physical netlists). Those definitions serve as input to frontend and backend tools, such as Yosys , nextpnr and Verilog to Routing. They are created within separate collaborating projects targeting different FPGAs:

- Project X-Ray for Xilinx 7-Series.
- Project IceStorm for Lattice iCE40.

- Project Trellis for Lattice ECP5 FPGAs.

To prepare a working bitstream for a particular FPGA chip, the toolchain goes through the following stages:

- A description of the FPGA chip is created with the information from the relevant bitstream documentation project. This part is done within the F4PGA Architecture Definitions. The project prepares information about the timings and resources available in the chip needed at the implementation stage, as well as techmaps for the synthesis tools.
- Then, logic synthesis is carried out in the Yosys framework, which expresses the user-provided hardware description by means of the block and connection types available in the chosen chip.
- The next step is implementation. Placement and routing tools put individual blocks from the synthesis description in specific chip locations and create paths between them. To do that, F4PGA uses either nextpnr or Verilog to Routing.
- Finally, the design properties are translated into a set of features available in the given FPGA chip. These features are saved in the FASM format, which is developed as part of F4PGA. The FASM file is then translated to a bitstream, using the information from the bitstream documentation projects.

Only Verilog is used as the description language. If it's VHDL, it needs to be translated to Verilog.

Supported Architectures:

- Xilinx 7-Series: the most popular Xilinx FPGA family.
- Lattice ice40: world's smallest FPGAs for mobile devices.
- Lattice ecp5: low cost FPGAs with high performance features.
- QuickLogic EOS S3: FPGA + CPU sensor processing platform.
- QuickLogic QLF K4N8: a 24x24 eFPGA with 6144 flip-flops, 4608 LUT4s, adder and shift-register support.

Somewhere the use of the Zynq 7000 is considered, but on average the lower price segment is exploited. Are big systems the lot of big companies and big money?

CONCLUSION

Currently, the MTS department uses Vivado software fo FPGA labs. But the team is closely following the trends in the market.

Taking into account the specifics of the moment, we want to use a convenient product with a suitable set of functions. And maybe it doesn't have to be all the features of all the products in the line. Using the F4FPGA does not seem to be too simple from a methodological point of view, but it may be one of the options if it is not possible to install a large product, for example, due to lack of memory. Another option would be to use Python and the HDL library. Just a big shed with a set of tools for all occasions (Vivado or Vitis) you can't take with you on the road. The proposal of possible further solutions is presented in fig. 4.

Fig. 4. The proposal of possible further solutions.

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Development of Testbenches Base on STM32 and CC253X Microcontrollers

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***Abstract*—The purpose of the development is to create a test layout on the STM32 microcontroller and CC253X expansion module. Performing this work had to consider the following steps: analysis of similar devices and expansion modules; develop the spatial structure of the device and its layout; develop the design of the printing module; conduct testing; integrate the test layout and expansion module.**

Keywords—STM32, microcontroller, expansion module, testbench, CC2530, SPI, I2C, GPIO, testing.

I. INTRODUCTION

This template, A test bench or testing workbench is an environment used to verify the correctness or soundness of a design or model [1]. The Wireless sensor networks (WSN) systems have a lot of problems like security, energy consumption, heterogeneity and other disadvantages that need be solved. Therefore, it is quite difficult to design a sensor network node so that it satisfies the necessary criteria for optimality. If such a node is also used for testing and training, then additional requirements for the construction will be propose to, for example, as in articles of designing microprocessor systems [2] or embedded control systems [3]. Energy monitoring [4] is a key factor for the successful prolongation of life times each nodes in wireless sensor network, for examples reducing the power consumption of nodes [5].

STM32 is a family of 32-bit microcontrollers from STMicroelectronics. STM32 chips are grouped in series, each using the same 32-bit ARM core. The CC2530 is a true system-on-chip (SoC) solution for IEEE 802.15.4, Zigbee and RF4CE applications. The CC2538 is the ideal wireless microcontroller System-on-Chip (SoC) for high-performance ZigBee applications.

Performing this work had to consider the following steps: analysis of similar devices and expansion modules; develop the spatial structure of the device and its layout; develop the design of the printing module; conduct testing; integrate the test layout and expansion module.

II. PREPARE YOUR PAPER BEFORE STYLING ANALYSIS OF SIMILAR DEVICES AND EXPANSION MODULES

We analyzed various approaches to the design of such stands - with the presence of a scheme for additional installation (Fig.1) and without it (Fig. 2).

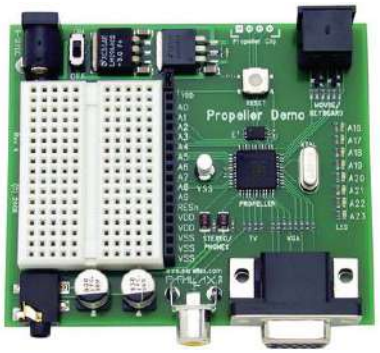

Fig. 1. PCB testbench board with additional installation.

The stand (Fig. 2) the typical implementation of debug bench.

Fig. 2. Typical implementation of debug bench.

We also looked at typical breadboards for modeling - conductive modeling (Fig.3), soldering, (Fig. 4), prepared printed circuit board (Fig. 5).

III. THE USE OF THESE BOARDS FOR TESTBENCH WAS ALSO ANALYZED (FIG. 6).DEVELOPMENT OF THE MODULE BASE ON STM32

As a result of the analysis and design, a printed circuit board was developed and the module was assembled. The Fig. 7 shows the appearance of the text layout and its layout.

The developed expansion module is shown in the (Fig. 8).

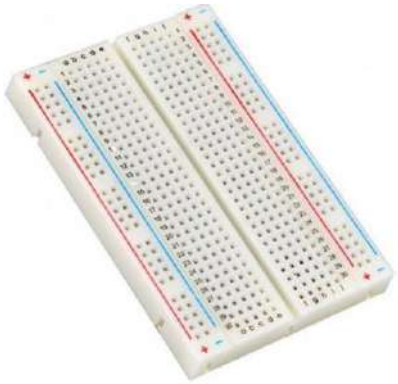

Fig. 3. PCB testbench board with expansion module.

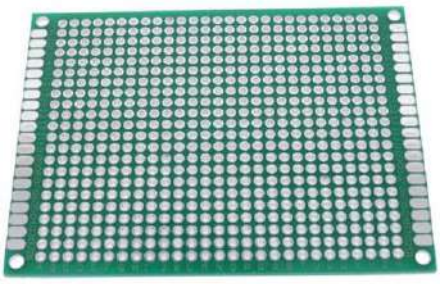

Fig. 4. Testbench board for soldering.

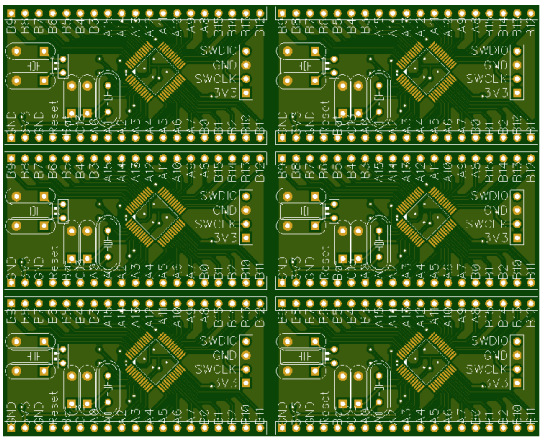

Fig. 5. PCB testbench board .

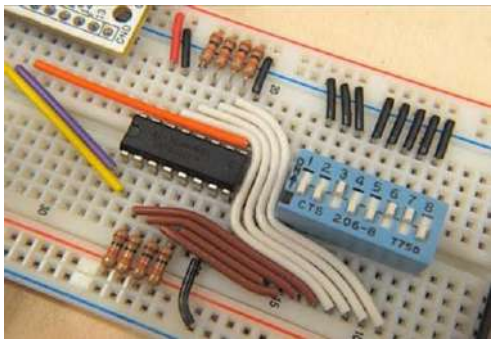

Fig. 6. Testbench board with conductive modeling.

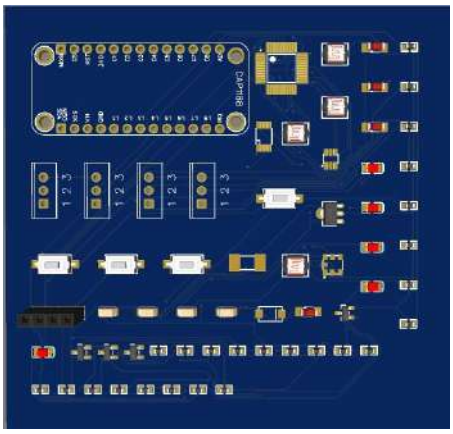

Fig. 7. STM32 testbench base on STM32 microcontroller F103C8 series.

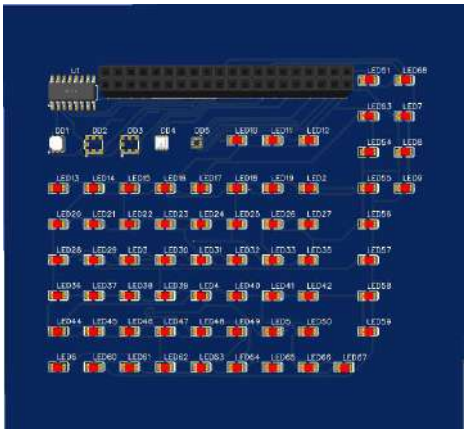

Fig. 8. Developed expansion module.

The proposed model defining defines different levels of system interaction. Each level performs certain functions in such interaction (Fig. 8).

IV. Development of the Module Base on CC2530

There are various modules based on the SoC CC2530 [9], in essence they are a board that hosts the CC2530 itself, an external quartz resonator, several passive components, an antenna connector (or built-in antenna) and outputs for connecting to other devices. The typical node of wireless sensor network can be constructed using a chip CC2530. This transceiver can be ready for prototyping by PCB board-module (Fig. 9).

Developed testbench base on CC2530 shown at the (Fig. 10).

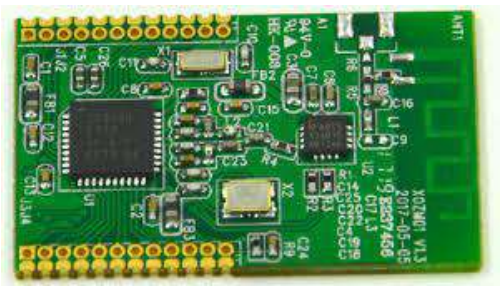

Fig. 9. PCB board-module base on chip CC2530.

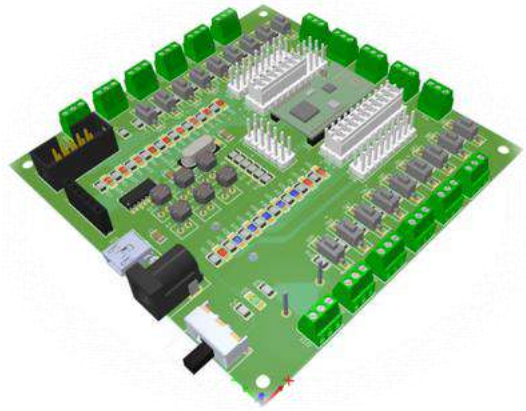

Fig. 10. PCB testbench base on chip CC2530.

V. Development of the Module Base on CC2538

The ZigBee CC2538 module with the CC2592 amplifier is intended for building a ZigBee radio network. The module differs from similar modules in its small size, large programming capabilities and long range. The module consists of a SoC based on SS2538, which has an integrated Cortex M3 processor, RAM 32Kb, Flash 512Kb, several groups of ports for different purposes, ADC, and RFcomm. The second chip is a power amplifier, preamplifier, switches.

As a result of the analysis, the node structures, wireless sensor network modules, CC2538 peripherals were analyzed. A module based on the CC2538 was chosen as the hardware. As elements of the periphery, the following elements were chosen: LEDs; push buttons; temperature, humidity and pressure sensor in the one case; buzzer; hall sensor; lighting sensor; voltage divider with adjustable resistor.

A contact switch is selected to switch between the peripheral elements, and electrical switch for switching between external and internal peripheral (Fig. 11).

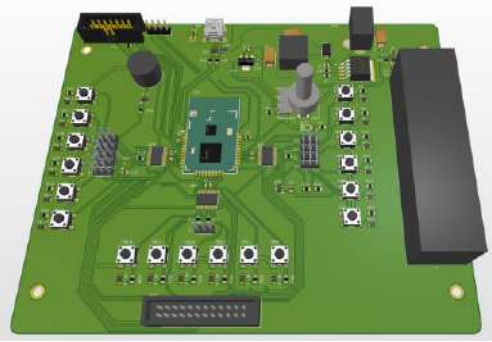

Fig. 11. PCB testbench base on chip CC2538.

Conclusions

Developed of testbenches base on STM3, CC2530, CC2538 microcontrollers. The during of research, it was considered optimize the structure of the node, selection of chip for wireless sensor network node and discussion about peripheral requirements development. Similar constructions and modules are analyzed[1-8]. A test layout based on the STM32 microcontroller has been developed. A test layout based on the CC2530 and CC2538 microcontroller has been developed. Three different models for testing embedded systems have been proposed.

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Practical Aspects of Software Optimization for MCUs with RTOS

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***Abstract*—This paper is focused on some practical aspects of optimization of MCU software written in C programming language using RTOS. Machine-specific optimizations and RTOS specific optimizations are described.**

Keywords—optimization, RTOS, MCU, periphery.

I. Introduction

The task of optimizing MCU software often appears in the process of developing and extending existing software. Although there is a lot of information on C programming language software optimization, the area of MCU software optimization remains largely undescribed. RTOS software optimizations are also extremely under-documented.

II. Before Optimization

The optimization process begins with searching for bottlenecks. Bottlenecks are searched by profiler integrated into debugger or by means of RTOS [1]. There are also IDE plugins for RTOS profiling [2]. It is also possible to perform profiling on your own.

When the bottlenecks are detected, it is necessary to determine what place consumes so much memory resource or processor time for a certain code fragment. In order to do this, a more detailed profiling is performed, determining how much time it takes to execute each function in a given code section, until you get to the clean code and library functions or system calls.

Understanding assembly code and architecture is necessary to analyse why normal code (without system and library calls) takes a long time to execute. For example, some calculations can be done using floating point numbers, which will take much longer than the same code using integer calculations.

Bottleneck analysis in system and library calls is more difficult because the source code is often unavailable. Generally, this is solved by a detailed inspection of the documentation. In some cases, it is possible to try to analyse the assembler code. When the bottleneck is the usage of libraries, there are the following solutions:

- rewrite the code without using third-party libraries, or system calls;
- to use more optimized versions of libraries;
- to use calls which use fewer resources but give the same or similar result.

III. Optimization Methods

A lot of information on optimization of programs for MCU written in C can be found in open access [3, 4]. There are also user's guides for program optimization for particular compilers [5] and particular MCU [6]. Here will be described some optimization techniques which are rarely described and which give significant performance gain.

A. Machine-specific optimizations

Define abbreviations and acronyms the first time they are used in the text, even after they have been defined in the abstract. Abbreviations such as IEEE, SI, MKS, CGS, sc, dc, and rms do not have to be defined. Do not use abbreviations in the title or heads unless they are unavoidable.

1) Copy code and constants to RAM or other "fast" memory: depending on the MCU architecture, this can improve the code execution time. For example, in many TMS devices of F28xxx family the speed of code execution is lower from flash memory than from RAM. Also, the speed of reading the constants from the flash memory, may have latency in the absence of prefetch data mechanisms [3]. In this case, can be recommended the placement of the most frequently executed or time-critical functions, as well as the constants associated with them in the RAM, additionally to methods of code optimization. For various devices and clock frequencies, this can give performance gains from 2.5% to 40% [7].

2) Intrinsic functions: Most microcontrollers architectures provide intrinsic functions for simplifying and increasing the performance of the most commonly used

tasks. For example, the Corterx-M4 kernel contains intrinsic functions for byte and bit reordering, which are useful in communication tasks [8]. There are also internal functions for frequently occurring DSP addition/subtraction with saturation.

3) Using more peripherals: One of the ways of offloading the CPU is to use more peripherals. Modern MCUs have a lot of peripherals which can do completely different things for the CPU. It is also possible to change the program, or algorithm, to make more usage of the peripherals.

a) Copying data using DMA instead of CPU resources: The C memcpy function in RTOS does not use DMA, so in order to copy large amounts of data frequently, it would be better to configure DMA.

b) Check-sum calculation: Many controllers have built-in peripherals to calculate error detection codes - for example CRC, or SHA-256. In case of need to increase performance of controller, it is recommended to use them.

c) Usage of timers, or the built-in RTOS delay functions, instead of using the C delay function: Often there is a requirement of implementation delays in MCU programming. For this purpose, you can use the function delay, which implements the delay by means of CPU. It is preferably to use RTOS facilities to implement delays (e.g. vTaskDelay in FreeRTOS [9]), or the MCU's timers. To implement delay accurately, it is necessary to use only the MCU timer with interrupts at the end of the time interval.

4) Using fixed-point arithmetic instead of float-point: Using fixed-point arithmetic (IQmath for example) instead of floating-point arithmetic in many architectures can give a performance gain, despite the fact that floating-point computation in many MCUs is handled by the peripheral coprocessor. At first look, it seems to contradict the previous point, but with floating point math the CPU is forced to stay idle while waiting for the operation to complete and for the result to be available. Additionally, to this time is added the time of copying values into the coprocessor registers and copying the result. Often, this time is longer than performing the same operation using fixed point arithmetic. Thus, it is recommended to use integer math in heavily loaded parts of the program. If it is impossible to refuse the floating-point arithmetic (for example, the required functions are missing in the library), it is possible to use optimized computation libraries (such as Fast RTS for the C2000 architecture by TI) or extension of the FPU - like TMU in C2000.

B. RTOS specific optimization

1) System calls cutting: One of the ways of optimizing time-critical interrupts is to remove RTOS code from interrupt begin and end. RTOS monitors the interrupt to check if higher priority tasks that may have been released during the interrupt operation are needed. If the interrupt does not use RTOS calls then it can bypass RTOS and interrupt hooks, profiling and other functions provided by OC will not be available. In case of need to profile such interrupts, it will be possible to use built in timers of MC by implementing profiling functions yourself.

2) Place more code into task and only necessary code into ISR: The main idea when placing code into interrupt handlers is: "Place only necessary code into ISR". Moving code between interrupts and tasks does not free up additional CPU resources, but allows the device to be more responsive to external impacts. However, if an interrupt is executed more often than a task, it will free up CPU resources. Also, it is worth actively using memoization, with the transfer of rare calculations to low-priority RTOS tasks.

3) Refuse usage of FPU in interrupts, or tasks: The usage of FPU coprocessor in applications with RTOS involves the need of saving FPU registers in the task stack and recovery (in addition to the ALU registers). For example, in STM32F4 MCU FPU has 32 single precision registers [10] (each 32-bits) that also have to be stacked in addition to 12 general-purpose registers and other registers. Such storing and restoring is performed by the CPU, and could be done every time tasks are switched and interrupts are entered. As an intermediate optimization, it is possible to allocate usage of FPU only in one handler of the program - a task, or interrupt. In such case there is no need to save and restore FPU registers, because other parts of the program will not use the coprocessor. In addition to the previous point, it is possible to move all resource-consuming calculations to low-priority task and do them with FPU using floating point arithmetic.

CONCLUSION

In this paper was described some optimization techniques for MCU software which give significant performance gain. Attention was focused on the optimizations related to the use of RTOS.

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Implementation of the Fibonacci method in AHDL

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***Abstract*—The paper shows that the method of successive approximation is a variant of Fibonacci sequences. The relation by means of which the sequence of quatronacci numbers can be described is presented. The algorithm of operation of the register of sequential approximation for its further realization on FPGA is offered. The text of the Logic block program describing the 8-bit sequential approximation register in AHDL is presented.**

Keywords—AHDL, Fibonacci, FPGA.

I. MAIN PART

The Fibonacci sequence is one of the most famous formulas of mathematics. The Fibonacci sequence is defined as a series of numbers in which each subsequent number is equal to the sum of the previous two [1]. So, for example, if the usual sequence of Fibonacci numbers will look like

0, 1, 1, 2, 3, 5, 8, 13, 21, 34…,

then the triple sequence of Fibonacci numbers (tribonacci) will have the form

0, 1, 1, 2, 4, 7, 13, 24, 44, 81

Accordingly, the sequence of quatrain numbers will look like:

0, 1, 1, 2, 4, 8, 16, 30, 58, 112

If we analyze the last sequence of Fibonacci numbers (quatronachi), we can explicitly determine the five numbers that correspond to the set of numbers that can be obtained using the method of sequential approximation. Accordingly, it can be noted that the method of successive approximation is a variety of Fibonacci sequences. The sequence of quatronacci numbers can be described by a recurrent relation [2]:

$$a_{n+1} = a_n + a_{n-1} + a_{n-2} + a_{n-3}, \qquad (1)$$

where $a_1 = 1$, $a_2 = 1$.

Currently, there are chips that work on the method of sequential approximation: 8-bit serial approximation register MC14549B [3]. At the same time, there is a need for registers with smaller or larger bits, not a multiple of 8, and implemented on FPGA.

The inputs of such a register must be provided with data on the iteration number and the need to increase or decrease the output data. The algorithm of the sequential approximation register is presented in Fig.1. Oscillograms of the sequential approximation register are presented in Fig. 2. The simulation was performed in Quartus Prime Lite Edition 18.0. The operation of this algorithm is as follows:

1. The inputs of the sequential approximation register receive data on the ITR iteration number, and the need to add or subtract data D.

2. If a high logic level is set at input D, a certain number will be added to the previous result, the value of which depends on the iteration number.

3. If a low logic level is set at input D, a certain number will be subtracted from the previous result, the value of which depends on the iteration number.

It is possible to implement the method of sequential approximation using the branching algorithm and the selection operator. The text of the Logic block description program of the 8-bit sequential approximation register in AHDL is as follows.

```
IF D==VCC THEN
        CASE ITR[] IS
                WHEN 0 => RG[].D = 128;
                WHEN 1 => RG[].D = (Q[]+64);
                WHEN 2 => RG[].D = (Q[]+32);
                WHEN 3 => RG[].D = (Q[]+16);
                WHEN 4 => RG[].D = (Q[]+8);
                WHEN 5 => RG[].D = (Q[]+4);
                WHEN 6 => RG[].D = (Q[]+2);
                WHEN 7 => RG[].D = (Q[]+1);
        END CASE;
ELSE
        CASE ITR[] IS
                WHEN 0 => RG[].D = 128;
                WHEN 1 => RG[].D = (Q[]-64);
                WHEN 2 => RG[].D = (Q[]-32);
                WHEN 3 => RG[].D = (Q[]-16);
                WHEN 4 => RG[].D = (Q[]-8);
                WHEN 5 => RG[].D = (Q[]-4);
                WHEN 6 => RG[].D = (Q[]-2);
                WHEN 7 => RG[].D = (Q[]-1);
        END CASE;
```

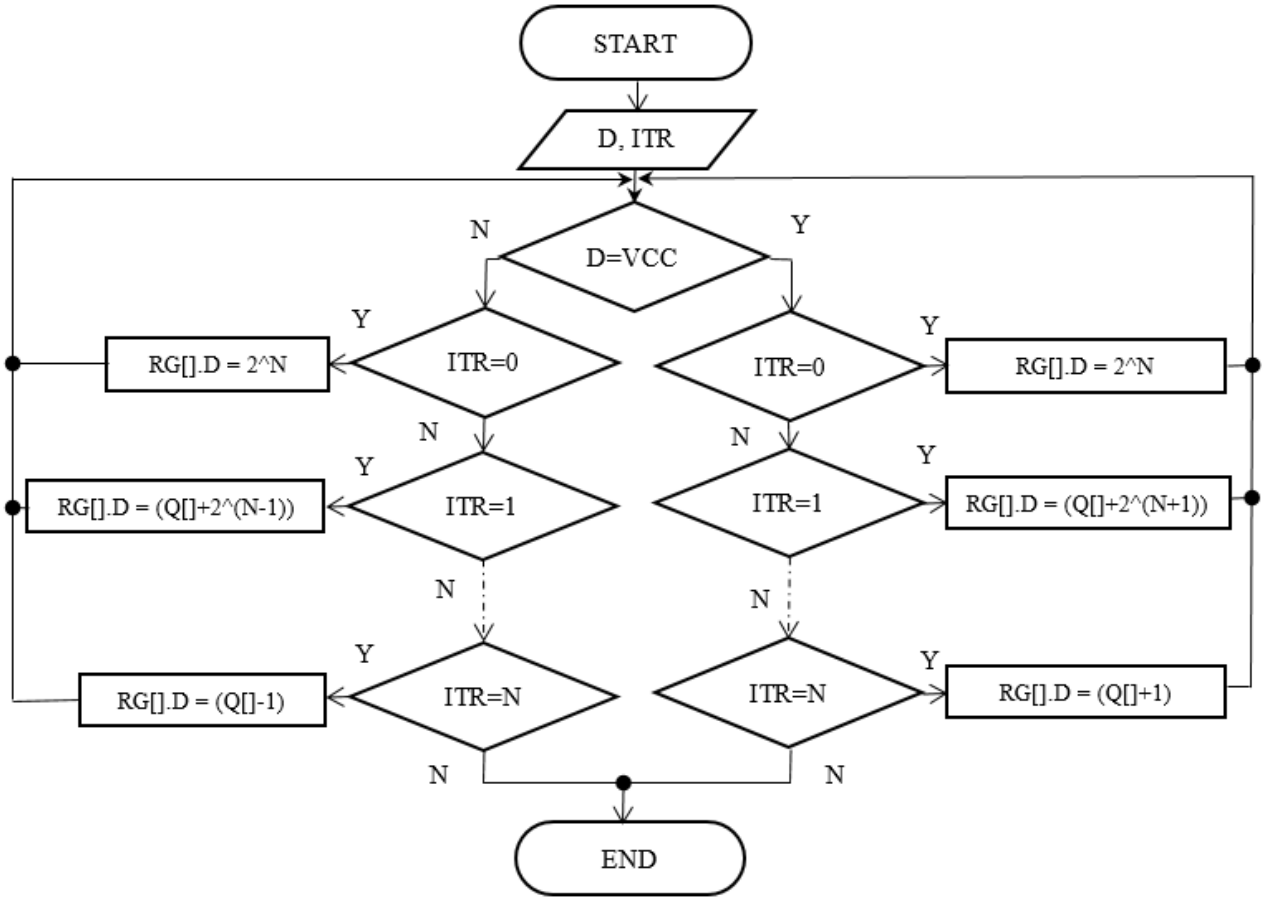

Fig. 1. Algorithm for sequential approximation register operation.

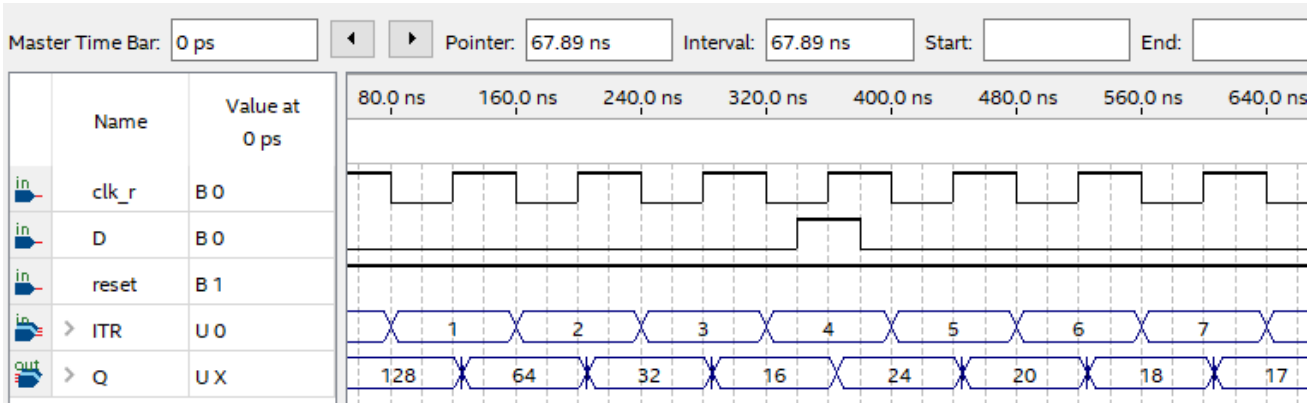

Fig. 2. Oscillograms of the sequential approximation register.

CONCLUSION

From the oscillogram of Fig. 2 shows that as soon as a high-level logic signal appeared at input D, a numerical sequence increased at output Q []. 113 logical elements of FPGA were used to implement the 8-bit sequential approximation register. Similarly, you can implement a register of any bit, which will form any sequence of numbers: Fibonacci, Mersen and others.

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Architectures of Portable Systems for Orientation of the Blind

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***Abstract*—This paper analyzes the differences and disadvantages of various electronic assistants for the blind. It also describes our architecture.**

Keywords—blind, electronic assistant, parallax, tactile feedback.

I. Introduction

There are over 39 million totally blind people in the world, 5.9 million in Africa, 3.2 million in the Americas and 2 million in Europe. Blind people have significant limitations in daily life, mainly in mobility. While they can often learn certain routes (such as showing them how to get to the nearest store or station), this ability is far from being able to move freely.

Various means and aids, such as guide dogs, have been used for centuries to increase the mobility of the blind. In our time, it has become possible to solve this problem by technical means by creating an electronic assistant.

This article will discuss the various architectures of such solutions, the principle of their operation and disadvantages.

II. Types of Electronic Assistants

Electronic assistants are divided into three main groups according to the principle of operation: radar, global positioning, and stereo vision [1].

A. Radar systems

The most widely known electronic assistants are based on the radar principle. These devices emit laser or ultrasonic beams. When a ray hits the surface of an object, it is reflected. Then the distance between the user and the object can be calculated as the time difference between the emitted and received beam, or a depth map can be built if an emitter matrix or lidar is used. The user is then informed about the presence of the object by various methods [2, 3]

The disadvantages of this radar class of devices are various interferences depending on the environment. For example, rainy weather or laying snow will require additional corrections in signal processing.

B. Positional systems

The second type of electronic assistant includes devices based on the global positioning system (GPS). These devices are designed to guide a blind user along a previously selected route; In addition, it provides the user's location, such as street number, intersection, etc. In this group, the most well-known devices are. Their effective range is up to 5m outdoors. Using radio signals supplied by satellites, the device can provide real information about every point on the Earth, informing the user in real-time about their position in the environment.

The disadvantages of position class devices are dependent on an external signal, and as a result, “floating” accuracy of work depending on the location.

C. Parallax based systems

The third type of electronic assistant is based on the parallax effect. The real opportunity to create an affordable device appeared relatively recently, with the advent of affordable cameras. The stereo camera allows you to calculate the distance to an object if you know the base distance between the cameras. Also, having an image can be used for further processing.

The disadvantage of parallax-based devices is their sensitivity to light. Devices using cameras that are not sensitive to infrared radiation will require additional illumination for correct operation at night.

III. Peculiarities of Perception of the Blind that Should be Considered when Developing Electronic Assistants

There are a few things to keep in mind when designing helper systems:

First, losing sight, a person relies more on the remaining senses and most on hearing. When offering a device that uses sound alerts, there is a high probability that users will face distrust the assistant.

Secondly, the white cane is still the main assistant for blind people. The electronic assistant must allow their combined use [4, 5].

Thirdly, taking into account the level of material support for blind people in Ukraine, the device should be available for independent purchase.

IV. Description of the Proposed Architecture

We assume that to solve such a problem, it makes sense to use the available computing power of a smartphone, which will allow using artificial intelligence for higher efficiency and functionality.

We propose the idea of creating a device that will use a stereo camera to detect obstacles and process information on a smartphone transmitted via Bluetooth [6].

This will make it possible to implement various system reactions depending on the class of obstacles. For example, the user must first be informed about dangerous objects such as cars or animals. The use of artificial intelligence will recognize traffic lights and inform users. This will increase their mobility and integration into society.

It is possible to argue about the choice of a specific architecture only after testing its performance in practice. Perhaps it makes sense to train a neural network to recognize generalized classes of objects, such as a tree or a lamppost, these are static objects that can be bypassed. A wall or fence is a static obstacle that cannot be bypassed, and so on. This approach can reduce the required processing power requirements of the end device.

Informing the user will take place using a special feedback module, in the form of a bracer with a matrix of ERM motors that provide a tactile response for the user. Depending on the distance to the interference, with different intensity and/or frequency, the corresponding pixels of the navigation matrix will create a spatial representation of the environment. This design will allow the user to use the hand, for example, to hold a white cane, and leave the other hand free [7].

The Block diagram of the proposed device is shown in Fig.1. In the given block diagram: 1 - user, 2 - tactile response block, 3 - computing block, 4 - stereo camera block.

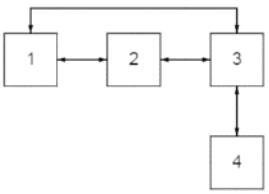

Fig. 1. Block diagram of the proposed device.

Conclusion

Despite the fact that after the Second World War, more than 40 different systems were created, of which only 13 reached the stage of a commercial product [8]. Nothing is known about them in Ukraine. In underdeveloped countries, the situation is even worse. Blind people have little hope for support from the government. Therefore, an affordable device is needed that can be used offline, including in rural areas.

We believe that the device we offer can occupy the niche of an assistant available to blind people with a low level of income, and capable of working in various conditions.

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Formation of Acoustic Interference Based on a Microcontroller for the Suppressor of Unauthorized Speech Recording

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***Abstract*—The report analyzes the effectiveness of suppressing unauthorized speech recording with acoustic countermeasures. To significantly increase the efficiency of suppression, it is proposed to adapt the acoustic method taking into account the peculiarities of the propagation of acoustic oscillations in the air and the psychophysical perception of sounds by the human ear. The results of experimental researches are given and the means of counteraction on the basis of the microcontroller are offered.**

Keywords—speech, unauthorized recording, microcontroller, speech protection device.

I. INTRODUCTION

The urgency of protecting language information is mainly due to two factors: the first - language information is very informative and the second - the widespread use of language recording devices, starting with modern smartphones (today there are more than 4 billion units in the world)who record speech, various dictaphones and ending with special means of recording language that have the ability to counteract the means of suppressing unauthorized recording [1, 2]. Unfortunately, none of the currently known methods of preventing and suppressing unauthorized recording of speech can, without knowledge of the type of recording device, guarantee complete prevention of unauthorized recording of speech information. The article proposes a method and on its basis a tool that significantly increases the effectiveness of counteracting unauthorized recording of voice information, regardless of the type of recording device.

II. ADAPTATION OF ACOUSTICS METHOD FOR INCREASE EFFICIENCIES OF SUPPRESS OF UNAUTHORIZED SPEECH RECORDING

To significantly increase the efficiency of suppression, it is proposed to adapt the acoustic method taking into account the peculiarities of the propagation of acoustic oscillations in the air, psychophysical perception of sounds by the human ear and improving the technical characteristics of the acoustic suppression system. Namely:

1) the distance between the source of the acoustic interference and the probable location of the recorder must be minimized and made smaller than the distance between the source of speech and the recorder;

2) to form an acoustic barrier from the speech of interlocutors. Such a speech interference cannot be filtered out because it occupies the same frequency band as the speech signal.to form an acoustic barrier off the speech of the interlocutors. Such a speech interference cannot be filtered out because it occupies the same frequency band as the speech signal;

3) significantly improve the technical parameters of the speaker system for the emission of speech interference, using an electrostatic acoustic system of radiation, abandoning the use of traditional electrodynamic emitters, which will lead to:

a) increasing the linearity of the frequency response of the speaker system;

b) reducing the magnitude of its nonlinear distortions;

c) narrowing directional diagram of the speaker system.

These changes in the technical parameters of the speaker system will bring the spectral characteristics of the interference as close as possible to the voices of the interlocutors. A narrowing of the directional diagram of the electrostatic speaker system with the same radiant power will lead to:

- increasing the power flux density of the interference signal, which increases the efficiency of suppression of speech recording;
- some reduction in the intensity of the interference signal on the hearing organs of the interlocutors due to the spatial orientation of the acoustic emitter on the possible location of the recording device in the clothes of the visitor.

III. Results of the Experimental Study of the Efficiency of the Adapted Acoustic Method of Suppress of Unauthorized Recording of Speech

To evaluate the effectiveness of the adapted acoustic method of suppression of unauthorized speech recording using an interference generated by an electrostatic emitter, an experiment was conducted - comparison of technical parameters of protection against unauthorized speech recording built using adapted acoustic (EST-ST, EST-P), electromagnetic (SHUMOTRON-3, PD - 2) and ultrasonic (USPD-C, UltraSonic-50) suppression methods for five modern types of sound recorders - digital voice recorders and smartphones (Olimpus VP-20, Edic-mini B76, Galaxy S8 +, Iphone Xs Max, Iphone 12 Pro Max.) The results of the experiment are presented in tables 1-3.

Table I shows the distance of complete suppression of dictaphones when using electromagnetic suppressors "SHUMOTRON-3" and "PD-2"

TABLE I.

Model	SHUMOTRON-3 Radiation power 15W	PD-2 Radiation power 8W
Olimpus VP-20	2,2m	1,6m
Edic-mini B76	0,6m	0,2m
Galaxy S8+	0,3m	0,1m
Iphone Xs Max	0m	0m
Iphone 12 Pro Max	0m	0m

Table II shows the range of complete suppression of voice recorders when using ultrasonic suppressors.

TABLE II.

Model	USPD-C(26 emitters, acoustic pressure 115dB)	UltraSonic-50 (50 emitters, acoustic pressure 115dB)
Olimpus VP-20	0,9m	1,2m
Edic-mini B76	1,1m	1,3m
Galaxy S8+	6m	8m
Iphone Xs Max	1,8m	2,4m
Iphone 12 Pro Max	2,2m	3m

Table III shows the range of complete suppression of dictaphones by ultrasonic suppressors provided that their microphone is closed by a pocket material (the dictaphone is in the pocket).

TABLE III.

Model	USPD-C(26 emitters, acoustic pressure 115dB)	UltraSonic-50 (50 emitters, acoustic pressure 115dB)
Olimpus VP-20	0,1m	1,1m
Edic-mini B76	0,2m	0,3m
Galaxy S8+	0,4m	0,5m
Iphone Xs Max	0,15m	0,2m
Iphone 12 Pro Max	0,2m	0,25m

Table IV shows the range of complete suppression of dictaphones when using electrostatic suppressors "EST-ST" and "EST-P".

TABLE IV.

Model	EST-ST (acoustic sensitivity 88dB)	EST-P (acoustic sensitivity 86dB)
Olimpus VP-20	3,5m	3,2m
Edic-mini B76	2,8m	2,6m
Galaxy S8+	2,46m	2,4m
Iphone Xs Max	2,2m	2m
Iphone 12 Pro Max	1,8m	2m

IV. Development a Work Algorithm of the Protection Device Against Unauthorized Recording With Sound Recording Devices

The means of protection against unauthorized recording by sound recording devices consists of one device. The device includes a microphone, two amplifiers, a unit for generating interference processing and a speaker for signal (interference) reproduction . The functional diagram of the tool is shown in Fig. 1.

When turned on, the device starts recording voice information, namely the voice of the person generating the information to be protected from unauthorized recording on various devices. This is necessary in order to create a language-like interference based on this voice in real time. Once the microphone has generated a signal, it is amplified by a microphone amplifier. With this amplifier, we convert a weak signal from a microphone to a linear one. When the amplifier has done its job, the signal is transmitted to the main executive unit of the formation and processing of the interference, which is a microcontroller. At this stage, the signal is digitized and written to the array. After that, based on the array using the algorithm to create a speech-like interference, a speech-like interference is generated.

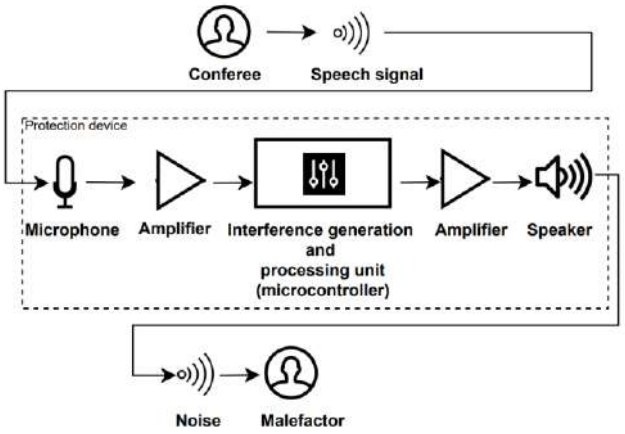

Fig. 1. Functional diagram of the means of protection against unauthorized recording of speech.

The microcontroller controls all the units of the device and performs the main function, namely the generation of speech-like interference. In this device, you can use almost all algorithms to create a speech-like interference. For example, one of them, the digitized speech signal is recorded in two arrays then these arrays are shifted in time and form speech-like interference.

Since the device circuit is quite simple, and the algorithm for creating interference is created using software, it allows you to change the algorithm by reprogramming the microcontroller.

The microcontroller processes the received interference for its further reproduction. After the microcontroller, the interference is fed to the amplifier. The amplifier sends a signal to the speaker playback device. You can see the algorithm of the device in Fig. 2.

Almost every microcontroller that has a DAC or ADC is suitable for project implementation. Among the most popular microcontrollers to date, STMicroelectronics microcontrollers, namely STM32, have proven themselves well. 4th generation microcontrollers (STM32F4 ...) are ideal for this project.

The choice of this microcontroller is also due to the convenient software supplied by the company. It is very convenient to work in the STM32CubeIDE development environment. You can configure HAL in CubeIDE and then do the connection schema.

It was decided to use MAX9814 when choosing a microphone. The module consists of an electronic microphone and a special amplifier on the MAX9814 chip from Maxim. The chip amplifies the sound much better than other amplifiers due to the built-in automatic gain control, which suppresses "loud" sounds and amplifies "quiet" sounds. The module has an additional GAIN input, with which you can adjust the "maximum gain", if you do not connect it, the maximum gain will be 60 dB.

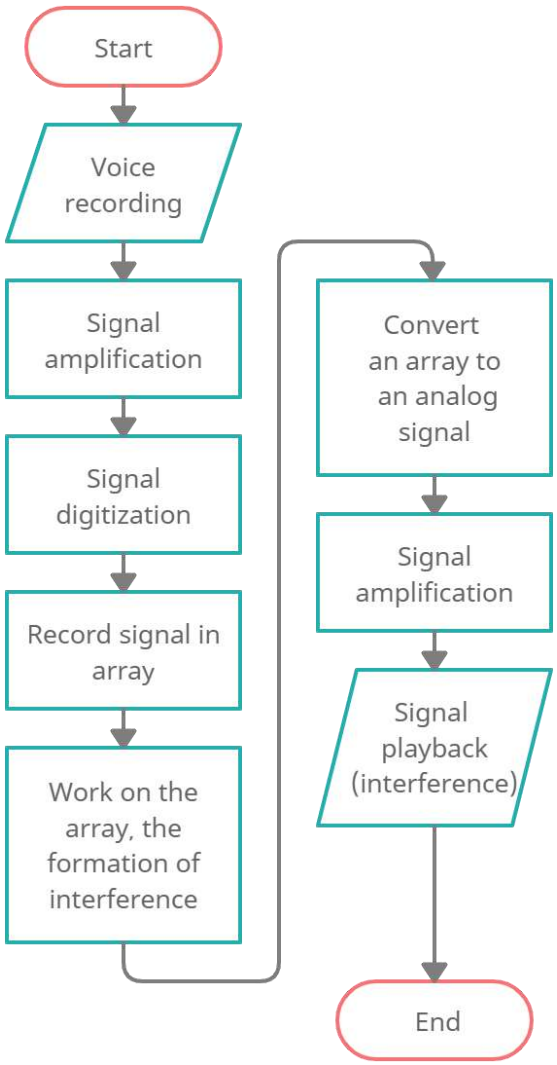

Fig. 2. Algorithm of the device.

CONCLUSION

The algorithm of work of the mean of protection of the information on the basis of the microcontroller is developed. This tool uses an adapted acoustic method to counter unauthorized speech recording. This method is equally effective for all types of recording devices, as the interference is formed by a functional channel - acoustic, taking into account the peculiarities of the propagation and perception of acoustic vibrations by humans in the air.

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Analysis of Sensors as Components of Mobile Robots

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***Abstract*—Given the current trends in robotics, the paper provides an overview of sensors for use in robotics. It is given what characteristics the sensors must meet for further integration into mobile works.**

Keywords—robot, sensor, sensor, device, characteristics of sensors, types of sensors.

I. INTRODUCTION

Sensor systems of robots are the main part of information and measurement systems, the purpose of which is to generate and publish information about the state of objects and processes in the environment and about the robot itself, for the operation of which this information is required.

In many industries and environments, there is a growing demand for rigid multi-purpose work that is easy to operate. Now robots need sensors to understand the context and intuitive interfaces for ease of use. Some applications, for example, may use gesture recognition to control a physical device.

IoT protection, low power consumption, security and reliability - all these are certain requirements and lead to the use of sensors to monitor electricity, temperature and other parameters to ensure that the system operates efficiently and safely. In the near future, robotics will increase the number of engines and the versatility of the environment, and more social robots will appear around the world. The number of sensors used by robots will increase with the development of more control systems and settings [1-5].

II. SENSORS IN ROBOTS AND THEIR CHARACTERISTICS

The sensor is a primary transducer that responds to the value (temperature, pressure, displacement, current, etc.) that is subject to control, and converts it into another value, convenient for further use, giving a signal of its presence and intensity [6]. This signal can be of any physical nature, which can be measured using different principles of operation of the sensitive element of the device.

The characteristics of the sensors allow you to choose the appropriate sensor to work in different situations. Some of the basic attributes of robot sensors are analyzed below [6]:

- precision is this characteristic of the sensor refers to the proximity of the registered value of the sensor to the actual value. It is often called a range of values;
- calibration is the accuracy and resolution of robot sensors can also be improved by calibrating them;
- resolution is this parameter refers to the smallest variable of the input signal that the sensor can detect and reliably specify;
- linearity is this information becomes useful when presenting sensor output to a low-level computer that cannot perform many calculations and compose calibration equations;
- frequency is the peculiarity of robot sensors is that they must give the same result every time the measurement is performed under the same conditions;
- dead zone and hysteresis it's what in mechanical systems such as robots, some error in the gears always causes different values depending on the direction of movement or the dead zone, when the robot sensors do not detect any movement;
- drift;
- temperature range;
- field of vision (FOV) it's what indicates which area (usually angular) can be detected by robot sensors. Horizontal is often mentioned (hFOV) and vertical (vFOV) components;
- the size of the stain is this mainly applies to lasers, but it is important to know how large the spot size is at a given distance. This spot size is crucial to determine the size of visible objects. A small spot size is required to observe through dust, rain and snow. To

do this, you can use both horizontal and vertical scale of spots;

- the shape of the output signal;
- reliability.

III. Types of Sensors and Features of their Use in Robots

A. Contact sensors, pressure sensors

Tactile pressure sensors are useful in robotics because they are sensitive to touch, force and pressure. An example of such a sensor is shown in Fig. 1. If there is a development of a hand (manipulator) robot and it is necessary to measure the force of capture and the pressure required to hold the object, then use this sensor.

Fig. 1. Pressure sensor C7.5B.

Contact sensors include push-button switch, limit switch, etc. These sensors are mainly used for robots that avoid interference. Contact sensors can be easily implemented, but their disadvantage is that they require physical contact. In developing modern humanoid robots, manufacturers are equipping them with these sensors to make devices even more "spiritual", able to perceive information about the world around them literally by touch. There are also capacitive contact sensors that respond only to human touch.

B. Optical sensors and display sensors

These sensors work with a photoresistor. The display sensor (emitter and receiver) allows you to detect white or black areas on the surface, which allows, for example, a wheeled robot to move along a drawn line or to determine the proximity of an obstacle. The light source is often an infrared LED with a lens, and the detector - a photodiode or phototransistor.

The light sensor is used to detect light and create a voltage difference. The two main light sensors are photoresistors and photovoltaic cells. Other types of light sensors, such as phototubes, phototransistors, charge-coupled devices, and so on, are rarely used.

C. Photoresistor

An example of a photoresistor is shown in Fig. 2. These inexpensive sensors can be easily implemented in most robots that depend on lighting.

Photovoltaic cells convert solar radiation into electrical energy. This is especially useful if you plan to build a solar robot. Although the photocell is considered a source of energy, an intelligent implementation in combination with transistors and capacitors can turn it into a sensor.

Fig. 2. Photoresistor LDR.

D. Sound sensors

Sensors are used to safely move robots in space by measuring the distance to the obstacle from a few centimeters to several meters. The sensor detects sound and emits a voltage proportional to the sound. An example of a module with such a sensor is shown in Fig. 3.

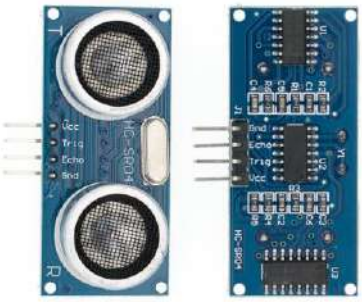

Fig. 3. Ultrasonic module HC-SR04.

These include a microphone (allows you to record sound, voice and noise), rangefinders, which are sensors that measure the distance to nearby objects and other ultrasonic (US) sensors. Ultrasound is especially widely used in almost all fields of robotics.

The operation of the ultrasonic sensor is based on the principle of echolocation. The speaker of the device emits an ultrasonic pulse at a certain frequency and measures the time until it returns to the microphone. Sound locators emit directional sound waves that are reflected from objects, and some of this sound comes back to the sensor. The time of arrival and the intensity of such a return signal provide information about the distance to the nearest objects. These include a microphone (allows you to record sound, voice and noise), rangefinders, which are sensors that measure the distance to nearby objects and other ultrasonic (US) sensors. Ultrasound is especially widely used in almost all fields of robotics.

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Robotic systems, which are part of autonomous submarines, mainly use underwater sonar technology, and on the ground sound locators are mainly used to prevent

collisions only in the immediate vicinity, as these sensors are characterized by a limited range.

A number of other devices alternative to sound locators include radars, lasers and lidars. Instead of sound, this type of rangefinder uses a laser beam reflected from an obstacle. These sensors are more widely used in the development of autonomous vehicles, as they allow the vehicle to cope more efficiently with traffic.

E. Position, tilt, proximity and distance sensors

These types of sensors are used mainly in unmanned vehicles, industrial works, as well as devices that provide self-balancing.

GPS. Satellites orbiting the Earth transmit signals, and a robot receiver receives and processes these signals. The processed information can be used to determine the approximate position and speed of the robot. These GPS systems are extremely useful for robots outdoors, but they do not work indoors. Another disadvantage is their high cost.

Digital magnetic compass. Like a hand-held magnetic compass, a digital magnetic compass provides directional measurements using the Earth's magnetic field, which directs work in the right direction to achieve a goal. An example of a digital compass is shown in Fig. 4. These sensors are cheap compared to GPS modules, but the compass works best with it.

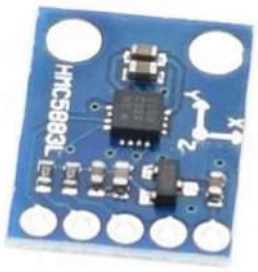

Fig. 4. Digital compass, magnetometer HMC5883L GY-273.

Localization. Artificial landmarks or beacons are placed around the robot, and the robot sensor captures these signals to determine its exact location. Natural landmarks can be doors, windows, walls, and so on, which are perceived by the robot sensor / technical vision system (camera). Localization can be achieved with beacons that generate Wi-Fi, Bluetooth, ultrasound, infrared, infrared, radio, visible light or any other similar signals.

Gyroscope. The gyroscope is used to measure the speed of rotation around a certain axis. This device is especially useful when you need the robot to be independent of gravity to maintain orientation, unlike the accelerometer.

Tilt sensors. They are responsible for balancing and stabilizing any device. And due to the fact that this part is relatively inexpensive, it can be installed in any homemade robot.

IMU. An example of such a module is shown in Fig. 5. IMUs are able to provide feedback, detecting changes in the orientation of the object (pitch, roll and jerk), speed and gravitational forces. Some IMUs go further and integrate a GPS device, providing positional feedback.

Fig. 5. IMU BMI160.

There are different types of proximity sensors, but in this paper we will consider only some of them, which are most often used in works.

Infrared (IR) sensor. The most accessible and simplest type of sensors used in the work to determine the approximation. An example of such a sensor is shown in Fig. 6. In the "beacon" mode, this sensor sends constant signals by which the robot can determine the approximate direction and distance of the beacon. This allows the robot to be programmed so that it always moves in the direction of this beacon. The low cost of this sensor allows you to install it on almost all home-made work, and thus equip them with the ability to move from obstacles.

Ultrasonic distance sensors. The sensor emits an ultrasonic pulse received by the receiver. Since the speed of sound in the air is almost constant and is approximately 344 m/s, the time between sending and receiving is calculated to obtain the distance between the revolution and the obstacle. Ultrasonic distance sensors are especially useful for underwater robots. It is also proposed to use sensors in the JY 450F type machine system [7].

Fig. 6. IR distance sensor E18-D80NK.

Laser distance sensor. The distance is measured by calculating the speed of light and the time required for the light to be reflected from the receiver. These sensors can be used when measuring long distances. An example of this sensor is shown in Fig. 7.

Fig. 7. Laser distance sensor GY-530 on VL53L0X.

Encoders. A transparent and opaque pattern (or black and white pattern) is applied to the rotating disk. When the disk rotates with the wheel, the emitted light is interrupted, generating an output signal. The number of breaks and the diameter of the wheel allow you to determine the distance traveled by the robot.

Stereo camera. Two cameras facing each other can provide depth information via stereo vision.

There are other tensile and bending sensors that are also able to measure distance. But their range is so limited that they are practically not used in the design of mobile robots.

F. Temperature sensors

Temperature sensor is used to automatically measure the temperature in different environments. They provide the voltage difference when the temperature changes. As in computers, the device is used to control the temperature of the processor and its timely cooling.

G. Voltage sensors

Voltage sensors convert low voltage to high or vice versa. One example is an operational amplifier that accepts low voltage, amplifies it, and generates higher voltage at the output. Few voltage sensors are used to determine the potential difference between the two ends (voltage comparator). Even a simple LED can be used as a voltage sensor that can detect a voltage difference and signal it by flashing.

H. Current sensors

Current sensors are electronic circuits that monitor the flow of current in the circuit and emit either proportional voltage or current. Most current sensors emit analog voltage in the range from 0 V to 5 V, which can be processed by a microcontroller.

I. Capacitive sensors

The sensitive surface of a capacitive sensor is formed by two concentrically arranged metal electrodes. If an object approaches the sensitive surface of the sensor, then it enters the electric field in front of the electrode surfaces and contributes to an increase in the coupling capacitance between the plates. In this case, the amplitude of the generator begins to increase. Such sensors are often used in medical robotic systems and devices [8-11].

J. Other sensors for robots

Today, there are a large number of sensors that can detect many technological parameters, and it is almost impossible to list all available sensors. In addition to those analyzed above, there are many other sensors that are used for specific applications. For example: humidity sensors measure humidity; gas sensors are designed to detect certain gases (useful for robots that detect gas leaks); potentiometers are so versatile that they can be used in many different applications; magnetic field sensors determine the strength of the magnetic field around it [12].

CONCLUSION

So the more complex the robot, the more sensors are used. A combination of different sensors may be required to perform one technical task, or different technical tasks may be solved using a single sensor. It is necessary to correctly determine which sensor is best to install on the robot, based on availability, cost and ease of use.

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The Use of GreenPAK Dialog Semiconductor as a Laboratory Basis for the Design of FPGA Devices

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***Abstract*—The peculiarities of modern higher technical education in the conditions of the rapid flow of new scientific and technical solutions within the framework of industrial revolutions are considered. It is shown that the cooperation of higher education institutions and leading industry companies allows to provide training of highly qualified specialists in modern conditions. The rationale for the feasibility of using GreenPAK Dialog Semiconductor as a laboratory basis for technical educational components aimed at designing devices on FPGAs is given.**

Keywords—CPLD, FPGA, GreenPAK, Dialog Semiconductor, laboratory base, higher education, device design.

I. Introduction

Modern higher technical education is based on the rapid development of industrial revolutions and requires higher education institutions (HEIs) to provide appropriate personnel, material and technical, informational and methodical support. At the present time, provision of the appropriate level of material and technical base for the HEI is possible only with the support of production, scientific-production and industrial structures. Such cooperation will allow higher education institutions to train specialists at a high scientific and technical level, and enterprises to obtain qualified personnel with the necessary skills [1-4].

The Department of Microprocessor Technologies and Systems (MTS) of the Kharkiv National University of Radio Electronics (KHNURE) conducts fundamental training of specialists in the field of designing devices on microcontrollers and field programmable gate array integrated circuits (FPGAs) [1-5]. In cooperation with the Dialog Semiconductor company, the MTS department is working on the development of a laboratory workshop based on Dialog Semiconductor's GreenPAK integrated circuits using the GreenPAK Designer software.

Dialog Semiconductor's GreenPAK ICs are a family of configurable mixed-signal integrated circuits (CMICs) that provide miniaturized and customized solutions to common challenges faced by system-level circuit designers. GreenPAK provides means to significantly reduce PCB size, specification cost, and development time. A motivated developer will be able to use GreenPAK in almost most industries. Taking into account the wide range of practical problems solved with the support of GreenPAK, it is advisable to implement this solution in the development of laboratory workshops on the design of devices on programmable logic integrated circuits. The GreenPAK Designer software has a fully graphical design process, requires no programming language or compiler, and has an open distribution license [10].

II. The Main Part

The MTS department teaches the educational component "Design of devices on microcontrollers and programmable logic integrated circuits" module "FPGA" [5-9]. Given the capabilities of Dialog Semiconductor's GreenPAK integrated circuits, the availability of a programmer and the open-license GreenPAK Designer software is a very attractive proposition for use in the educational process for the development of a laboratory base.

GreenPAK™ ICs are a cost-effective programmable non-volatile memory device that enables the integration of many system functions while minimizing component count, board space, and power consumption. Using Dialog's GreenPAK Designer software and the GreenPAK Development Kit, designers can create and program their own circuit in minutes [10-13].

GreenPAK offers the following advantages over a discrete design:

- smaller area on the printed circuit board - plastic cases measuring only 1.0 x 1.2 mm;

- fewer components / lower cost – a typical GreenPAK implementation allows you to save ten to thirty components per instance;
- higher reliability – a smaller number of interconnections on printed circuit boards increases reliability;
- accelerated design - with the help of a full cycle design with GreenPAK Designer;
- reduced power - use of components with low energy consumption and sleep function;
- design security – significantly complicates reverse engineering by disabling reverse reading of the non-volatile memory configuration, which allows you to hide design details;
- tested solutions - each GreenPAK IC is tested, while the discrete circuit is not tested before the final board-level test.

GreenPAK can provide unique subsets of functions [10]:

- GreenPAK dual power supply – a flexible interface of two independent voltage ranges;
- GreenPAK with load switches – GreenPAK configuration with simultaneous control of high current drive power switches;
- GreenPAK with asynchronous state machine - allows you to develop your own state machine designs;
- GreenPAK with regulators with low voltage drop;
- GreenPAK with in-system programming provided;
- high-voltage GreenPAKs – the benefits of combined mixed-signal logic and high-voltage H-bridge functionality;
- automotive GreenPAKs – integration of many system functions in one integrated microcircuit that meets the AEC-Q100 standard;
- analog GreenPAKs – creation of unique analog circuits in combination with customizable GreenPAK logic.

The appearance of the programmer board is shown in Fig. 1. The appearance of integrated circuits is shown in Fig. 2.

Fig. 1. Appearance of the programmer board.

Fig. 2. Appearance of integrated circuits.

The appearance of the programmer board with a representation of the available peripherals is shown in Fig. 3.

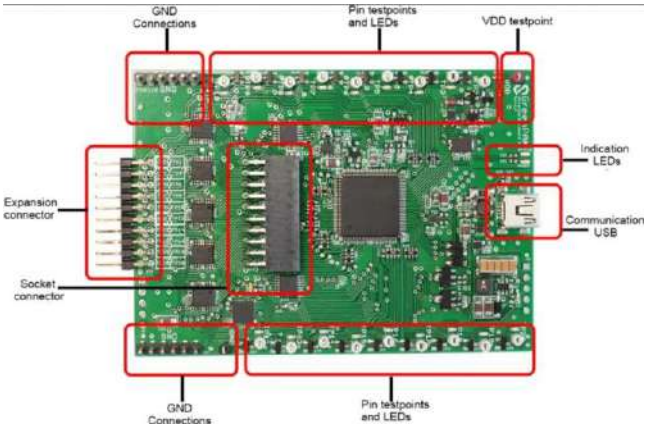

Fig. 3. Programmer's board showing the available peripherals.

Power Supply (Power Supply). The primary power source for the GreenPAK Advanced Development Board is the USB power line. The development board can output voltages from 0 to 5.5 V. To provide this power range, the development board is equipped with a step-up converter. A signal generator with a buffered output controls the power bus of the GreenPAK chip.

USB communication (USB Communication). The board has a USB communication interface that uses a USB mini-B connector. This interface communicates with the control software tool and supplies power to the platform.

GND connections (GND Connections). There are 6 GND pins on the left side, 6 pins and 1 pin on the right side. They can be used as a signal ground the test ground of equipment (oscilloscope, multimeter, etc.) or to connect an external test ground circuit.

Pin Test Points. Each pin of the GreenPAK chip, including VDD, has its own observation reference point. These test points are for observation only. Use the software-controlled expansion jack to connect an external signal source.

Light emitting diodes (LEDs). All pins except pin 2 can be connected to buffered LEDs. This option allows you to visualize the digital levels on the IC pins. There are two selection modes:

- buffered LED (with high input resistance);
- inverted buffered LED (with high input resistance).

Connector (Socket Connector). The optional GreenPAK development board must be used with the removable connector board. Its main purpose is to connect the GreenPAK chip to the programmer board. It is easy to use the programmed chip in external circuits or to measure the current consumption of a realizable project.

Expansion Connector (Expansion Connector). This port was designed to connect the GreenPAK Advanced Development Board to external circuits and supply external power, signal sources and loads. It can be used to apply the GreenPAK chip to your custom design with minimal additional tools.

GreenPAK Designer is a full-featured integrated development environment (IDE) that implements a full cycle of end-to-end design, which includes the stages of: creation of initial project descriptions, synthesis, modeling, placement and tracing on the crystal, crystal configuration and in-crystal hardware setup. It provides direct access to all GreenPAK device features and full control over routing and configuration options. GreenPAK Designer has an integrated programming tool that allows you to program your customized design into your GreenPAK chip. With this tool, you can also read an already programmed chip and export its data to the designer. The designer will generate a project that has the same configuration as the chip. GreenPAK Designer is designed to work in the environment of operating systems (OS): Windows 7/8.1/10, MAC OS X (v10.8 or higher), Ubuntu 18.04 (32, 64-bit), Debian 11 (32, 64-bit) [12].

Digital blocks are the main functional components of any GreenPAK. They include: Look-Up Table (LUT); D Flip-Flop (DFF) / Latch; Counter / Delay (CNT/DLY); I2C (many devices); SPI (select devices); Pattern Generator (PGEN); Pipe Delay; Programmable delay (PDLY); Filter / Edge Detector (Fig. 4) [10-13].

Many components in GreenPAK Designer can be configured as one of several block types. This is indicated by the name of the digital block, for example:

A 2-bit LUT0/DFF/LATCH0 can be, as the name suggests, a LUT, DFF, or Latch. Block type selection is configured using the Type option in the Properties window.

Almost every GreenPAK is equipped with two or more analog comparators [ACMPs], each with two input sources; IN+ and IN-. The input signal source for each is configured in the Properties window.

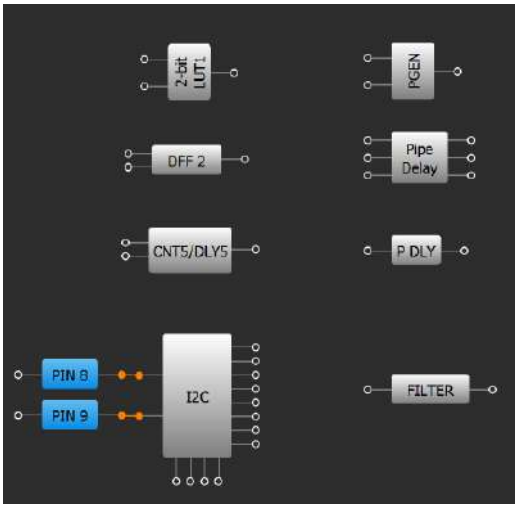

Fig. 4. Digital blocks.

The inputs/outputs in GreenPAK are very flexible. I/O capabilities vary from pin to pin and from part to part, so before choosing a specific GreenPAK you need to match the design with the required pin configuration. The outputs can be configured as push-pull or open-drain in NMOS or PMOS configuration. A scaling factor such as 2x indicates that the output power is doubled. In addition, 10 kΩ, 100 kΩ and 1 MΩ pull-up and pull-down resistor options are available on the output pins.

Several input options are also available, such as: digital input, Schmitt-trigger digital input, low-voltage digital input, and analog input. Analog input is used as ACMP input.

The GreenPAK user interface is shown in Fig. 5.

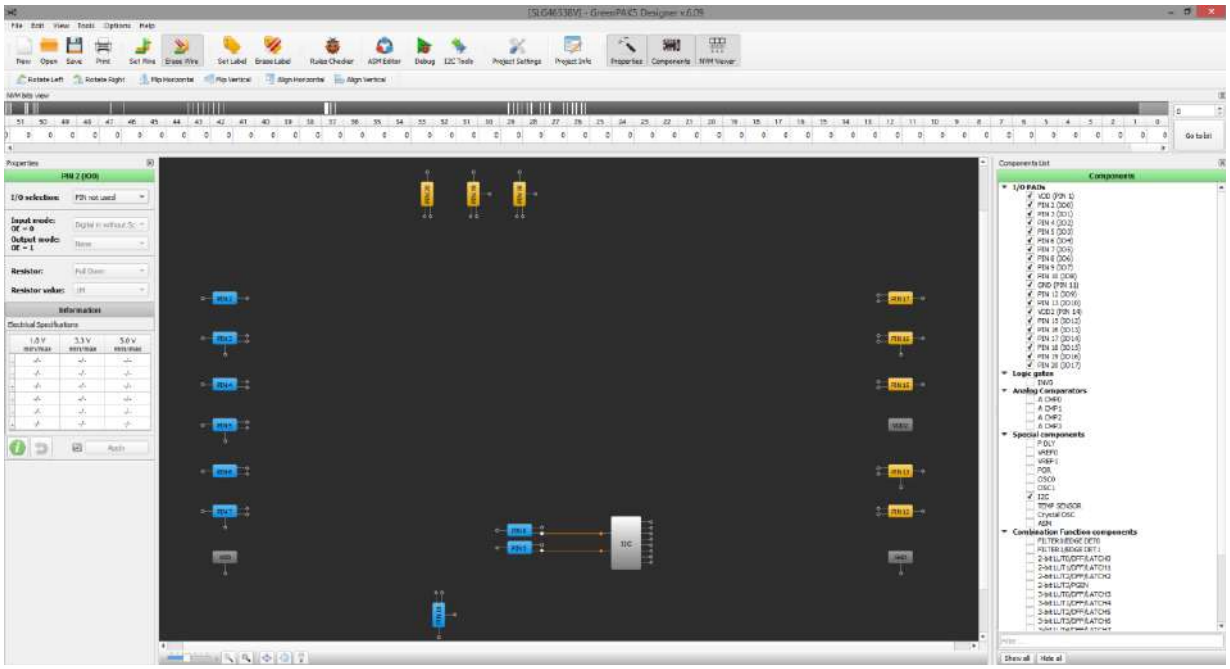

Fig. 5. User Interface in GreenPAK Designer.

The given description of GreenPAK Dialog Semiconductor, GreenPAK Designer and GreenPAK Development Kit demonstrates the full capabilities of the existing at the MTS department laboratory workshop on the educational component "Design of devices on microcontrollers and programmable logic integrated circuits" module "FPGA" [1]. And it will also allow to implement new laboratory work and conduct the work of student groups. GreenPAK Designer will allow students to study fully in remote mode with the support of remote laboratories of the MTS department [6-8].

CONCLUSIONS

The use by institutions of higher education in the educational process of higher technical education of modern material and technical, informational, methodical support with an appropriate level of training of scientific and pedagogical workers and educational and support staff allows to ensure the training of a highly qualified specialist in demand on the labor market. Fulfillment of such requirements is possible only with the consolidated cooperation of leading industry enterprises and companies with institutions of higher education.

Dialog Semiconductor is a leading global manufacturer of highly integrated GreenPAK mixed-signal integrated circuits optimized for personal portable, low-power wireless, LED solid-state lighting and automotive applications. Dialog Semiconductor takes an active part in the support and development of higher education in terms of providing high-quality technical education. The expediency of using GreenPAK Dialog Semiconductor as a laboratory basis for technical educational components is demonstrated on the example of laboratory workshops of the Department of Microprocessor Technologies and Systems of the Kharkiv National University of Radio Electronics.

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Aspects of STEM Education in the Design of Devices on Microcontrollers and FPGAs

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***Abstract*—Nowadays the system of engineering and technical education is facing acute challenges of today. Innovative technologies confidently occupy leading positions in society. But there is still a significant shortage of qualified specialists for STEM fields. The paper considers the introduction of elements of STEM education in the laboratory practice of designing devices on microcontrollers and programmable integrated circuits. The comprehensive approach of STEM education allows in the laboratory practice to expand the horizons and awareness of students in relation to the tasks of work. Also, these developments can be scaled to tangential educational components.**

Keywords—STEM, education, integrated approach, laboratory base, higher education, device design, microcontrollers, FPGA.

I. INTRODUCTION

The system of engineering and technical education requires from institutions of higher education (HEIs) appropriate personnel, material and technical, informational and methodical support. Such education should also take into account promising approaches to the training of specialists based on the implementation of aspects of STEM education. STEM education is crucial because of the demand for IT professionals, programmers, engineers, etc. The professions of the future are related to technological production at the interface with natural sciences. Also, the introduction of elements of STEM education into the educational process will allow students to expand their participation in research projects of university departments, workshops, etc. The educational process should be practice-oriented, motivate students to create their own projects and developments, with the aim of developing critical thinking, creativity, spreading the problem-based approach in education, self-education, education throughout life.

The Department of Microprocessor Technologies and Systems (MTS) of the Kharkiv National University of Radio Electronics (KHNURE) conducts fundamental training of specialists in the field of designing devices on microcontrollers and programmable logic integrated circuits (PLCs) [1-6].

According to the results of the development of educational, methodological and practical materials, the lecturers of the MTS department propose to analyze the prospects of applying a new model of education in the field of science and technology - STEM. The acronym STEM stands for four directions: science, technology, engineering, and mathematics.

Strengthening the role of STEM education is one of the priorities of education modernization, an integral part of the state policy to increase the level of competitiveness of the national economy and the development of human capital, one of the main factors of innovative activity in the field of education that meets the demands of the economy and the needs of society.

STEM education is aimed at the development of the individual through the formation of competences, a natural and scientific picture of the world, worldview positions and life values using an interdisciplinary approach to education based on the practical application of scientific, mathematical, technical and engineering knowledge and skills to solve practical problems for their further use in professional activities.

The use of the leading principle of STEM education - integration, allows to modernize the methodological principles, content, volume of educational material of technical cycle subjects, technology of the learning process and form: skills of solving complicvated (complex) practical problems, critical thinking, creative qualities and cognitive flexibility, organizational and communication skills, the ability to assess problems and make decisions, readiness for a conscious choice and mastery of a future profession, a holistic scientific worldview, technological and engineering competencies, mathematical and natural literacy, research and practical skills, etc. An important role consists in the integrative approach to the implementation of STEM education, where significant attention is paid to consistent, thorough, high-quality teaching of educational components

of mathematical, technical, engineering and scientific direction.

The development of STEM education in educational institutions can be implemented at the following levels [7]:

- primary – stimulation of curiosity and support of interest in learning and the search for knowledge, motivation for independent research, creation of simple devices, constructions, scientific and technical creativity;
- basic – formation of persistent interest in natural and mathematical subjects, mastering of technological literacy and problem solving skills, involvement in research, invention, project activities, which will make it possible to increase the share of those who seek to choose scientific, technical, engineering professions;
- profile - in-depth mastery of the system of knowledge and skills of STEM education using methods of scientific research, implementation of innovative projects;
- higher/professional – formation of specialists in various scientific and technical, engineering professions on the basis of institutions of higher education, as well as improving the professional skills of pedagogical workers in the implementation of new teaching methods, relevant courses and implementation of innovative projects.

II. The Main Part

The MTS department teaches the educational component "Design of devices on microcontrollers and programmable logic integrated circuits", which consists of the following modules: "Modeling of digital signals using MATLAB and VHDL"; "Microcontrollers"; "FPGA" [1-6].

Given that STEM education is focused on interdisciplinary connections and applied nature, all this fits very well into the concept of the educational component "Device Design on Microcontrollers and Programmable Logic Integrated Circuits" [8].

The module "Modeling digital signals using MATLAB and VHDL" aims to: study the mathematical foundations of digital signal processing and master the basic algorithms used for the analysis and synthesis of digital signal filtering devices.

The "Microcontrollers" module aims to: study programming of modern STM32F407VGT microprocessors produced by the ST company in C++ language, in-circuit debugging of microprocessor software. Considerable attention is paid to learning the programming language, working with the IAR Embedded Workbench for ARM and STM32CubeMX software packages, for writing and debugging programs, and the use of these microprocessors in digital devices for transmitting and processing information.

The "FPGA" module aims to: study the architecture and programming of modern programmable logic integrated circuits (FPGAs) of the Artix-7 family manufactured by Xilinx, the VHDL digital device design language and debugging methods and tools using Vivado CAD software; use of FPGAs for the development of digital signal processing devices.

One of the approaches to the implementation of STEM education within the educational component "Designing devices on microcontrollers and programmable logic integrated circuits" can be to replace classic laboratory work with design tasks of various levels of detail for individual or team performance. Such design tasks can be developed within the framework of one module or within the framework of end-to-end design of the entire educational component [9-14].

Examples of such project tasks can be:

- for the module: development of a software product in C, C++ for implementing the Butterworth filter of the 3rd order using MATLAB; development of files to create a bandpass filter with a linear phase-frequency characteristic of the first type for implementation on a crystal when using VHDL using MATLAB; to develop a door opening signaling device in the laboratory on the STM32F407VGT microprocessor; develop a low-pass filter with the specified parameters when using the Nexys 4 DDR Artix-7 FPGA Trainer Board, etc.;
- for the educational component: design of a simple information transfer system between two devices using a wireless interface; design of a door opening notification system; designing a device for encoding/decoding information based on PWM modulation, etc.

One of the examples of the effective implementation of STEM education is the implementation of research projects in the educational component "Designing devices on microcontrollers and programmable logic integrated circuits". Students of higher education, under the guidance of lecturers of the educational component, as part of the acquisition of declared competences, carry out research and cross-cutting projects. These projects are presented for approval and protection at university conferences, forums, seminars, exhibitions, etc. According to the results of research projects, students of higher education under the guidance of lecturers participate in publishing activities [15-17].

Conclusions

The implementation of elements of STEM education within the educational component "Designing devices on microcontrollers and programmable logic integrated circuits" demonstrates the effectiveness of learning the material, interest in the implementation of practical tasks, motivation to study, development of research skills, etc.

This is confirmed by the active participation of higher education students studying at this educational component in competitions, hackathons, exhibitions, conferences and forums, and, in particular, is expressed through publishing activities [15-17].

Successfully mastering the elements of STEM education as part of the educational component allows students of

higher education to acquire the necessary skills for more successful job interviews.

Thus, all of the above demonstrates the effectiveness of introducing elements of STEM education into the educational process.

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