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Design and Synthesis of Multi-Bit Binary Adders on FPGA

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***Abstract*— Fields of application and main classes of multi-bit binary adders (MBAs) are outlined. The well-known structures of cascade, parallel-serial and pyramidal multi-bit adders are analyzed and their system characteristics are determined when classical single-bit components are used. A comparison of the system characteristics of the MBA using the new single-bit components of full and partial adders is carried out. MBA structures were developed using hardware description languages, and their simulation and synthesis on FPGA was performed.**

Keywords—adder, FPGA, algorithm, structure, hardware complexity, time complexity

I. Introduction

Widespread use of algorithms and methods of performing mathematical operations, including arithmetic operations, logical operations and elementary functions, in computer technology and their improvement allows to find new solutions that need implementation and research on modern element base using FPGA [1,2].

Multi-bit binary adders (MBAs) are widely used components of computing devices, matrix and stream multipliers, microcontrollers and specialized processors [3-6].

Functionally and structurally, multi-bit binary adders (MBAs) are divided into the following classes:

- linear (cascade) without structural branches [4,7-13];
- accumulating adders with memory [4,5,12];
- pyramidal multi-bit adders [14-16];
- adders with accelerated transfers [4,6,14,16];
- vertically organized binary adders [3,4].

The priority criteria of MBA efficiency are to ensure minimum hardware (A_S) and structural (k_S) complexity, maximum speed (τ_s), as well as minimum delay of sum bit formation signals (S_i) and end-to-end transfers (C_i). At the same time, it is necessary to take into account the structural complexity of direct, inverse and paraphase inputs/outputs, as well as to minimize the duration of the signal delay between all input/output pairs of the adder.

Important parameters of components of MBAs are functional completeness (F_s) and minimum structural complexity (S_s) [7,8].

Today, there is a wide nomenclature of structures of one-bit partial and full adders [12-14].

At the same time, the possibilities of improving structural solutions and improving of the system characteristics of single-bit and multi-bit adders according to various criteria of complexity and speed have not yet been fully exhausted [15,16].

Thus, designing and researching the system characteristics of MBAs and their single-bit components not only as separate structures, but as functional multi-bit components in FPGA environments and specialized processors is an urgent scientific and applied task.

II. Overview of known MBA structures and their components

Consider the well-known structures of MBA. The structure of an 8-bit MBA of cascade type is shown in Fig. 1.

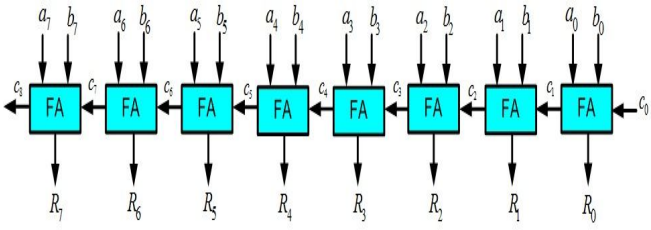

Fig. 1. The structure of an 8-bit MBA of cascade type

The classical structure of the well-known complete one-bit binary adder built on the basis of logic elements AND and "Exclusive OR" is presented in Fig. 2.

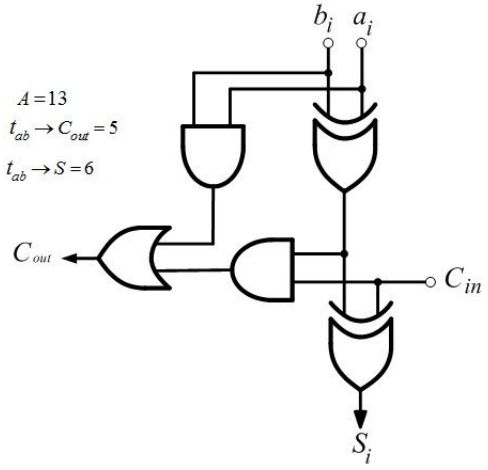

Fig. 2. The structure of a classical full binary adder

In Fig.3 shows the internal structure of the logical element “Exclusive OR”.

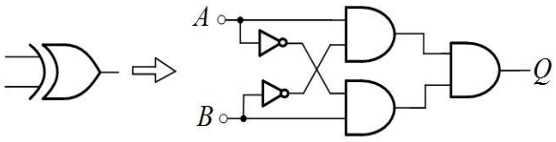

Fig. 3. The internal structure of the logacal element “Exclusive OR”

The logical element “Exclusive OR” contains 5 gates.

When applying known structures of full one-bit adders with hardware complexity $A_{FA}=13$, i.e. logic gates [14], the hardware complexity of such a MBA is calculated according to the expression:

$$A_1 = A_{FA} \times n, \quad (1)$$

where n is its bit rate.

For example, when $n=64$: $A_1 = 13 \times 64 = 832$ logic gates.

When using known structures of full one-bit adders with a time complexity $t_{FA}=6$, i.e. microclocks [14], the speed of cascade-type MBA is calculated according to the expression:

$$t_1 = t_{FA} \times n, \quad (2)$$

where $t_{FA}=6$ microtacts.

For example, when n=64: $t_1 = 6 \times 64 = 384$ microtacts.

The disadvantage of the cascade-type MBA is the low speed, which is due to the sequential formation of bits of end-to-end transfers in each component of the MBA.

The classical structure of the well-known incomplete one-bit binary adder built on the basis of logic elements AND and "Exclusive OR" is presented in Fig. 4.

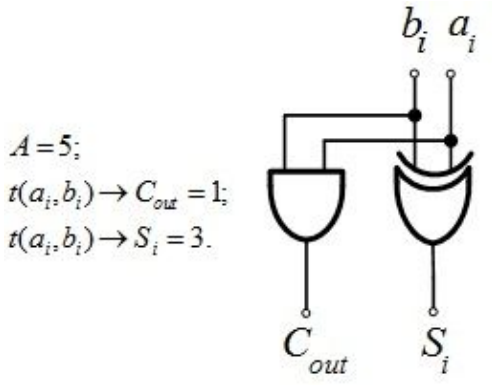

Fig. 4. The structure of a classical incomplete binary adder

Fig. 5 shows the structure of an 8-bit parallel-serial binary adder.

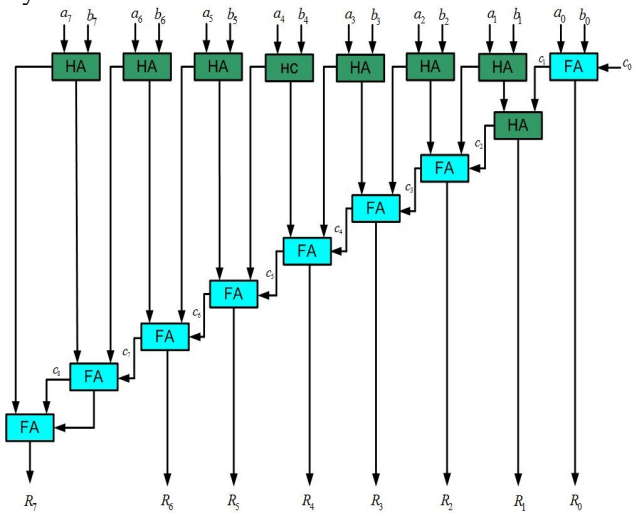

Fig. 5. The structure of the 8-bit MBA of the parallel-serial type

The hardware complexity of such a MBA built on classical components is calculated according to the expression:

$$A_2 = (A_{HA} + A_{FA}) \times n, \quad (3)$$

where n is its bit rate.

When $n=64$: $A_2 = 64 \times (5+13) = 1152$ logic gates.

The speed of the MBA of the parallel-serial type is calculated according to the expression:

$$t_2 = 2t_{HA} + t_{FA} \times (n-1), \quad (4)$$

where $t_{FA}=6$ microtacts, $t_{HA}=3$ microtacts.

When $n=64$: $t_2 = 2 \times 3 + 6 \times (64-1) = 384$ microtacts.

The disadvantage of parallel-serial type MBA is high hardware complexity and low speed.

Fig. 6 shows the structure of an 8-bit MBA of the pyramidal type built on incomplete binary adders.

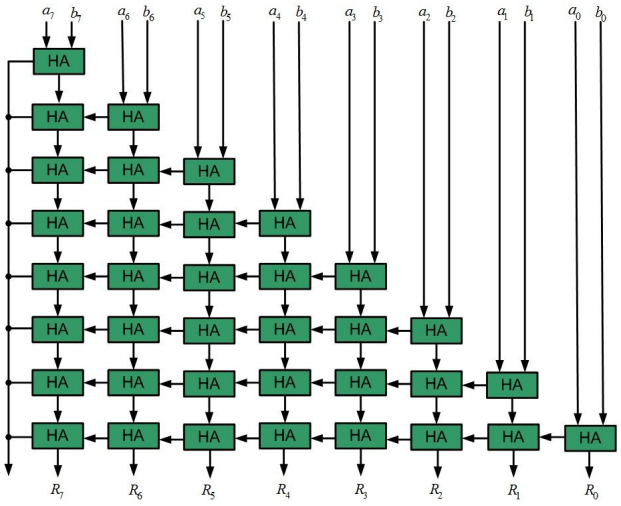

Fig. 6. The structure of the 8-bit MBA of the pyramidal type

The hardware complexity of such MBA built on classical components is calculated according to the expression:

$$A_3 = A_{HA} \times \frac{n^2 + n}{2}, \qquad (5)$$

where n is its bit rate.

When $n = 64$: $A_3 = 5 \times (4096 + 64) / 2 = 10400$ logic gates.

The speed of the pyramidal type MBA is calculated according to the expression:

$$t_3 = n. \qquad (7)$$

When $n = 64$: $t_3 = 64$ microtacts.

The disadvantage of the pyramid-type MBA is the high hardware complexity. However, compared to other types of MBA, it has the best speed.

Fig. 7 shows the structure of an improved one-bit incomplete binary adder, which is described in [17].

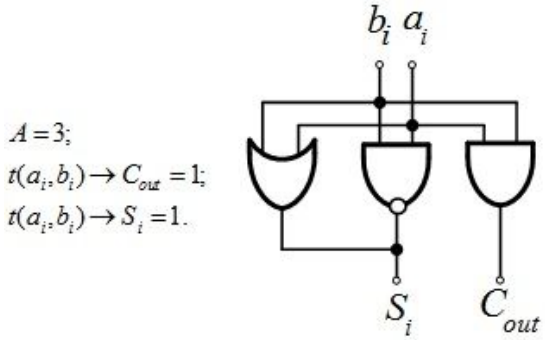

Fig. 7. Structure of an improved incomplete binary adder

When applying such structure of an improved incomplete binary adder in a pyramidal-type MBA, we will get a 1.7-fold reduction in hardware complexity and a 3-fold increase in the speed of forming the sum bit.

The hardware complexity of such MBA built on an improved incomplete one-bit binary adder ($n = 64$) will be equal to $A_4 = 3 \times (4096 + 64) / 2 = 6240$ logic gates, and the time complexity of $t_4 = 64 \times 1 = 64$ microtacts.

Fig. 8 shows the structure of the improved full binary adder, which is described in [18].

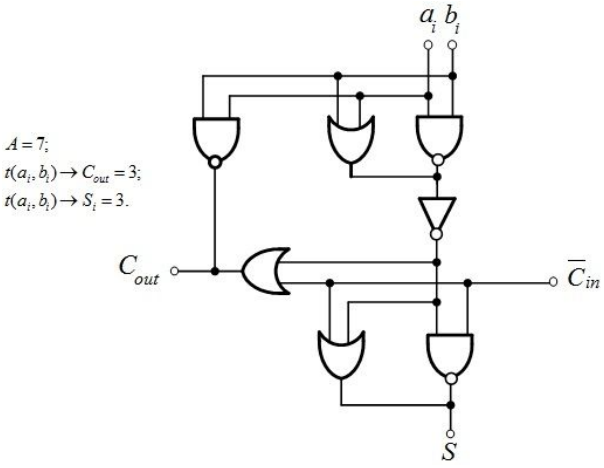

Fig. 8. Structure of an improved full binary adder

When applying such structure of an improved full binary adder in a linear (cascade) type MBA, we will get a 1.8-fold reduction in hardware complexity and a 1.7-fold increase in the speed of forming a through-carry bit and a 2-fold sum bit.

The hardware complexity of such MBA built on an improved full one-bit binary adder ($n = 64$) will be equal to $A_5 = 7 \times 64 = 448$ logic gates, and the time complexity of $t_5 = 3 \times 64 = 172$ microtacts.

When applying the structures of the improved incomplete and complete binary adders in the parallel-serial type MBA, we will get a 1.8-fold decrease in hardware complexity and a 2-fold increase in the speed of forming the sum bit.

The hardware complexity of such MBA built on improved components of incomplete and complete one-bit binary adders ($n = 64$) will be equal to $A_6 = 64 \times (3 + 7) = 640$ logic gates, and the time complexity of $t_6 = 2 \times 1 + 3 \times (64 - 1) = 191$ microtacts.

III. Modeling and Synthesis of MBAs on FPGA

The development of the MBAs of the investigated types was carried out using the hardware description language VHDL in the integrated Active HDL SE environment.

The functional simulation diagram of a 64-bit adder of the pyramidal type is shown in Fig. 9.

The diagram shows the supply of the input 64-bit binary integer values at inputs A and B. 64-bit results of addition are formed at output Q.

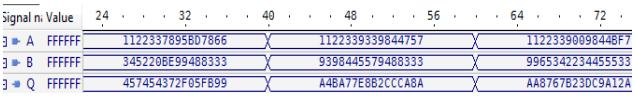

Fig. 9. Functional diagram of the 64-bit MBA of the pyramidal type

The synthesis of the studied class of MBAs was carried out on the FPGA of the Artix-7 family, crystal XC7a100Tcsg324-1 of the Xilinx company [2,11].

The section of the FPGA crystal in an enlarged view, on which the structure of the 64-bit multi-bit adder of the pyramid type was implemented in Vivado Design Suite CAD, is shown in Fig. 10.

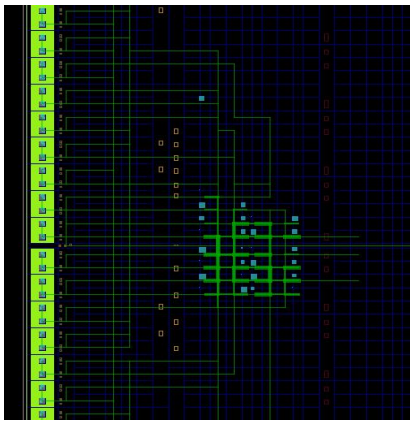

Fig. 9. Implementation of a 64-bit pyramid-type MBA on a FPGA crystal in Vivado CAD

As a result of the synthesis and implementation of the pyramid-type MBA on the specified FPGA crystal, its implementation requires 1237 LUT from the available 63400 ones on the chip, 132 (1%) triggers from the available 126800 ones and has 192 (84%) inputs and outputs from the available 210 ones on the FPGA. The clock frequency of the pyramid-type MBA is 243 MHz.

Table 1 presents the results of MBA synthesis of the studied types on Artix-7 FPGAs using classic and improved components of one-bit full and partial adders.

TABLE I. THE RESULTS OF MBA SYNTHESIS ON FPGAS

№	MBA type	Classic		Improved	
		Number LUT	*F, MHz*	*Number LUT*	*F, MHz*
1	Cascade	64	98	40	163
2	Series-parallel	89	95	56	181
3	Pyramidal	800	125	495	237

From the above results, we can see that the largest number of LUTs must be spent on the implementation of the pyramidal-type MBA. However, its speed is the highest among the investigated types of adders. Serial-parallel and cascade MBAs have the optimal ratio between hardware and time complexity. They have practically the same speed of operation, but lower hardware costs are required for the implementation of the cascade-type MBA.

It was possible to reduce the number of equipment by approximately 1.8 times and increase the speed of the studied class of MBAs by 2 times with the use of improved components of full and incomplete one-bit adders.

IV. CONCLUSIONS

The work describes the main areas of application of multi-bit binary adders, which are components of arithmetic and logic devices of processors. The well-known MBA structures of various types were analyzed and their hardware and time complexity was calculated on the well-known classical element base. The improved components of complete and incomplete one-bit binary adders are described, and improved system characteristics are obtained when they are used in MBA structures. The design and modeling of 64-bit binary adders using the VHDL hardware description language was performed. During the synthesis of the studied class of MBA on FPGA in Vivado CAD, practical results of equipment costs and speed of operation were obtained, which coincide with theoretical calculations.

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