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There proceedings depict: mathematical modeling of information signals and systems; hardware description languages; systems of computer aided design of devices on microcontrollers, microprocessors and FPGAs; features of device development on microcontrollers and microprocessors; aspects of the development of devices in the FPGA; architecture and microarchitecture of specialized computing systems; modern trends in the design of microprocessor technology; the problem of improving the quality of training specialists.

Papers are presented in authors' edition.

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Study of the Effectiveness of Using Nextion Displays in Projects Based on STM32 Microcontrollers

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***Abstract*—An analysis of the problems of developing graphic screens with an original design for STM32 microcontrollers without a built-in graphics accelerator was carried out. The analysis of the electronics development companies requirements for projects with built-in visualization in electronic devices has been carried out. A comparative analysis of the Nextion displays characteristics and industrial operator panels was carried out. The capabilities of Nextion displays were studied: the speed of loading images from flash memory and displaying these images on the screen, the time it took to develop screens, the speed of data exchange between the display and the microcontroller. A comparative analysis was carried out between identical projects created for the Nextion display in the Nextion Editor environment and a display for which there is no specialized GUI development environment. The effectiveness of using Nextion displays for high-quality visualization of the device state and systems designed on the STM32 microcontrollers has been proven.**

Keywords—display, microcontroller, widget, Nextion, STM32, interface UART.

I. INTRODUCTION

In many modern electronic devices and systems of multimedia, industrial, household, etc. applications use touch displays. They allow to display a device or system status in real-time and allow the user to control processes or configure device or system parameters [1, 2]. To compete in the modern electronics market, a number of requirements are imposed on new electronic devices [3]. The time to write code for the controller and display should be kept to a minimum. When changing programmers, new developers should quickly get to grips with the existing code and continue developing or maintaining it. All this requires the use of universal programming environments and standard approaches. Modern displays are divided into two groups: with and without an integrated controller [1, 4]. The presence of a built-in controller allows you to use any microcontroller to control the display. However, the exchange rate is limited by the speed of the controller built into the display, the capabilities of its software and the data transfer interface. The usage of displays without an integrated controller requires the use of microcontrollers with an integrated graphics accelerator. Among microcontrollers of the STM32 family, only the high performance F7, H7, L4 series have a built-in graphics accelerator [1]. For such series, there is a specialized software product Touc5GFX [4], using which, in a short time and at a high design level, you can create a set of graphic screens for visualization and control, and even provide video streaming. However, in the cheaper and more popular in practice series F0, F1, F2, F3, G0, L0, part of the F4, etc., is missing a graphics accelerator. In this case, the creation of beautiful and functional graphic screens requires the usage of third-party software environments, and the import of graphics into the microcontroller project requires significant time resources, which unacceptably increases the development time. Such solutions also require specific knowledge, which complicates the creation of a programmers team in large projects.

Since 2014, Nextion company has been producing 4 series of resistive and capacitive displays with screen sizes from 2.4' to 10'. The clock frequency of the controller built into the display is in the range from 48 to 200 MHz. Displays have built-in flash memory from 4 to 128 MB, built-in RAM from 3.5 to 512 kB, non-volatile memory up to 1 kB. The UART interface is used to communicate with the display. The main advantage of these displays is the intuitively simple environment for their configuration and programming - Nextion Editor. The displays are not designed to receive streaming video from the camera, but they successfully solve all other tasks of high-quality visualization and control [6, 7]. On the manufacturer's website and other resources, you can find many examples of interaction with Arduino devices [7], but there are no results from a study of performance when implementing animation and implementing complex graphic screens [6-9]. In [10-14] questions and examples of work that can be useful for studying the specified question are considered.

Therefore, the purpose of research and analysis was to evaluate the effectiveness of the Nextion displays usage when working together with STM32 microcontrollers.

II. Development of Graphic Displays and Data Exchange With STM32

The Nextion Editor environment has a built-in set of standard graphic widgets: screens, buttons, pictures, input fields, sliders, etc. For each widget, the user has access to settings: labels on widgets, their sizes, positions, colors, etc. However, it's not possible to change the design of the widget. For example, you can't make a standard button oval, round the edges, create a color gradient within the button, etc. It is only rectangular with a solid color fill. The solution to this problem is to overlay the graphic on the button widget. In this case, the creation of the image is carried out by the designer. In the same way, the problem associated with the limited number of widget types is solved. So, using pictures, you can create very complex scales, multi-position switches and other elements corresponding to electronic devices. However, each of the images that is superimposed on the widget must be read from the controller's flash memory and displayed. The display manufacturer does not provide information about the screen refresh rate. Therefore, it is necessary to conduct a study - what is the speed of the transfer images between flash memory to display and what is the relationship between the transfer and visualization time and the number of output files.

An equally important issue for developers of display screens is the required amount of RAM and flash memory to create one screen with original design. For each widget, at least one picture must be stored in flash memory. Although the number of pictures can be much larger. For example, for a button, it is necessary to save the images of the unpressed and pressed button. Information widgets that display errors or actuator states can have up to 10 or more graphical icons corresponding to their states. RAM stores information about the position of widgets, their sizes, available to change properties.

In addition to widgets, you can create variables in the Nextion Editor environment. The environment only supports 2 data types: 32-bit integers and string variables. This constraint requires all other microcontroller data types to be converted to screen data types before those values are sent to the screen. So, for example, float variables can be converted to text values. The UART interface is used to transfer data between the microcontroller and the screen. The transmission rate is adjustable from 2400bps to 921600bps. When display transmits data to the microcontroller, it is possible to form an arbitrary package structure or a structure that corresponds to the the Nextion display operating system. An arbitrary structure makes it possible to combine the values of a variables group into one package and reduce the data transfer time. When a structure corresponding to the Nextion environment is used, the value of each variable is passed as a separate package. Each byte of this packet is an ASCII character code. The package structure looks like

$$\text{Variable\_name.val} = \text{Value\_of\_variable 0xFF 0xFF 0xFF},$$

where val - shows access to the value of the variable; 0xff,0xff,0xff - three bytes that indicate the end of the packet.

When such a packet structure is used, the data transfer rate is determined by the expression

$$R_{inf} = \frac{N_{infinf\ char}}{N_{name\ var}+N_{infinf\ char}+7} \cdot 0.8 \cdot R_{interface},$$

where R_{inf} - is the rate of useful information transmission (values of variables), bit/s; $R_{interface}$ - UART interface data transfer rate, bps; $N_{infinf\ char}$ - the number of characters in the variable name; 7 - the number of bytes, which consists of the packet end and the group of characters '.val'. If we use variables with a name length of 2 characters, then the simplified formula for determining the information transfer rate is

$$R_{inf} \approx 0.286 \cdot R_{interface},$$

With a maximum screen baud rate of 921600 bps, up to 8200 variable values can be transferred in one second. In operator panels from companies such as Siemens, GE Fanuc, etc., when displaying the status of an automation system on the screen, the average number of variable values per screen is up to 100-150. The default value of the data update period on the screen is 1s. Less commonly, this value is set to 0.5s. Thus, the amount of data that can be transferred between the controller and the screen is sufficient to update the information on the display in a timely manner.

When values of string variables are passed, the frame format that is used in the operating environment of the display

$$\text{Variable}_{\text{name}}\text{.val} = \text{“Value}_{\text{of}_{\text{variable}}}\text{” 0xFF 0xFF 0xFF}.$$

The rate of useful information transmission is determined by the expression

$$R_{inf} = \frac{N_{infinf\ char}}{N_{name\ var}+N_{infinf\ char}+9} \cdot 0.8 \cdot R_{interface},$$

where $N_{infinf\ char}$ - is the number of characters in the string variable.

The transfer of variable values from the microcontroller to the display is carried out only in the format corresponding to the Nextion displays.

III. Development of ALGORITHMS and Research Results

The NX4832K035 display was chosen for research (Fig. 1).

Fig. 1. The appearance of the Nextion display.

The frequency of its built-in controller is 108MHz, the amount of flash memory is 32MB, the amount of RAM is 8kbytes, the screen resolution is 480x320, the amount of EEPROM memory is 1kbytes. The STM32F407 microcontroller was chosen to connect with the display. When studying the efficiency of information transfer between the display and the STM32 microcontroller, its UART interface was configured to transfer data at speeds of 460800 and 921600 bps. An array from 70 packets was formed in the microcontroller memory, which corresponded to 70 values of 32-bit internal display variables. In this case, the length of the array was 1050 bytes, and the transmission time was 10ms. Such a period for updating the values of variables made it possible to implement a check for missing received data in the interrupt handler from the timer in the display. To create a continuous stream of transmitted data, the array was transmitted in a cyclic mode using a DMA channel [9]. In each transmission cycle, the value of each variable was increased by 1. This made it possible, when processing the received information on the display, to detect a gap in the received value. The research results are presented in table 1.

TABLE I. PROBABILITY OF MISSING DATA DEPENDING ON THE TRANSMISSION RATE

Data transfer rate, bps	Probability of missing variable value
460800	0
921600	0.001

An unshielded cable 10 m long was used to connect the microcontroller and the display. As can be seen from Table 1, there are no gaps at speeds up to 460 kbps. At 921600 bps, no more than 1 pass per 960 packets is possible. Such gaps can be explained by the limited speed of the display processor, since the STM32F407 microcontroller operates in DMA mode. When a skip occurs, no errors occur inside the display, and work continues normally.

To estimate the refresh rate of graphic images on the screen, the following algorithm was developed:

1) The screen is loaded with an image resolution equal to the screen resolution.

2) A timer has been added to the project, and in the timer interrupt handler, the image is read and displayed on the screen.

3) The interval of the timer every 2s decreased by 1ms and a check was made - whether the display had time to display the image completely.

4) Test steps 1-3 were repeated for the case where 10 images are displayed. Each of the images has an area equal to 1/10 of the screen area.

In the screen refresh rate study, high-speed screen capture was performed at a frame rate of 120 fps. Further analysis of artifacts in the image made it possible to estimate the limiting value of the update rate without artifacts.

The results of the update time estimation are presented in the form of Table 2.

TABLE II. SCREEN REFRESH TIME

Number of images	Image size, pixels	Loading and display time, ms
1	480x320	324
10	48x320	352

Analysis of the data in Table 2 shows that the speed of updating images in the design of the screen meets the requirements of automated control systems.

To analyze the requirements for the amount of RAM and flash memory, a project was developed. It contained 7 screens of varying complexity. The simplest screen is the settings selection menu and contains only 3 widgets that allow you to go to the corresponding settings screens. The appearance of the simplest screen is presented in Fig. 2.

Fig. 2. The appearance of the simplest screen.

The most complex screen contained 12 widgets and 32 images corresponding to the states of these widgets. Most widgets had 4 images corresponding to their states. The project had multilingual support for up to 10 languages. The captions over the images were superimposed in accordance with the current interface language. The rest of the screens were marginally simpler than the main screen. Table 3 shows the data on the development time of the screens and the results of their compilation.

TABLE III. RESULTS OF DESIGN TIME AND COMPILATION OF PROJECT SCREENS

N screen	Flash memory size, kb	RAM size, bytes	Number of images	Number of widgets
1	71	400	1	2
2	106.6	712	26	15
3	32	508	29	12
4	46	680	10	7
5	16	608	4	8
6	28	756	8	14
7	30	672	6	6

The analysis of the data obtained shows that for storing images of one screen, the average value of the flash memory amount is 47 kbytes, and 612 bytes of RAM. Then the resources of the selected screen model are enough to create 13 full-fledged screens with design. Based on the characteristics of Nextion displays, the maximum number of screens is much more limited by the amount of RAM than flash memory.

This project is an updated and improved version of a previously developed project based on the demo board Makerbase MKS TFT35. Comparison of the screens

development time on Nextion and Makerbase MKS TFT35, shows that without the usage of development environments for graphic screens that are compatible with displays, it takes 5-6 times more time to create one screen and animate it.

IV. Conclusions

Nextion displays are great to visualize the status and control electronic devices in addition to displaying images from a video camera. In combination with STM32 microcontrollers that don't have an integrated graphics accelerator, they are an excellent low-cost solution. To obtain a high-quality screen design, you should use the original widget images loaded from flash memory. The time of loading images and displaying them on the screen does not exceed 352ms, which corresponds to the visualization standards for automated process control systems (APCS) operator panels. At UART speeds up to 460kbps, the display can process a continuous stream of packets with variable values. At a speed of 921600bps, the probability of missing a value does not exceed 10-3. At the maximum exchange rate, up to 8200 values of 32-bit variables can be transferred per second. This value is sufficient to visualize a system or control device of any complexity. In the operator panels of APCS, up to 100-150 variable values are displayed on one screen. It takes 1-2 days to learn the Nextion Editor environment. It takes 4-5 days to create one screen and related scripts, which is 5-6 times less than without using the interface development environment. The cost of Nextion displays is 5-8 times less compared to operator panels for process control systems from Siemens.

Thus, Nextion displays fully satisfy the requirements for visualization that are imposed on the development of new electronic devices by developers: development of visualization projects with original graphic design in a short time, quick acquaintance with the project when changing the programmer-developer.

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Digital Twin of the Educational Equipment "Sorting Station"

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***Abstract*—This work describes the solution to the problem of creating a digital twin of the educational equipment "Sorting Station" from the FESTO company. A structural diagram of the software was developed. The principle of interaction of the digital twin of the educational equipment with the real world has been developed. The scheme of interaction of the developed digital twin with real means of automation is built. Algorithms for the operation of the digital twin have been developed. In order to check the operability of the developed program, the problem of remote monitoring of the state of the main nodes of the conveyor was solved using the Codesys technological software development environment.**

Keywords—PLC, FESTO, modbus, digital twins, program, control module, protocol, conveyor.

I. Introduction

A digital twin of an object is a means of accessing information about the life cycle and a single interface to it. Digital twins can be created for any entity of interest to the enterprise. All the listed technologies are approaches to the implementation of the concept of the Fourth Industrial Revolution (Industry 4.0). If for the traditional industry the acquisition of the necessary characteristics of the product is carried out through numerous field tests, then the task of Industry 4.0 is to conduct multiple tests with the help of a digital twin, and to pass the field tests the first time.

The digital twin of the product includes:

– geometric and structural model of the object;

– a set of calculation data of parts, assemblies and products in general;

– mathematical models that describe all physical processes occurring in the product;

– information about technological processes of manufacturing and assembly of individual elements and the product as a whole;

– product life cycle management system.

A digital twin is used at all stages of a product's life cycle, including design, production, operation and disposal.

In this work, a digital twin of the laboratory model from the FESTO company is developed, which is intended for training students and specialists in the field of production automation. It allows you to reproduce the process of automatic sorting of parts, which allows you to ensure the efficient and accurate operation of the production process.

II. Analysis of the Functional Possibilities of the Educational Equipment "Sorting Station"

The educational model "Sorting Station" from the FESTO company is intended for training students and specialists in the field of production automation. It allows you to reproduce the process of automatic sorting of parts, which allows you to ensure the efficient and accurate operation of the production process (Fig. 1) [1].

Fig. 1. Appearance of the mechatronic module "Sorting Station".

The module simulates the section of the production line where the metal and plastic parts supplied from the store are sorted. Parts are fed to the conveyor line using a vacuum translator.

The sorting station distributes the workpieces in three directions depending on the properties of the material or other specified conditions specified when programming the controller.

The training model consists of a set of pneumatic mechatronic executive devices fixed on a stationary base: a conveyor belt, pneumatic distributors, ramps, a set of sensors for detecting parts in different directions.

With the help of pneumatic distributors, actuated by short-stroke cylinders with the help of a direction change mechanism, the workpieces are sorted into the appropriate slopes.

At the entrance to the conveyor, for example, an inductive sensor is installed to determine the type of material.

Under the influence of distributors, the parts are directed to certain slopes. An optical sensor with a reflector is installed on each slope. Sensors monitor the filling level of slopes.

An industrial controller controls the educational equipment. Depending on the program embedded in it, it is possible to perform various tasks related to the study of pneumatic and mechatronic devices.

III. Development of the Principle of Interaction of the Digital Twin of the "Sorting Station" Model with the Real World

A digital twin must have one or more communication channels to interact with the real world [2, 3]. These channels are used to read information using sensors and execute commands from the control device.

Fig. 2 shows the interaction diagram of the developed digital twin with real automation tools.

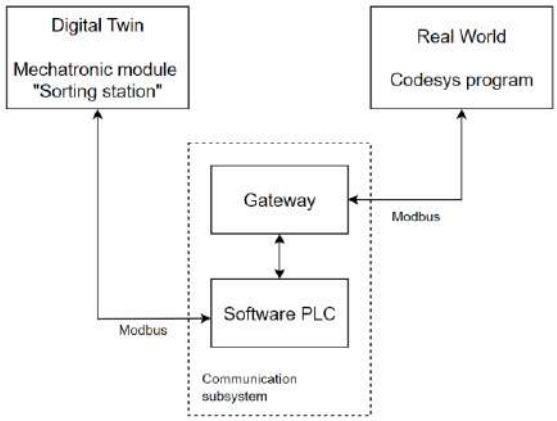

Fig. 2. The interaction scheme of the developed digital twin with real means of automation.

The virtual educational equipment "Mechatronic module "Sorting Station"" produces signals from virtual sensors depending on the location of parts on the conveyor line and the position of executive devices.

The Codesys program receives this data through its own Software PLC tool, processes it and, based on the algorithm embedded in the work of the technological program, controls the operation of executive devices.

Thus, the interaction of the digital twin with the real world takes place thanks to the Modbus industrial protocol. With its help, data packets with information about the state of the sensors are obtained, according to the design of the real educational equipment: a sensor for the presence of parts at the entrance to the conveyor line, sensors for filling storage units in all directions of sorting.

Also, with the help of the Modbus protocol, commands are received for controlling virtual means of automation: the conveyor motor, the distributors of the parts flow and the status indicators of the educational equipment.

Auxiliary software components are used to combine the two main components of the system: PLC server, Gateway to the virtual device.

Fig. 3 shows the constructed structure of the software that implements the functions of the digital twin of the educational equipment "Mechatronic module "Sorting Station"".

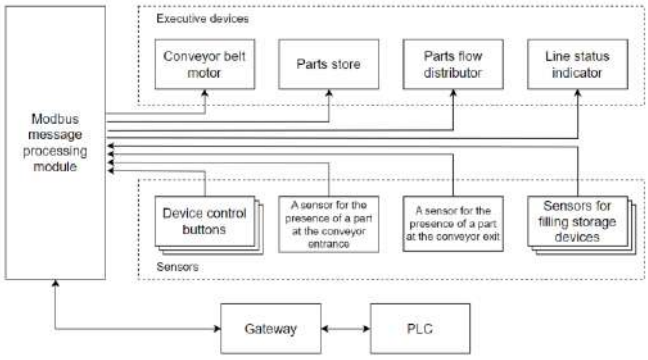

Fig. 3. The software structure that implements the functions of the digital twin of the educational equipment "Mechatronic module "Sorting Station".

The software consists of:

– message processing module using the Modbus protocol;

– a set of virtual modules that implement the functions of executive devices;

– a set of virtual modules implementing sensor functions.

The set of virtual modules that implement the functions of executive devices includes software emulators of the following devices:

– conveyor belt engine;

– the stock of the parts store, which feeds the conveyor line;

– parts flow distributor;

– line status indicator.

The set of virtual modules implementing sensor functions includes software emulators of the following devices:

– device control buttons;

– a sensor for the presence of a part at the entrance of the conveyor belt;

– a sensor for the presence of a part at the exit of the conveyor belt;

– sensors for filling storage devices.

IV. Work Algorithm Development of the Digital Twins

Let's consider the principle of operation of the decision-making subsystem, which forms the basis of the operation of the digital twin of the educational equipment "Sorting Station". Thanks to the developed algorithm, the virtual model behaves like a real device, reacting to external influences through the controls of the graphical interface and through the network communication channel using the Modbus industrial protocol.

Fig. 4, a shows the algorithm for processing messages through the Modbus protocol and controlling executive devices.

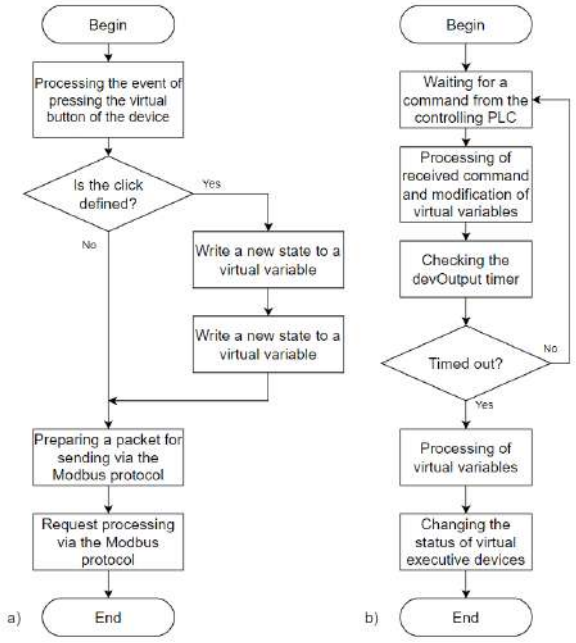

Fig. 4. Algorithm for processing messages via the Modbus protocol and controlling executive devices (a) and the algorithm for surveying sensors and generating messages via the Modbus protocol (b).

The message processing module receives packets in the Modbus protocol format in automatic mode and stores information in the corresponding registers specified in the message.

The system timer is configured for a certain period of time. When it ends, the received data is processed. Depending on the received information, internal variables are modified. Each variable is assigned to a specific Modbus register address.

In all registers, the active level is a logical unit. Thus, the appearance of a logical unit leads to the activation of the corresponding executive device

Fig. 4, b shows the algorithm of polling sensors and generating messages via the Modbus protocol.

The activation of any sensor leads to the formation of a logical unit signal at the output of the corresponding contact.

The educational equipment uses an 8-bit ADC, given that the input registers are 16-bit, the most significant byte in the response will always be zero.

The conveyor is started by writing a logical unit to the variable "YC_Moto". In this case, the canvas of the conveyor line begins to move, which is visually displayed on the PC screen.

Parts are issued by short-term recording of a logical unit in the "YC_Stor1" variable. The holding time of the high level signal must be at least 0.5 s and not more than 2.5 s.

Parts can be issued automatically. To do this, you need to select the "Auto" mode in the drop-down list, which is located above the "YC_Stor1" variable. In this case, external control signals are ignored.

At the end of the conveyor line there is a parts receiver. The parts that were not redirected during the movement of the line fall into this receiver and are stored there until the moment the "Reset" button is pressed.

The number of parts in the magazine and in the final receiver is displayed as a number on the background of the part in the corresponding device. For example, the number "5" located on the red part corresponds to their initial number in the store.

In the process of moving parts along the conveyor line, their direction of movement can be changed using two levers "YC_Sp1" and "YC_Sp2". Levers are controlled by writing a logical unit to the corresponding variable. The activated lever visually blocks the direction of movement of the parts and forces it to move into one of the two parts store "YC_MSt1" and "YC_ MSt2".

The number of parts in the parts store is displayed as a number against the background of the last received production unit.

With the help of requests in the format of the Modbus protocol, you can find out about the number of parts in the store and in all parts store. The corresponding value is written to the storage registers.

V. Program for Controlling the Digital Twin of the Educational Equipment "Sorting Station"

Fig. 5 shows the external view of the user interface of the virtual device "Conveyor and technological line". A feature of the implementation of this device is the combination of a conveyor line with a module for feeding parts of the conveyor line into a single production module.

The software implementation of the digital twin allows you to perform the following functions: issuing parts for feeding the conveyor line; moving them along a conveyor line; if necessary, the distribution of the flow of parts depending on the characteristics of the parts, or according to another principle; control of the mode of operation of the device using an additional block of buttons; visualization of the current state of all device elements.

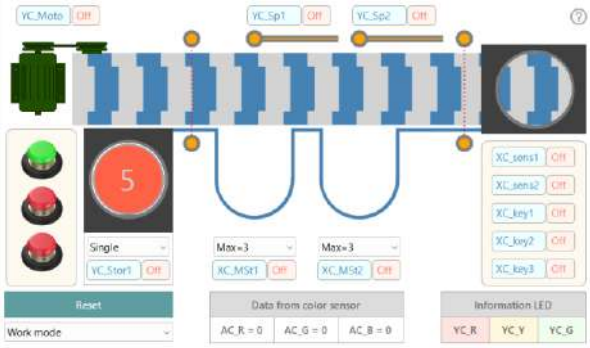

Fig. 5. Appearance of the user interface of the virtual device "Conveyor and technological line".

To check the functionality of the developed model, we will consider the task of remote monitoring of the state of the main nodes of the conveyor using the Codesys technological software development environment.

It is necessary to monitor the following parameters:

– the condition of the motor that moves the conveyor belt;

– the position of the flow distributor;

– the number of parts remaining in the store feeding the conveyor line;

– the number of parts in the first parts store; the number of parts in the second parts store;

– the number of parts in the final parts store.

In fig. 6 red shows the channels for controlling the device, and in fig. 7 in green – channels for monitoring the state of the conveyor line [4].

Fig. 6. Channels for device control.

Fig. 7. Channels for monitoring the state of the conveyor line.

For the program to function, we created a set of variables used to receive or transmit data using the Modbus protocol.

With the help of visual components, we will develop the graphical interface of the operator's panel (Fig. 8).

Fig. 8. Graphical interface of the operator panel.

Fig. 9 shows an example of a program interface and a virtual device in the process of executing a technological program.

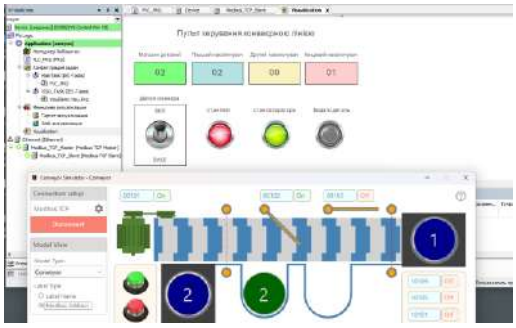

Fig. 9. An example of a program interface and a virtual device in the process of executing a technological program.

From the figure, you can see that the executive mechanisms of the educational equipment correspond to the position of the control bodies on the operator panel. Information panels display the remaining parts in the store.

VI. Conclusions

This work describes the solution to the problem of creating a digital twin of the educational equipment from the FESTO company "Mechatronic module "Sorting Station"".

The structural diagram of the software tool and the principle of interaction of the digital twin of the educational equipment "Sorting Station" with the real world are described. The scheme of interaction of the developed digital twin with real means of automation is built. Algorithms for the operation of the digital twin have been developed.

A program for controlling a digital duplicate of a educational equipment has been developed. The software implementation of the digital twin allows you to perform the following functions:

– issuing parts for feeding the conveyor line;

– moving them along a conveyor line;

– if necessary, the distribution of the flow of parts depending on the characteristics of the parts, or according to another principle;

– control of the mode of operation of the device using an additional block of buttons;

– visualization of the current state of all device elements.

In order to check the operability of the developed digital twins, the problem of remote monitoring of the state of the main nodes of the conveyor was solved using the Codesys technological program development environment.

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Hardware for Providing Smart Farming Technologies

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***Abstract*—Modern agricultural and horticultural technologies have made it possible to obtain higher yields with smaller areas, which supports the ever-growing population. Agriculture is inherently unstable. This is largely due to the influence of external environmental conditions on productivity from year to year. The desire for greater consistency and stability in agriculture prompts the introduction of another type of modern technology in this field.**

Keywords—farming technologies, information systems, LoRa, Wi-Fi, Core Independent Peripheral, wireless components

I. Introduction

Indeed, we may be on the threshold of the Second Green Revolution. Crops are being sewn and fertilized using fancy new tractors with cabs that resemble cockpits, gathering and wirelessly transferring field data collected by myriad sensors that can be used to maximize yields during the growing season while planning next year's crop.

Another element of the Second Green Revolution is addressing the inextricable link between agriculture, energy use and even climate change. While the first Green Revolution provided the template for feeding a hungry world, the next great transformation of agriculture must also address related energy and environmental challenges, as well as what sustainability researchers call "food security" [1].

The Green Revolution taught humankind how to grow more food using less soil. Among the hurdles to ending hunger and improving nutrition are better distribution channels needed to feed humans plagued by poverty and war.

Among the biggest innovations of the last five years has been the introduction of cloud-based platforms that use steadily improving broadband connections to collect and organize field data swept up by sensors.

Modern farming technologies make it possible to significantly increase productivity, which is extremely necessary in the conditions of the constantly growing population of the country. However, agriculture is inherently unstable. First of all, this is due to the influence of external environmental conditions on the yield from year to year. The desire for greater consistency and stability in the agricultural economy prompts the introduction of a new type of modern technology in this field [2].

II. Built-in and Wireless Solutions for Information Complexes

The availability of modern livestock condition monitoring systems has led to improved product quality. Remote systems for monitoring the state of the environment and plants make it possible to monitor the state of the crop with high accuracy. Thanks to modern sensor systems with built-in wireless communication elements, "smart agriculture" will soon have the tools and capabilities needed to increase yields and profitability while providing the level of quality society demands.

Field data collection and analysis has transformed traditional equipment manufacturers into data management information centers for a growing list of software tools. It's a way for farmers to view operations in real-time and get information on how to improve operations, including spending less money to improve yields. The goal is to gain control over all variables related to agriculture by understanding yield data across space and time.

Modern information systems, based on an extensive network of sensors and controllers, can help make the best decisions for producers, allowing them to grow crops and livestock with a higher level of productivity, while reducing the use of water, pesticides and fertilizers. This can help reduce the farm's impact on its natural environment, ensuring a future for posterity.

The main solution for ensuring the efficiency of a modern farm is to provide farmers with information about the state of the production process. Thanks to the innovations of today's embedded and wireless components, this goal can be achieved by implementing large arrays of low-cost sensor networks. Sensors monitor on-site conditions – temperature, acidity, light, humidity, pressure, water level, workflow data, motion detectors, presence, animal physical condition sensors and coordinates – on agricultural plots. This data is then transferred to a centralized database (cloud) via wireless networks such as 4G/5G cellular and LoRa [3].

Data can be accessed in real time on any device connected to the Internet. This allows the manufacturer to access information from anywhere in the world and provides the opportunity to make appropriate adjustments to correct a certain situation.

With an increase in the number of sensors, the area of the automated system increases, the efficiency of control

algorithms increases, and the use of distributed systems becomes more efficient.

The maximum benefit from a distributed system is achieved when the controllers work independently, and the exchange of information between them is minimal.

The distributed system has the following characteristics:

- greater speed, this is achieved due to the use of parallel distribution of tasks between processors;
- the system uses a simplified modernization algorithm;
- resistance to failures;
- increased reliability;
- simpler expansion of reconfigured systems;
- must have a great simplicity of design, layout, configuration, diagnostics and maintenance of the system [4].

Network sensor nodes are not a new concept; but to ensure a certain level of performance and reliability in such a complex space, some key requirements must be met. First, they need a reliable power source, which is a difficult task, since the space of the farm is not limited by meters.

The components must have autonomous power that will work for months or even years without replacing the battery. This requires high energy efficiency, usually achieved by implementing a microcontroller-based system that can perform complex tasks without intensive core usage and minimizes sleep power consumption.

Second, sensor nodes on a smart farm must remain operational in harsh, remote areas and monitor moving objects. Individual components must work in the field for a long period of time and not require hardware maintenance. All software updates must be performed remotely and securely. This requires a reliable remote connection through the WAN infrastructure within the sites and LoRa [5].

Thus, the ideal solution of the system will be the general design of the base node, which can be easily adapted to the needs of a separate farm. To achieve this, the base node must be flexible enough to interact with a wide range of analog and digital sensors.

Another, more complex design challenge concerns the wide variety of engineering disciplines required to implement such a system. Smart farm component developers or engineering teams must have expertise in classical embedded design methods, radio frequency communications including the intricacies of LoRa, Wi-Fi and cellular topologies, and network security. understands cloud infrastructure [6].

Therefore, the beginning of the development of the structure of a smart farming system begins with the search for the most energy-efficient solutions among the component base.

8-bit microcontrollers have been known for 50 years. The latest devices that have appeared recently have received new functions that meet the needs of smart systems. Among the many new features are Core Independent Peripheral devices (CIP) that expand the capabilities of embedded systems. Core Independent Peripherals and integrated analog features are designed to implement a variety of functions and applications that do not need constant interaction with the Central Processing Unit. Because CIPs can enable many simultaneous functions in a single MCU, you can use a smaller and more cost-effective device to implement complex control systems and create innovative designs. These blocks of configurable hardware intelligence require little to no code, consume minimal power and are much smaller than the RAM or Flash needed to implement the same functions in software. CIPs can operate independently of the kernel, allowing developers to configure them to perform routine and repetitive tasks with the lowest power consumption. An additional benefit of CIPs in maintenance-free environments is their ability to increase system reliability. CIPs are actually built into the device structure of the FPGA cell included in the MCU, and are virtually immune to software collisions such as stack overflows or underflows.

To minimize the number of external components, micro controllers have various interfaces for connecting digital sensors, as well as analog converters. It is also necessary to remember the availability of development environments that support a wide range of modern MCUs.

Smart farming technology

Adoption cannot be rushed. In the next few years, the world's population will grow to more than 9 billion. Food production is estimated to increase by 70%, making full adoption of precision agriculture necessary to meet demand. For developers, this means that there is still a lot of potential in the market for agricultural sensor systems. Modern agriculture is experiencing another technological revolution. Access to real-time data on plant and animal health and condition via the global network is changing the way farms are managed, resulting in ever-increasing yields and improved land viability. At the forefront of this revolution is remote control, but its hardware will continue to be based on the familiar 8-bit microcontroller. Modern MCU architectures are becoming key components in bridging the gap between the sensor and the cloud for today's productivity-enhancing product developers [7]. It’s unclear whether a Second Green Revolution will solve our pressing global problems. But it does seem likely that the tools of precision agriculture can help raise living standards around the world. That alone is reason for hope.

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Modeling the Acoustic Channel of Voice Information Leakage

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***Abstract*—The article analyses the modelling of an acoustic channel for voice information leakage. The model consists of 5 parts that are coordinated with each other by mathematical expressions. The results of experimental studies are presented. The proposed model can be used as a basis for software for modelling the acoustic channel of voice information leakage.**

Keywords—modeling, channel, voice, information, leakage

I. Introduction

The method of instrumental control doesn't allow to estimate a priori information security from leakage through the acoustic channel. It may be required for example at the stage of designing of a complex protection system. This possibility can be provided by creating a mathematical model of acoustic information leakage channel.

The model is a consistent set of mathematical expressions that allows calculating the intelligibility of the speech signal at the output of the technical means of intelligence (TMI), depending on a given set of spatial and energy characteristics of the acoustic information leakage channel. It can be decomposed into 5 models: speech signal source (SSS), acoustic interference sources (AIS), propagation environment (PE), TMI, and speech intelligibility assessment (SIA).

II. Mathematical Expression of Models

The formant method, also known as Articulation Index (AI), is used for intelligibility estimation, in which the articulation (formant) intelligibility is the sum of the intelligibility of individual bands into which the spectrum of the speech signal is divided (1).

$$R = \sum_{i=1}^{n} k_i \cdot r_i(Q_i) \tag{1}$$

where i - number of frequency bands, n - their number, k_i - probability coefficients of formants presence in bands, $r_i(Q_i)$ - coefficient of formants perception, depending on signal/noise level, corrected for energy redundancy of speech spectrum $Q_i = q_i - \Delta A_i$. Syllabic and verbal intelligibility are related to formant by known relationships.

Thus, the input data for the model is an array of signal to noise ratios to be derived from the TMI model output.

The partitioning of the spectrum into bands is arbitrary, but in practice 20 equal-articulation bands with equal k_i, or 21 third-octave bands, and in a simplified version 7 or 5 octave bands are used [1].

The input parameters for the TMI are the speech and noise signal levels at the point of reconnaissance contact for the frequency bands (FB), taking into account the arrival directions. The latter point is important if the TMI has directional properties. In such a case, the directional characteristic (DC) will be the mathematical relationship describing it. For example, for a reflector microphone it is approximated by the expression (2).

$$R(\Theta) = \frac{2 * J_1(\psi)}{\psi}, \text{where } \psi = \frac{2 * \pi}{\lambda} \rho_0 * sin\Theta \tag{2}$$

and $J_1(\psi)$ is a Bessel function of kind 1.

In an analogy to antennas, the concept of the coefficient of protective action (CPO) is introduced, which is the ratio of the sensitivity in the direction of interference arrival to the axial sensitivity of a narrow-field microphone. In the case of isotropic interference, an integral index, the directivity index, is applied.

The propagation environment model must convert the arrays of speech and noise signal levels in the FB from their sources to the corresponding levels at the point of reconnaissance contact, taking into account the spatial conditions.

According to the interstate standard, sound propagation attenuation in the terrain (3):

$$A = A_{div} + A_{atm} + A_{gr} + A_{bar} + A_{misc} \tag{3}$$

where A_{div} is attenuation due to geometric divergence, A_{atm} is attenuation due to atmospheric sound absorption (neglected at small distances), A_{gr} is attenuation due to ground effect, A_{bar} is attenuation due to shielding, A_{misc} is attenuation due to other effects (e.g., foliage spread). In the simplest case, only the first summand is retained (4):

$$A_{div} = \left[20\lg(\frac{d}{d_0} + 11)\right] \quad (4)$$

where d is the distance from the noise source to the receiver, m; d_0 is the reference distance (RD) (d0=1m). Constant 11 relates the sound power level of a non-directional point source to the sound pressure level at the RD.

If the source and receiver are located in adjacent rooms and the acoustic signal penetrates the building envelope (BE), the signal levels at the design point are determined by the formula (5):

$$L = L2_{\text{м}} - R + 10lg\ S - 10lg\ B - 10lg\ k, \quad (5)$$

where R - coefficient of sound insulation of BE, dB; S - area of BE, m2; B - acoustic constant of the room with TMI; k - coefficient taking into account the sound field diffusivity disturbance; $L2_{\text{м}}$ - sound pressure level in the room with the source at 2 m from BE, dB, determined by the formula (6):

$$L = L_w + 10lg\left(\frac{\chi\Phi}{\Omega r^2} + \frac{4}{kB}\right) \quad (6)$$

where L_w - source power level, dB; r - distance from acoustic centre of source, m; χ - coefficient taking into account influence of near field; Φ - directivity factor; Ω - spatial angle of source radiation, rad.

In addition to the above relationships, the PE model must account for other possible reconnaissance contact options to maximize its completeness.

The acoustic source (AS) model must convert a given power level or sound pressure level at a reference distance into an array of sound levels in the FB.

For a speech signal source, the spectral levels are calculated as follows (7):

$$Lsi = Ls + Vi\ [\text{дБ}], \quad (7)$$

where Ls is integral level of acoustic signal at distance of 1 m; Vi is weight energy coefficient of the i-th band, in dB it has negative sign; $fagi$ is average geometric frequency of the i-th band.

To model acoustic noise sources (ANS), some types of coloured noise and noise with a spectrum close to speech should be considered [2]. In order to mask speech, a "speech chorus" or near-spectrum pink noise, whose levels in the FB are often used (8):

$$L_{pn} = 10 \cdot log\left[g_{pn} \cdot (ln(f_{ui}) - \ln(f_{di}))\right], [dB] \quad (8)$$

where $g_{pn} = \frac{10^{0,1 \cdot L_{\Pi}}}{\ln\left(\frac{1}{f_{d_1}}\right) - \left(\frac{1}{f_{u_n}}\right)}$,

where L_{Π} is the integral level of the noise source.

The directional coefficient can also be taken into account, showing how much the equivalent sound pressure level in a given direction differs from the sound pressure level of a non-directional source with the same sound power level [3].

III. Results of a Partial Model Implementation

The fig. 1 and fig. 2 shows the results of a partial model implementation for free space in a single plane, representing the verbal intelligibility coefficients for each point in 1 m steps, converted for clarity into greyscale luminance levels.

As TMI was chosen narrow-directional microphone of "linear group" type with the following characteristics: number of microphones n=20, step d=0.05 m, DC of a single microphone - cardioid, directional index of TMI at frequency 1000 Hz - 20 dB. The level of the speech signal at the RD is 60 dB, the level of isotropic noise is 40 dB, the noise levels at the RD from point sources is 80 dB.

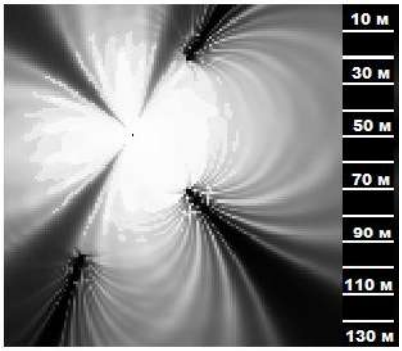

Fig. 1. 3 point noise sources.

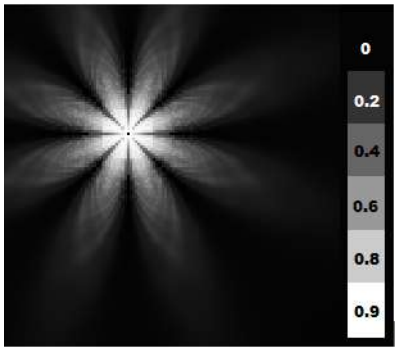

Fig. 2. 8 noise sources surrounding the speech source.

IV. Conclusion

The mathematical model considered can form the basis of software that will greatly simplify and speed up the procedure for modelling the acoustic leakage channel.

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Sound Design Exploration in Educational Multimedia Publications Applying Computing Platform

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***Abstract*—The commonly used practices of preparing a balanced sound support for educational multimedia publications have been examined. The methods for distinguishing key sound sources when modeling sound design have been streamlined and expanded. On basis of determined means of polar characteristics describing of meaningful sound fragments, typical and cardioids' sound fixation pattern were analyzed, which are laid as a basis of developed analytical apparatus of projected microprocessor system for researching of sound content quality for multimedia publication.**

Keywords—educational content, multimedia publication, computing platform, sound design, sound fixation pattern

I. INTRODUCTION

The practice of preparing balanced sound support for educational multimedia publications is an important stage in methodical content quality improving aimed at effective learning ensuring. Sound design in multimedia projects has a significant impact on the student's perception and interaction with field-oriented training materials, facilitation to increase their interest and attention. Adequate audio fragments selection helps to enhance the recipient's overall experience, creating a targeted academic environment, as well as supporting effective communication of messages and information [1].

The high-quality audio support of the educational publication clarifies the researched subject area and strengthens the immersive degree [2], providing a deeper impression of content. The established hierarchy and importance of selected methodical aspects contributes to the convenience and efficiency of the user's cooperation with the content, determines priorities and emphasis for drawing attention to important events in interaction with textual or visual elements.

The situational relevance of audio materials to the educational scenario and their technical performance are of great importance to ensure proper perception of audio recordings. When creating and editing audio tracks, it is important to consider the context and purpose of the educational multimedia publication. Sound design should be aimed at achieving educational goals and contribute to a comprehensive understanding of training content [3]. For example, informative video presentations can use clear and professional voiceovers that explain key concepts and ideas. In training games or interactive tasks, it is advisable to use sound effects that emphasize correct and incorrect answers, providing unobtrusive feedback. Next, for music-oriented content, audio tracks can be specialized for skills development of instruments sounding recognizing, understanding the musical form of analyzed composition, approbation of different genres and styles. In language education, audio tracks should it is worth specialized for improving language skills, teaching pronunciation and developing vocabulary, understanding different language variants, dialects and accents.

When demonstrating natural sounds, the specialization of soundtracks helps to audio effects conceive that occur during the course of physical phenomena or the reaction of chemical compounds. So, typical categories distinguishing the operation sounding of engines, gears, roller bearings, etc. allows engineering degree students to expand their understanding of structure, kinematics and dynamics of mechanisms and systems when studying the scientific foundations of their design. The tracks' categorization in context of signals, oscillation and other aspects of electronic devices will allow visualizing the abstract concepts of wave theory in the study of electrical and magnetic phenomena.

Thus, particular sources distinguish in audio tracks helps students to separate and recognize different situations in subject area, which contributes to development of their professional competences and analytical skills, understanding and perception of concepts and phenomena related to specific engineering branch. This opportunity allows students to focus on specific sound elements and study their role in researched stages of technological process. Therefore, hardware and software complex development for sound design study of multimedia publications is timely and relevant, it will ensure the improvement of technical quality of electronic training content and strengthen the multisensory interaction of recipients with industry-oriented methodical materials.

II. METHODS OF DISTINGUISH KEY SOUND SOURCES IN EDUCATIONAL MULTIMEDIA PUBLICATIONS PREPARATION

Particular sources distinguish in soundtracks is carried out by using and combining a number of methods that allow to virtually place sound sources in space, creating a sense of volume and realism. As noted, soundtracks can be specialized for a wide range of educational purposes depending on the specific requirements and learning context.

A. Limits of spatial sounding effects applying

An effective means to distinguish particular sound sources in an audio track is *stereophonic sounding* using, allowing different sound sources to place in spatial position.

Sound objects can be placed across of virtual scene width, reproducing their spatial localization: this creates the presence effect and realism, and also helps the listener to distinguish and identify particular sound sources more easily.

Panning as a method to distinguish particular sound sources involves moving the source from one channel to another or mixing it in different proportions between channels, moving from left to right or from foreground to background. Panning allows to precisely controlling the position and movement of particular sound sources in space, which makes the sound scene more detailed and realistic.

Amplitude dynamically changing of particular sources is another effective means of distinguish key audio content. Adjusting the volume allows giving a specific sound source a more prominent or muted role in the audio track, emphasizing important elements or leveling out the value of a fragment where distant sources have a lower volume. Volume changing affects the recipient's perception and attention, helping to focus on certain sound fragments.

The use of *reverberation*, *echo*, *chorus*, etc. can also help to particular sound sources distinguish. These effects create a sense of spaciousness and depth of the soundstage, bringing additional acoustic attributes to individual sound sources. So, reverberation gives the impression of presence in a certain environment, and echo emphasizes the volume or movement of particular sound sources.

The presented methods to key sources distinguishing in audio tracks can be used to create more target and effective sound design in engineering disciplines context. They help improve the perception, understanding and analysis of learning material, creating a more immersive and meaningful educational audiovisual experience. In order to prepare adequate audio content for educational multimedia publication, it is necessary to research the hardware for of particular sources distinguishing in audio tracks.

B. Hardware categorization for processing sound sources

When analyzing hardware for particular sound sources distinguishing, it is worth considering its ability to accurately and realistically reproduce sound, control volume levels and spatial processing. The use of appropriate hardware will help to achieve high quality and efficiency in the creation of means of particular sources distinguishing in audio tracks in researched subject area context of professionally oriented academic discipline.

An *audio interface* with the ability to record and reproduce multi-channel sound is used to particular sources distinguishing in soundtracks, which allows for more precise control of the spatial position of sound sources. This device provides communication between computer or other sound recording devices and, in fact, fixation object. Proper listening of audio tracks is essential for effective particular sources distinguishing. For this, in the technological process of sound design, it is necessary to provide high-quality *audio monitors* or professional *headphones* that transmit sound information accurately and with high resolution. This will make it possible to adequately assess the position and placement of sound sources in space.

Sound processors with spatial processing functions can create immersive acoustic effects that help imagine the spatial location of sound sources. *Equalizers* allow adjusting of individual frequencies levels in sound spectrum, which can also be useful for certain sound sources distinguishing. *Sound controllers* and *mixers* are used to precisely control the volume levels of individual sound sources in audio tracks, allowing adjusting the amplitude, panning and other parameters of each source individually, aiding in dedicated sound effects creation. However, among all categories of researched hardware for processing audio effects, *microphones* are of decisive importance as primary means of key sources distinguishing and fixation for sound design of multimedia publication.

III. Polar Characteristics' Description Means of Key Sources of Sound Content

Appropriate microphones choice for distinguishing key sound sources depends on specific needs and thematic purpose of the multimedia publication. The correct microphones setting will ensure high-quality sound recording, accurate sources space localization, helping to achieve the desired sound effect. An important aspect when choosing microphones and when placing sound sources in space is the sound fixation pattern. Also known as audio specimen, this term is used to describe the polar characteristics of a microphone or sound source, indicating the way the sound wave is spatially distributed around the source.

A. Analysis of typical sound fixation patterns

The typical *spherical* pattern of universal microphone is characterized by uniform sensitivity to sounds from all directions [4]. It describes the sound signal coming from any angle within sensitive area (Fig. 1, *a*). Having no noise suppression mechanisms, the spherical pattern guarantees a wide perspective of audio recording without introducing a negative proximity effect. Such parameters provide the devices with a small size and compact design, which allows them to be used in various portable systems. However, in conditions when it is necessary to focus on a specific sound source or when fixing an object in a noisy environment, it is worth expanding this design, for example, with *side addresses* (Fig. 1, *b*), or use other specialized patterns that provide better directionality.

Equal focus on sounds coming from two opposite directions provides a *shaped* pattern with almost no response to sounds coming from the side (Fig. 1, *c*). Formed by special design with two built-in frontal microphone capsules, this pattern provides the strongest proximity effect. Providing the narrowest gather angle, *lobar* pattern works with adjustable zones (Fig. 1, *d*) and allows catching focused sounds at particularly long distances thanks to some width of lateral directions.

B. Cardioid modifications of sound fixation patterns study

The maximum sensitivity of audio specimen cardioid modifications is directed in sound source direction, while sensitivity decreases from sides and back [5]. The main sound fixation area in *cardioid* pattern is in frontal direction, forming a wide, up to 120°, sound capture angle. Such pattern in inverted heart shape (Fig. 2, *a*) allows to effectively sound source distinguishing located in microphone front, while reducing the coverage of unwanted sounds from sides and behind.

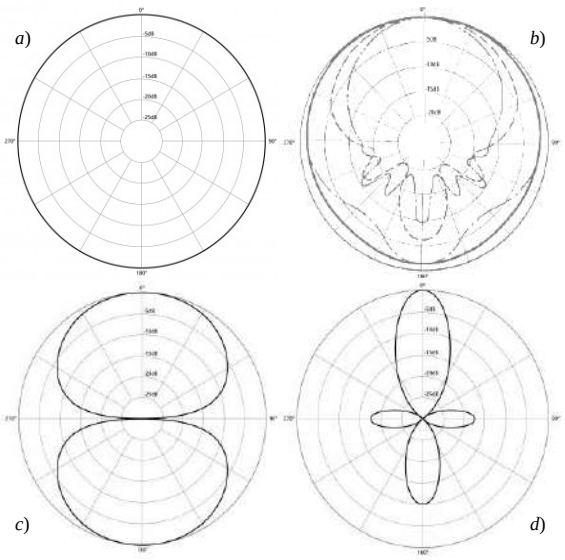

Fig. 1. Diagrams of typical sound fixation patterns

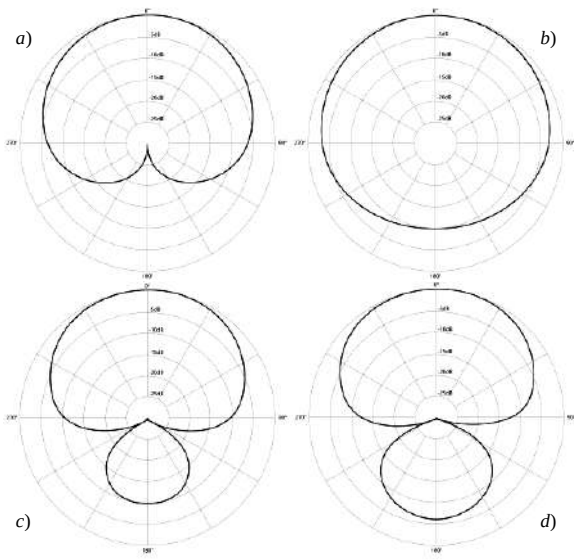

Fig. 2. Diagrams of modifications of cardioid sound fixation patterns

This makes cardioid microphones ideal for situations where it needs to reduce background noises, main sound source separate from environment, or focus on sources in a narrow area. Cardioid microphones applying can be found in many educational situations, including recording live lectures or public reports, conferences and webinars, industrial videography, and field experiments. They provide clear and directional sound capture, which helps to improve the quality of recording and transmission of sound information [4].

Subcardioid microphone pattern has a greater forward directivity (Fig. 2, *b*) and several features that affect its parameters. Characterized by increased sensitivity in the direction of the sound source located directly in front of the microphone, the subcardioid pattern has a wider sound capture angle, fixating sound objects at a short distance from each other and generally located slightly outside the direct direction. By reducing the influence of side and background sounds, such devices guarantee transparent sound with less approximation effect and preservation of natural low frequencies in relatively quiet scenes for rooms with controlled acoustics. However, there is also the possibility of triggering a feedback loop with the speakers [5].

Narrow and accurate sound capture with a larger zone-capturing forward direction and strong sound attenuation from the sides and back provides a *supercardioid* pattern (Fig. 2, *c*), allowing to capture sound sources located far enough from the microphone. Providing good isolation from unwanted background noise and sounds from other directions, distinguishing key fragments and minimizing the differences between them, this pattern type is very useful in situations where need to focus on a specific scene and ensure minimal influence of the environment.

The main sensitivity zone of the *hypercardioid* microphone is also directed forward (Fig. 2, *d*), which allows to accurately fixed the sound source in front of the microphone, but muffles the sounds coming from the sides. At the same time, there is a certain sensitivity to sounds coming from the rear direction, giving advantages in terms of feedback. The hypercardioid means use allows achieving maximum accuracy, high purity of sound and detail.

IV. Generalized structural scheme of the project

To perform computing tasks in the sound patterns researching, the resources of the computing platform as a complex software and hardware environment are used. Such a platform covers unified physical equipment and provides an integrated development environment that allows designing service utilities for managing and distributing project computing resources. The computing platform provides the power to perform complex computing operations, data processing, modeling, analysis, and other tasks that require significant computing resources.

A. Peripheral equipment

To optimal audio specimen research for sound design modeling of educational multimedia publications, it was decided to use the Arduino Uno computing platform [6, 7] based on the ATmega328P microcontroller.

The Keyes KY-038 electret microphone shield chosen for the project contains an audio module with a built-in amplifier and filters to capture pure sound [8].This module (Fig. 3) allows reading audio signals from the environment and carry out their further analysis. The module's power LED turns on when power is applied to the board.

The microphone digital input is connected to serial pin TX0 of computing platform [9]. The digital signal sensitivity is adjusted using from cyan potentiometer. A low signal level keeps the audio module in standby mode, and a high signal level indicates that the microphone has detected a sound pattern. At the same time, the signal trigger LED on the audio module turns on.

The researching of the physical nature of the detected pattern is carried out by the built-in ADC of the computing platform [10], which has the ability to receive amplified analog signals from the microphone through the channel connected to the A4 pin (Fig. 3). KY-038 is able to detect sound patterns in the range of up to 100 dB, which is quite enough for our project (Fig. 1, 2).

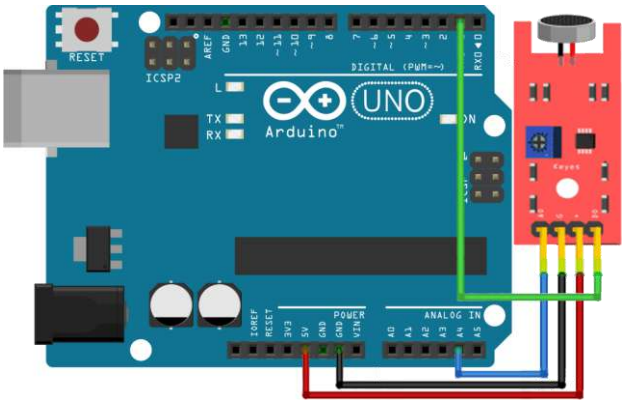

Fig. 3. Connecting the digital audio module board to computing platform

B. Programming the sound pattern research project

In the software of the project for the researching of sound patterns, first of all, the levels of the analog signal [11] coming from the audio module is measured. Further, it is converted into a digital signal using sampling by the analog-to-digital converter of the computing platform and is reduced to decibels. ArduinoFTT.h library was used for signal processing, which allows Fast Fourier Transform to be performed when analyzing the sound spectrum.

The Fourier transform makes it possible to decompose a signal in the time domain into its frequency components in the frequency domain. With supplementary analysis of the sound spectrum, FFT allows revealing the frequency components of the input audio signal. Since the audio spectrum represents the distribution of the signal's energy over different frequencies, applying the FFT to an audio signal produces a spectrogram that shows the intensity of the signal at each frequency versus time. It allows identifying the main components of the sound, such as the fundamental frequency, harmonics, noise components and other sound artifacts.

By revealing the frequency component of the audio signal, the Fourier transform allows the analyzer to identify key components of the pattern, such as bases tones and other features. As a result, a spectrogram is obtained, which visualizes the distribution of signal energy over the frequency spectrum. Next, using the Fourier transform for each moment in time of the corresponding audio fragment, a time-frequency representation of the sound is obtained. This makes it possible to detect changes in the frequency structure of sound depending on time, which is useful when analyzing the dynamics of sound patterns. That is, FFT is a powerful mathematical algorithm for converting data from the time domain to the frequency domain.

In addition to the considered ArduinoFTT.h, other libraries are also involved in the project. Yes, the Wire.h library allows the computing platform to interact with the peripheral via the I2C/TWI interface. On the Arduino Uno board, the SDA data line associated with this interface is located on pin A4 (Fig. 3). Thus, when researching sound patterns, it is possible to analyze different sound sources and their spectral characteristics by adjusting the size of the FFT window, frequency range and other parameters to obtain the desired results [10]. The coverage area identified by sound intensity is displayed on the simulator's serial plotter.

V. CONSOLUTIONS

In the presented study, hardware and analytical apparatus to audio specimens' analysis in sound design modeling for educational multimedia publications are proposed. The spectral information obtained as a result is suitable for further processing on a personal computer, in particular for intelligent comparison of reference target sound patterns and obtained diagrams. The coupling of the microprocessor system and the computer expands the possibilities of the project and allows carrying out more complex studies of sound patterns, capturing more data and interacting with them with the help of additional functions and network connection.

Fourier transformation is also planned to be used for sound signal processing, noise filtering, and amplification of certain frequency components or selection of characteristic features. This helps extract information from the sound that can be used for further analysis and development of sound models.

In the perspective of further research, it is planned to build an expert system of vicious elimination of bugs and integrate the project into built-in complexes of the Industrial Internet of Things.

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Overview of Modern Augmented Reality Capabilities for Creating a Navigation Aid for the Blind

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***Abstract*—This work considers the prospects and possibilities of using augmented reality to create a portable navigation assistant for the blind, the hardware requirements for working with ARCore.**

Keywords—ARCore, augmented reality, Google, smartphone, styling.

I. Introduction

Augmented reality is a technology that adds the ability to use a computer to perceive elements that are absent in the natural perception of a person. This type of task relies on various algorithms to determine the position of the device and / or user in space and the subsequent reconstruction of a three-dimensional scene, in which virtual objects are added. Google's ARCore framework provides the ability to determine the depth of a scene.

According to the WHO, there are at least 39 million blind people in the world. They are severely limited in mobility. Mobility should be seen as the possibility of free movement, independent of outside assistance. To increase it, you need a portable navigation assistant. The methods underlying AR and their implementation in frameworks open up new possibilities for creating such devices [1].

II. Types of Augmented Reality

Augmented reality includes two types of technology. Let's consider them in more detail.

A. Marker based AR

The first attempts to create augmented reality worked on the basis of markers . Additional content loaded on top of or near the markers. The marker is an object known to the application, such as an image, logo, or sound. The most commonly used QR code. The limitation is that this type of augmented reality can only be used with a smartphone [2, 3].

Marker augmented reality solves the problem of Perspective -n- Point - restoring points in 3D space by their perspective projection onto the device's camera plane. Thanks to it, you can restore the position of the phone relative to the picture from the camera.

B. AR without markers

This type of augmented reality uses various hardware sensors for orientation, such as a camera, global positioning systems (GPS , GLONASS, etc.), a compass, a gyroscope, an accelerometer, or depth sensors.

Based on information from available sensors, simultaneous localization and mapping (SLAM) is applied to scan the environment and generate appropriate maps for the placement of virtual objects. SLAM scans the environment and creates 3D placement maps of virtual objects , even if the objects are not in the user's field of view, do not move as the user moves, and the user does not need to scan new images.

Thus, this technology is able to detect objects or feature points in a scene without prior knowledge of the environment, for example, it can identify walls or intersection points. It is a technology that is characterized by association with the visual effect of combining computer graphics with images of the real world.

The first systems using this type of AR used the location and hardware services of the device to interact with the resources provided by the AR software in such a way that the location and orientation of the user in the space where he was determined [3].

III. Overview of the ARCore Framework and Hardware Support

At the moment, there are two frameworks that allow integrating AR capabilities into the application . These are Google 's ARCore and Apple 's ARKit . ARCore is now available for Android , Android NDK, Unity for Android , Unity for iOS , iOS , Unreal Engine .

The most interesting features of ARCore in the context of the development of portable navigation aids for the blind is the internal implementation of SLAM algorithms, which allows you to get a depth map and geospatial navigation that allows you to use links to Google street view.

API change that now uses 16 bits per pixel to represent depth, which increased the maximum depth from 8 meters to 65 meters. Depth values are measured in millimeters [4].

Geospatial anchors can improve navigation accuracy in cities through integration with Google street view. They would be of interest for building advanced GPS- based navigation .

You can't bypass the hardware either. Not all smartphones support the required depth API. Without them, basic functions like surface detection are available, which are not able to provide the required accuracy.

Unfortunately, devices of recent years do not have a hardware ToF depth sensor. Manufacturers were forced to abandon their use due to low interest from users. ToF camera is available and supported in several LG, Samsung and Sharp models .

API support must be checked for each model according to the list on the official ARCore page. It is constantly expanding and updating.

IV. Conclusion

Despite the fact that after the Second World War, more than 40 different systems were created, of which only 13 reached the stage of a commercial product [5]. Nothing is known about them in Ukraine. In underdeveloped countries, the situation is even worse. Blind people have little or no government support.

Taking into account the fact that the ultimate goal is the creation of a navigational assistant for the blind [6], it is necessary to take into account the realities of Ukraine. The material security of this category is low, so we can assume the possibility of acquiring a suitable smartphone with depth support API in the secondary market. Nevertheless, there is a laboratory base [7, 8] and experience in creating telemedicine services [9-11], which can be useful for developing such an assistant for visually impaired people.

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Analysis of the importance of continuous professional development for IT specialists

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***Abstract*—The information technology (IT) industry is constantly evolving and dynamic. Keeping pace with rapid technological progress can be difficult, so it is impossible not to appreciate the importance of continuous professional development of specialists. This article discusses the critical role that continuous professional development plays in shaping the careers of IT professionals, facilitating personal and professional growth and maximizing their potential for success.**

Keywords—continuing professional development, information technology, employability, lifelong learning.

I. WHAT IS CPD AND WHY IT'S IMPORTANT?

Investing in professional development is crucial as it can unlock career advancement opportunities such as promotions. This enables you to sharpen your current skill set while also acquiring new ones. Demonstrating your completion of professional development programs or additional industry certifications on your resume can make you stand out among other applicants. This will showcase your expertise in your field and potentially increase your chances of getting hired [1-3].

When an employee takes the initiative to learn on their own, it sends a positive message to their employer that they are eager to expand their knowledge and are enthusiastic about personal and professional growth.

Continuing Professional Development, or CPD, plays a vital role in the growth of professionals [4-5]. This term is frequently used in the medical sector and stems from "continuing medical education" (CME). In the healthcare industry, healthcare professionals must regularly enhance their expertise, abilities, and performance to stay effective.

But what about the field of IT? It's evolving rapidly with new technologies being developed every day. How can an IT specialist stay current in such a fast-paced environment? Continuous professional development is essential.

Achieving professional growth entails more than just acquiring knowledge. It also involves curiosity, humility, self-awareness, and the drive to venture into uncharted technologies. Let's explore the different training techniques utilized by IT professionals.

II. CPD METHODS IN THE IT FIELD

Professionals in the Information Technology (IT) field depend on different forms of ongoing education to enhance their careers. Here are some examples of such methods [6-10]:

A. Courses and training programs

In order to stay current in the ever-changing IT industry, professionals must stay informed about the latest trends and technologies. Courses and trainings provide opportunities for specialists to enhance their knowledge, learn new tools and methodologies, and stay up-to-date. These trainings can take place at the company, external educational institutions or online platforms.

B. Online courses and video tutorials

Thanks to the Internet and online education, people can now acquire knowledge and skills from the comfort of their homes or offices. Online courses and video tutorials provide a flexible learning schedule and a diverse range of topics, enabling professionals to delve into specific areas of the IT industry that pique their interest or are in high demand.

C. Certification

Many companies provide well-known training and certification programs to assess the proficiency and expertise of an IT professional in a specific domain. According to Columbia Southern University article, obtaining a certification can provide several benefits, including (1) validating one's skills and competencies, (2) boosting career advancement and job prospects, (3) updating knowledge and skills, and (4) presenting oneself as a professional to inspire confidence [2].

It is important to note that while obtaining a certification does not guarantee career success, it can undoubtedly increase your chances of achieving success and advancement within the IT industry.

D. Hands-On Projects and Participation in Team Assignments

IT professionals can apply their knowledge and cultivate

important skills, such as communication, project management, and teamwork, through active participation in real projects and team assignments.

Engaging in Hands-On Projects can aid in building a reliable network of professional contacts and enhancing one's level of expertise.

E. Mentoring

Receiving mentorship can greatly benefit a specialist's career development by providing valuable knowledge, support and resources [3-5].

Mentors possess a wealth of experience and knowledge in their respective fields. They are able to offer valuable insights, provide guidance on professional skill development, assist in overcoming obstacles, and aid in making crucial career decisions. Mentors can help an individual identify the core skills and competencies needed to achieve their career goals and provide targeted advice and practical tools for enhancing one's skills.

Having a mentor can be immensely helpful in boosting one's confidence and motivation. A positive mindset fostered by a mentor can greatly contribute to an individual's career development and overall success.

III. How corporations can motivate their employees to learn

There are several ways for corporations to encourage their employees to learn and grow. Below are some proven strategies for doing so:

A. Creating a stimulating learning environment

Encouraging a positive learning culture at work is key to a happy and healthy work environment. This is why CPD is so important. Companies that implement a CPD-wide culture encourage growth, reflection, commitment, and dedication. This may include providing time and resources for learning, access to educational materials and courses, and creating internal training programs and initiatives.

B. Establish precise goals and plans for employee growth

Employees and corporations can collaborate to establish well-defined development objectives and learning strategies. This approach can enable employees to recognize their potential for advancement and progress within the organization, serving as a potent source of inspiration.

C. Promoting internal opportunities and career growth

Companies can effectively encourage and facilitate internal career advancement by offering training programs. This may include internal retraining opportunities, involvement in high-priority projects, or new job positions based on newly acquired skills. By incentivizing employees who are dedicated to improving their professional abilities, businesses can foster a culture of growth and development.

D. Organization of educational events

Companies often organize training events, seminars, meetups, and conferences to provide their employees with opportunities to enhance their knowledge and skills. These gatherings also allow them to exchange experiences with their colleagues. By offering such events, organizations encourage continuous learning and provide a source of inspiration and motivation for their staff.

To foster employee growth, corporations need to cultivate a stimulating learning environment, establish clear development goals, provide access to resources, and maintain motivation through financial incentives, internal growth opportunities, event organization, and recognition of achievements. By employing these methods, corporations can motivate their employees to learn and contribute to their professional development.

Conclusion

Continuing professional learning is a fundamental aspect of a successful career in the IT industry. By actively leveraging the power of CPD, IT professionals can keep abreast of technological advances, increase their competence and relevance in the labor market, promote innovation, and build strong professional relationships. The use of CPD is critical not only for personal growth, but also for maintaining competitive advantage in the labor market in a field that is constantly evolving.

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Development of Environment for Generating Personalized Schedules

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***Abstract*—Peculiarities of construction and automation of the information system for forming the schedule for educational institutions were investigated. The web application architecture was built, which combines of analyzed means advantages and generates personalized schedules for students, teachers and classrooms according to developed algorithm for effective groups distribution.**

Keywords—schedule, optimization algorithm, modularity.

I. INTRODUCTION

There are about more than a quarter of a million students around the world. And each semester the teachers, students and educational departments employees have discomfort. For administration – to create the schedule that will fit the room area, and teachers' hours and should have a balanced count of lessons. For teachers and students – quickly find the schedule and determine the week's type. In presented study, various approaches to the automated creation of the schedule are analyzed with their advantages and disadvantages.

One of the main reasons for the deterioration of the quality of professional training is assessment and feedback. Our work will be most focused on this reason, as the student will be able to easily find feedback from the teachers. On the other hand, the teacher will receive notifications about appeals and thus get in touch faster and respond to the student in the shortest possible time.

II. TYPES OF AUTOMATION APPROACHED

The automation process could be divided into five main types: constraint-based scheduling, genetic algorithms, machine learning approaches, and timetabling software.

A. Constraint-based scheduling

One of the most popular is constraint-based scheduling based on systematic and rule-based approaches for scheduling. It allows customizing and handling specific requirements for scheduling [1]. But the main disadvantage is that it couldn't consider the best solution for schedule optimization. Set a schedule in huge room, e.g., for a group of ten students.

B. Genetic algorithms

That approach creates the algorithms by applying some selections and mutation operations. It can handle numerous scheduling problems and requirements [2]. The roulette wheel selection is frequently employed method for choosing chromosomes in genetic algorithms. It resembles spinning a roulette wheel, where each chromosome is assigned a portion on the wheel that corresponds to its fitness level. The main disadvantage is that it's a time-consuming process for the effective optimization of the algorithm and efficiency is based on correct selection.

C. Machine learning

Machine learning uses technique of learning historical data and some patterns [3]. It could make predictions or some recommendations for possible future schedule based on teachers' hours, students' ages, etc. The main disadvantage of machine learning is that often the university doesn't have or have a small amount of data for AI training and learning.

D. Timetabling software

That approach uses for building user-friendly applications that will display the schedule for all possible devices and operation systems [4]. According to the high development of technologies, it can fit all requirements and can provide accessibility for people with disabilities. There are fewer disadvantages as to previous approaches. Vain disadvantage is cost of developing and maintaining the application.

III. ENVIRONMENT SOFTWARE IMPLEMENTATION

After comparing different approaches, it was decided to build a web application architecture that would combine the advantages of above means and automate the personalized schedules generation for students, teachers and classrooms. The main architecture (Fig. 1) is to use .NET as a programming language for building the backend and use JavaScript framework Angular for the frontend side. There will be three types of users: anonymous users (everyone who can access the application), teachers who can add information about groups, schedules, rooms, etc., and the admin who will be able to add access for teachers to the application. For security reasons and to make it impossible that anonymous users will be able to modify the existing data, was decided to use Azure B2C as an identity provider and use JWT Token validation from the backend side. For the saving the data selected the SQL Database. For the storing files (such as pictures, excel files, or PDFs) decided to use Azure Blob Storage. For the mail notifications, such as approved/declined access requests, schedule changes will be used in the Email Domain as the SMTP server. And the finally for the saving logs about data manipulation we are using the Application insights.

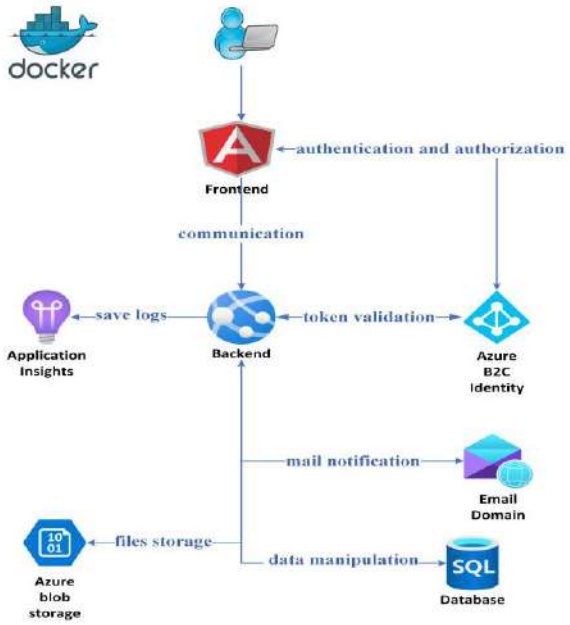

Fig. 1. Architecture of the schedule automation web application

IV. The Group Seating Algorithm with Capacity and Schedule Considerations

The group seating algorithm with capacity and schedule considerations is designed to efficiently assign groups of students to classrooms based on two important criteria: the capacity of the classroom and scheduling requirements. This algorithm ensures that small groups are not assigned to overly large classrooms, and large groups are accommodated in appropriately sized classrooms.

There is a detailed scheme of this logic that is used in our service on the backend side (Fig. 2). This logic scheme outlines the step-by-step process that the algorithm follows to determine the optimal seating arrangement for the groups. The algorithm considers the capacity of each classroom and avoids assigning small groups to large classrooms, thus preventing wasted space. It also ensures that larger groups are allocated to appropriately sized classrooms to avoid overcrowding and helps maximize space utilization, prevent overcrowding, and meet any scheduling requirements.

In addition to capacity considerations, the algorithm can be extended to incorporate any specific scheduling requirements. It will take into account constraints such as certain groups needing to be assigned to classrooms at particular times or in a specific sequence.

Implementing this algorithm in our service's backend enables us to automate the process of assigning groups to classrooms, saving time and effort for administrators or educators responsible for managing these allocations.

V. The Infrastructure Advantages

Thus, in the presented architecture docker containers provide isolation for applications, ensuring that they run independently of the underlying host system and other containers. This isolation helps prevent conflicts between dependencies and provides enhanced security by limiting the impact of any potential vulnerability.

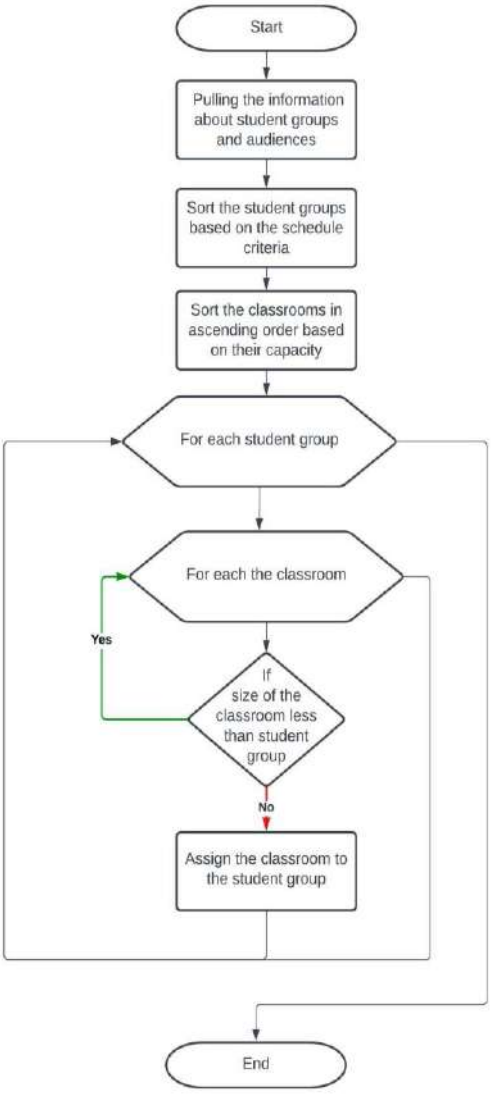

Fig. 2. Algorithm of effective groups distribution

Also will be able to do auto-scale depending on load traffic to the backend part which allows it to keep the high performance of backend system for better client experience. Overall, using Angular with .NET and Docker provides infrastructure advantages in terms of scalability, portability, rapid deployment, isolation, security, development environment consistency, and seamless integration with CI/CD pipelines. These advantages contribute to more efficient and reliable application development and deployment processes.

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“Microprogramming” Course in the Knowledge Field 12 “Information Technology”

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***Abstract*—Microprogramming is used to implement the control logic of a computer’s central processing unit at a low level of programming. The microprogram code specifies the sequence of the processor elementary operations execution, ensures the order of complex instruction sets implementation, and allows the design of high-level programming language commands. The relevance of studying the theory, methods, and techniques of microprogramming in higher education institutions allows students to acquire skills in developing functionally oriented processors structures, their command set, as well as system programming skills. The purpose of studying microprogramming is to gain an understanding of how flexible and a computer’s central processor efficient control is achieved using microcode. This allows microprogram optimization, improving performance and ensuring system functionality. In summary, students will gain an understanding of how hardware and software interact at a low level.**

Keywords—microprogramming, course, processor control, student

I. Introduction

In the development of specialized computing systems, matrix logic circuits and devices with microprogram control and bit-modular organization are widely used. This provides flexibility and versatility, and justifies the technical and economic efficiency of their use [1-5]. The use of such technical equipment allows for the creation of high-speed systems whose architecture takes into account the nature and structure of data, the specifics of the solved problem, and ensures the accuracy of calculations. A clear division of functions and their modular organization allows for easy and efficient implementation of practically any type of logic [4-8]. Devices with bit-modular organization and matrix-type logic circuits are widely used in special-purpose systems [2, 6, 8, 9]. If it is necessary to manufacture a limited quantity of computing systems, it is advisable to use microprogrammed devices [6-8]. However, with a significant planned release of developed systems, it is more economical to use very large-scale integrated circuits. The acquisition by students of theoretical and practical skills in building a computing processor environment and its microprogramming determines the relevance of introducing the academic course "Microprogramming" [9-18]. The purpose of studying this course is to understand the basics of machine languages, low-level languages, and system programming [9, 11, 13].

II. Basic Components of IT

The basic components of information technology (IT) that make up its infrastructure (Fig. 1), and according to which specialists are studied in the knowledge field 12 "Information Technology" are [1-1-4, 6, 8]:

- users of IT;
- environment;
- software;
- technical support.

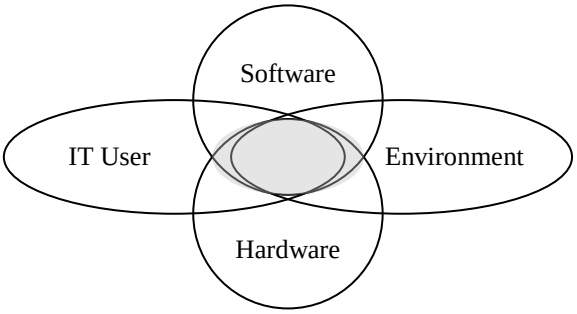

Fig. 1. Infrastructure of the IT basic components.

Students face the most difficulties when studying curses that are adjacent components of information technology (IT). These components are marked in gray on the diagram.

At the same time, it is necessary to define more specifically the components or elements that make up the software (Fig. 2) [3, 4, 6, 9]:

- application software;
- algorithmic support;
- mathematical support;
- operating system;
- system software;
- assemblers;
- machine languages.

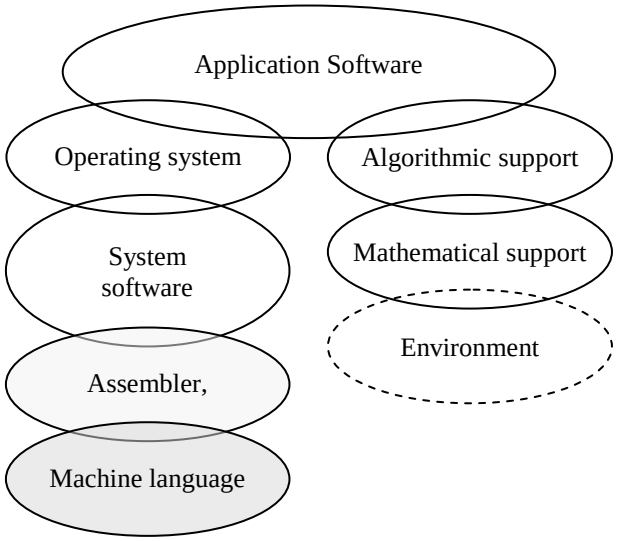

Fig. 2. Hierarchical software components.

As teaching practice shows, students have a "fundamental" gap in understanding the interaction of technical and software components on the microprogramming level (Fig. 3), which creates a psychological barrier to mastering programming languages and understanding the principles of software control and operation of hardware computing tools. Very often, the studying of principles and methods of software control of the computing environment is neglected or omitted, which is based on its dynamic reconfiguration during program execution. Studying high-level languages without a transitional link of microprogrammed control makes it impossible to subjectively understand the basics of programming [10-13, 15-18].

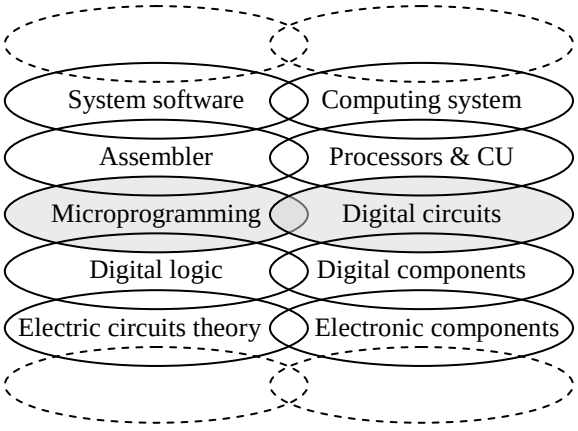

Fig. 3. Software and hardware interaction levels.

III. Implementation of the "Microprogramming" Course

It is proposed to separate the studying of the basics and methods of microprogram control, their integration into low-level languages - assemblers, and the synthesis of high-level programming languages. The relevance of introducing the "Microprogramming" course into the study program is also confirmed by the trends of including similar subjects in the curricula of several leading foreign educational institutions, based on the analysis of materials posted on their internet pages [11-14].

As a result of studying the "Microprogramming" course, a student should understand:

- methods of software control of the computational process course at the hardware level;
- basic principles of microprogramming and the difference between machine code and microprogram;
- methods of building microprograms, including methods of organizing conditional and unconditional program transitions;
- the process of designing microcode, including the process of creating, testing, and supporting microcommands;
- application of microprogramming techniques in designing processors and other computing devices.

Furthermore, a student should know the principles and methods of:

- structural organization and controlled synchronous dynamic reconfiguration of digital computing environments;
- synthesis of microcommands and their organization into program modules;
- organization, construction, and execution of basic components of linear programming and organization of unconditional and conditional transitions;
- synthesis of effective programs at the level of microprogrammed control;
- execution of complex commands at the assembler level, their mathematical and algorithmic structure, as well as their synthesis using microprogramming commands;
- transition to high-level languages and synthesis of commands according to established functional requirements.

A student should be able to:

- analyze the structure of a digital computing environment, evaluate its functional capabilities, and understand the composition of microcommands;
- perform structural analysis and optimization of linear programs, including loops;
- synthesize commands of higher levels of programming languages.

The main courses that support these skills are discrete mathematics, computer circuitry, and algorithmic.

IV. Infrastructure of the "Microprogramming" Course

The infrastructure of the "Microprogramming" course includes the following sections:

- principles and methods of software control of computing environments based on dynamic reconfiguration of their resources;
- synthesis of the structure and microprogram control of a single-bit processor;
- basic addressing methods, microcommand structure, and command decoder synthesis;
- composition of microcommands, their functions, and operation codes;
- methods of organizing, processing, and optimizing linear programs and programs with unconditional and conditional branching;
- synthesis of the structure and microprogram control of a multi-bit processor, specifics of data processing, and command execution;
- methods of organizing the software environment and its processing; state devices;
- methods of synthesizing assembler commands and high-level language commands.

V. Discussion & Conclusions

The feasibility of introducing the "Microprogramming" course is confirmed by the experience of students who have taken it, as well as the practical skills acquired. Recent years' practice shows that teaching the subject significantly improves students' understanding of the software control of computational process, data processing, effective program building methodology, and optimization. It deepens their understanding of the specific usage of high-level programming languages and approaches to programming methods. In general, studying "Microprogramming" course will help students comprehend the principles of computer systems functioning and methods of optimizing their work at the microprogramming level.

Acknowledgment

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Design and Synthesis of Multi-Bit Binary Adders on FPGA

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***Abstract*— Fields of application and main classes of multi-bit binary adders (MBAs) are outlined. The well-known structures of cascade, parallel-serial and pyramidal multi-bit adders are analyzed and their system characteristics are determined when classical single-bit components are used. A comparison of the system characteristics of the MBA using the new single-bit components of full and partial adders is carried out. MBA structures were developed using hardware description languages, and their simulation and synthesis on FPGA was performed.**

Keywords—adder, FPGA, algorithm, structure, hardware complexity, time complexity

I. Introduction

Widespread use of algorithms and methods of performing mathematical operations, including arithmetic operations, logical operations and elementary functions, in computer technology and their improvement allows to find new solutions that need implementation and research on modern element base using FPGA [1,2].

Multi-bit binary adders (MBAs) are widely used components of computing devices, matrix and stream multipliers, microcontrollers and specialized processors [3-6].

Functionally and structurally, multi-bit binary adders (MBAs) are divided into the following classes:

- linear (cascade) without structural branches [4,7-13];
- accumulating adders with memory [4,5,12];
- pyramidal multi-bit adders [14-16];
- adders with accelerated transfers [4,6,14,16];
- vertically organized binary adders [3,4].

The priority criteria of MBA efficiency are to ensure minimum hardware (A_S) and structural (k_S) complexity, maximum speed (τ_s), as well as minimum delay of sum bit formation signals (S_i) and end-to-end transfers (C_i). At the same time, it is necessary to take into account the structural complexity of direct, inverse and paraphase inputs/outputs, as well as to minimize the duration of the signal delay between all input/output pairs of the adder.

Important parameters of components of MBAs are functional completeness (F_s) and minimum structural complexity (S_s) [7,8].

Today, there is a wide nomenclature of structures of one-bit partial and full adders [12-14].

At the same time, the possibilities of improving structural solutions and improving of the system characteristics of single-bit and multi-bit adders according to various criteria of complexity and speed have not yet been fully exhausted [15,16].

Thus, designing and researching the system characteristics of MBAs and their single-bit components not only as separate structures, but as functional multi-bit components in FPGA environments and specialized processors is an urgent scientific and applied task.

II. Overview of known MBA structures and their components

Consider the well-known structures of MBA. The structure of an 8-bit MBA of cascade type is shown in Fig. 1.

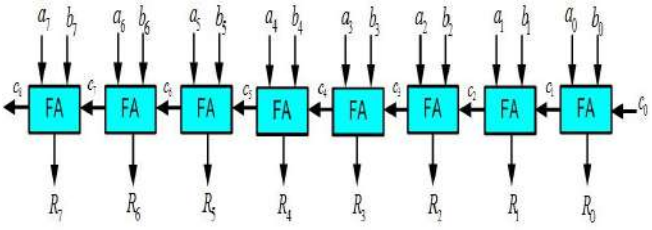

Fig. 1. The structure of an 8-bit MBA of cascade type

The classical structure of the well-known complete one-bit binary adder built on the basis of logic elements AND and "Exclusive OR" is presented in Fig. 2.

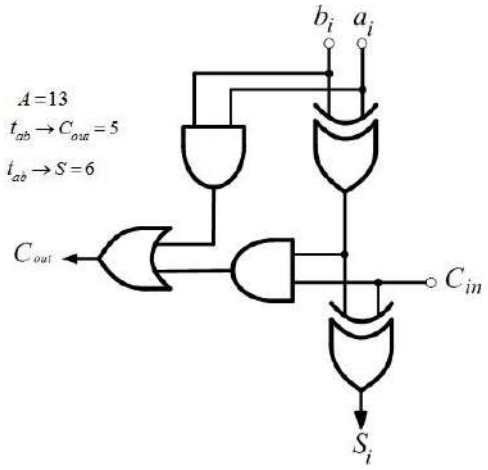

Fig. 2. The structure of a classical full binary adder

In Fig.3 shows the internal structure of the logical element “Exclusive OR”.

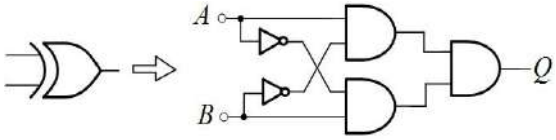

Fig. 3. The internal structure of the logacal element “Exclusive OR”

The logical element “Exclusive OR” contains 5 gates.

When applying known structures of full one-bit adders with hardware complexity $A_{FA}=13$, i.e. logic gates [14], the hardware complexity of such a MBA is calculated according to the expression:

$$A_1 = A_{FA} \times n, \quad (1)$$

where n is its bit rate.

For example, when $n=64$: $A_1 = 13 \times 64 = 832$ logic gates.

When using known structures of full one-bit adders with a time complexity $t_{FA}=6$, i.e. microclocks [14], the speed of cascade-type MBA is calculated according to the expression:

$$t_1 = t_{FA} \times n, \quad (2)$$

where $t_{FA}=6$ microtacts.

For example, when n=64: $t_1 = 6 \times 64 = 384$ microtacts.

The disadvantage of the cascade-type MBA is the low speed, which is due to the sequential formation of bits of end-to-end transfers in each component of the MBA.

The classical structure of the well-known incomplete one-bit binary adder built on the basis of logic elements AND and "Exclusive OR" is presented in Fig. 4.

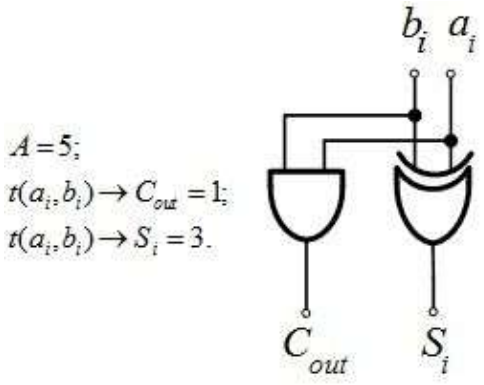

Fig. 4. The structure of a classical incomplete binary adder

Fig. 5 shows the structure of an 8-bit parallel-serial binary adder.

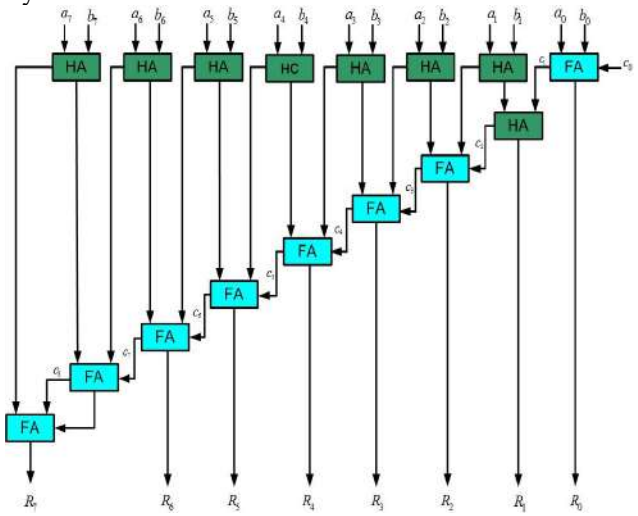

Fig. 5. The structure of the 8-bit MBA of the parallel-serial type

The hardware complexity of such a MBA built on classical components is calculated according to the expression:

$$A_2 = (A_{HA} + A_{FA}) \times n, \quad (3)$$

where n is its bit rate.

When $n=64$: $A_2 = 64 \times (5+13) = 1152$ logic gates.

The speed of the MBA of the parallel-serial type is calculated according to the expression:

$$t_2 = 2t_{HA} + t_{FA} \times (n-1), \quad (4)$$

where $t_{FA}=6$ microtacts, $t_{HA}=3$ microtacts.

When $n=64$: $t_2 = 2 \times 3 + 6 \times (64-1) = 384$ microtacts.

The disadvantage of parallel-serial type MBA is high hardware complexity and low speed.

Fig. 6 shows the structure of an 8-bit MBA of the pyramidal type built on incomplete binary adders.

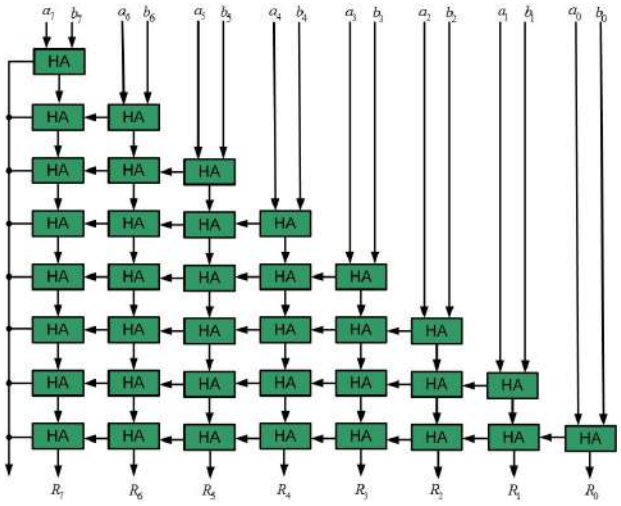

Fig. 6. The structure of the 8-bit MBA of the pyramidal type

The hardware complexity of such MBA built on classical components is calculated according to the expression:

$$A_3 = A_{HA} \times \frac{n^2 + n}{2}, \qquad (5)$$

where n is its bit rate.

When $n = 64$: $A_3 = 5 \times (4096 + 64) / 2 = 10400$ logic gates.

The speed of the pyramidal type MBA is calculated according to the expression:

$$t_3 = n. \qquad (7)$$

When $n = 64$: $t_3 = 64$ microtacts.

The disadvantage of the pyramid-type MBA is the high hardware complexity. However, compared to other types of MBA, it has the best speed.

Fig. 7 shows the structure of an improved one-bit incomplete binary adder, which is described in [17].

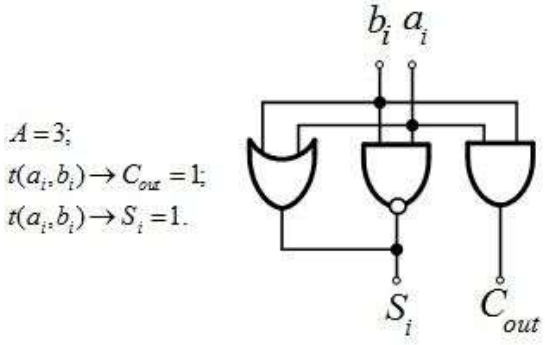

Fig. 7. Structure of an improved incomplete binary adder

When applying such structure of an improved incomplete binary adder in a pyramidal-type MBA, we will get a 1.7-fold reduction in hardware complexity and a 3-fold increase in the speed of forming the sum bit.

The hardware complexity of such MBA built on an improved incomplete one-bit binary adder ($n = 64$) will be equal to $A_4 = 3 \times (4096 + 64) / 2 = 6240$ logic gates, and the time complexity of $t_4 = 64 \times 1 = 64$ microtacts.

Fig. 8 shows the structure of the improved full binary adder, which is described in [18].

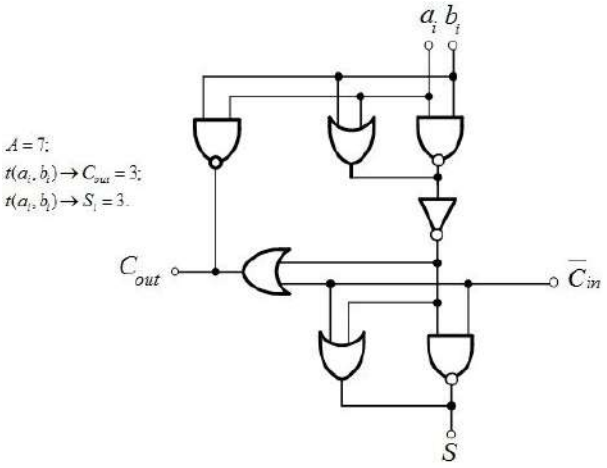

Fig. 8. Structure of an improved full binary adder

When applying such structure of an improved full binary adder in a linear (cascade) type MBA, we will get a 1.8-fold reduction in hardware complexity and a 1.7-fold increase in the speed of forming a through-carry bit and a 2-fold sum bit.

The hardware complexity of such MBA built on an improved full one-bit binary adder ($n = 64$) will be equal to $A_5 = 7 \times 64 = 448$ logic gates, and the time complexity of $t_5 = 3 \times 64 = 172$ microtacts.

When applying the structures of the improved incomplete and complete binary adders in the parallel-serial type MBA, we will get a 1.8-fold decrease in hardware complexity and a 2-fold increase in the speed of forming the sum bit.

The hardware complexity of such MBA built on improved components of incomplete and complete one-bit binary adders ($n = 64$) will be equal to $A_6 = 64 \times (3 + 7) = 640$ logic gates, and the time complexity of $t_6 = 2 \times 1 + 3 \times (64 - 1) = 191$ microtacts.

III. Modeling and Synthesis of MBAs on FPGA

The development of the MBAs of the investigated types was carried out using the hardware description language VHDL in the integrated Active HDL SE environment.

The functional simulation diagram of a 64-bit adder of the pyramidal type is shown in Fig. 9.

The diagram shows the supply of the input 64-bit binary integer values at inputs A and B. 64-bit results of addition are formed at output Q.

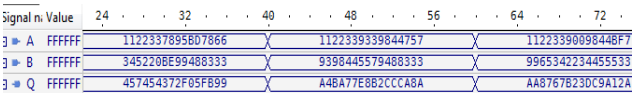

Fig. 9. Functional diagram of the 64-bit MBA of the pyramidal type

The synthesis of the studied class of MBAs was carried out on the FPGA of the Artix-7 family, crystal XC7a100Tcsg324-1 of the Xilinx company [2,11].

The section of the FPGA crystal in an enlarged view, on which the structure of the 64-bit multi-bit adder of the pyramid type was implemented in Vivado Design Suite CAD, is shown in Fig. 10.

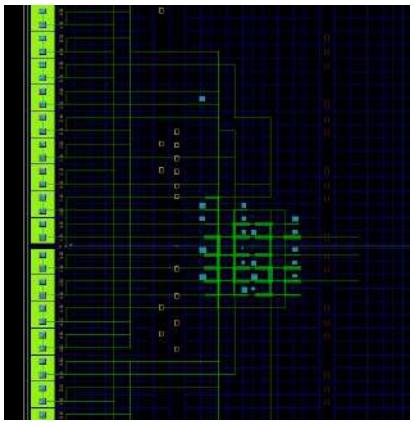

Fig. 9. Implementation of a 64-bit pyramid-type MBA on a FPGA crystal in Vivado CAD

As a result of the synthesis and implementation of the pyramid-type MBA on the specified FPGA crystal, its implementation requires 1237 LUT from the available 63400 ones on the chip, 132 (1%) triggers from the available 126800 ones and has 192 (84%) inputs and outputs from the available 210 ones on the FPGA. The clock frequency of the pyramid-type MBA is 243 MHz.

Table 1 presents the results of MBA synthesis of the studied types on Artix-7 FPGAs using classic and improved components of one-bit full and partial adders.

TABLE I. THE RESULTS OF MBA SYNTHESIS ON FPGAS

№	MBA type	Classic		Improved	
		Number LUT	*F, MHz*	*Number LUT*	*F, MHz*
1	Cascade	64	98	40	163
2	Series-parallel	89	95	56	181
3	Pyramidal	800	125	495	237

From the above results, we can see that the largest number of LUTs must be spent on the implementation of the pyramidal-type MBA. However, its speed is the highest among the investigated types of adders. Serial-parallel and cascade MBAs have the optimal ratio between hardware and time complexity. They have practically the same speed of operation, but lower hardware costs are required for the implementation of the cascade-type MBA.

It was possible to reduce the number of equipment by approximately 1.8 times and increase the speed of the studied class of MBAs by 2 times with the use of improved components of full and incomplete one-bit adders.

IV. CONCLUSIONS

The work describes the main areas of application of multi-bit binary adders, which are components of arithmetic and logic devices of processors. The well-known MBA structures of various types were analyzed and their hardware and time complexity was calculated on the well-known classical element base. The improved components of complete and incomplete one-bit binary adders are described, and improved system characteristics are obtained when they are used in MBA structures. The design and modeling of 64-bit binary adders using the VHDL hardware description language was performed. During the synthesis of the studied class of MBA on FPGA in Vivado CAD, practical results of equipment costs and speed of operation were obtained, which coincide with theoretical calculations.

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Building a Virtual Hardware Laboratory with FPGA and Raspberry Pi Integration

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***Abstract*— Nowadays, when the country is facing the coronavirus epidemic and the war, it is very important for educational institutions to provide their students with the opportunity to continue working remotely.**

All majors that require certain physical equipment have faced problems, as teachers need to find ways to provide students with all the equipment they need to study.

This problem was faced by those specialties that study hardware development, in particular digital circuitry using programmable logic integrated circuits.

Therefore, the issue of creating an application that will allow students to perform laboratory work online, for which they only need access to the Internet, is becoming relevant.

Keywords—FPGA, Raspberry Pi, Hardware, Remote Laboratory

I. INTRODUCTION

Practical and laboratory work is an integral part of education, as it allows students to consolidate the knowledge gained in lectures, gain an understanding of the practical use of this knowledge, and motivate them to continue their work.

In many specialties, such work requires the use of certain material resources, such as laboratory stands, etc.

Given that nowadays it is important to provide students with the opportunity to continue their studies despite external factors such as the epidemic and war, there is a need to create an application that will allow students studying digital circuitry to perform laboratory work remotely [1].

This application should be aimed at improving the quality of education in general, as it will make the learning process more adaptable to unforeseen situations in which attending higher education institutions becomes impossible.

The application for remote FGPA laboratory work should preferably be implemented as a browser-based application, as this is more convenient than using special client applications for a personal computer or phone.

An important component of the system that implements a remote laboratory is a video camera, which allows the user to see in real time what exactly is happening to the hardware during the work.

Also, since the user does not have direct access to the hardware, and therefore cannot physically interact with it, the application must provide the ability to press virtual keys that simulate real buttons in the hardware.

Also, based on the fact that the user does not have direct access to the hardware, the application should provide the ability to flash the FPGA with code written in the hardware description language.

This article discusses the principle of operation of the system, which allows you to perform laboratory work using FPGA boards remotely, namely to test the operation of digital circuits implemented on FPGAs, and the user only needs a device with Internet access

II. HOW TO INTERACT WITH A FPGA BOARD

The FPGA laboratory work involves the student writing code using a HDL (Hardware Description Language), loading this code into the FPGA, and testing its operation.

Testing consists of applying certain signals to the logical inputs of the FPGA, reading the signals on the logical outputs, and checking the correlation of these signals for correctness.

So, to implement a remote laboratory, you need a device that has the hardware capabilities to set signals on its outputs and read signals on its inputs.

GPIO (General-purpose input/output) devices are suitable for these purposes, since the signals are a sequence of logical levels "1" and "0".

Thus, having a device with GPIO and the ability to write software for it, it opens up the possibility of building timing diagrams that display the FPGA's response to external signals.

As mentioned in the introduction, it is important to be able to flash the FPGA board with user-written code using a hardware description language, and therefore the system that implements the remote laboratory must be able to interact with the FPGA board through special interfaces for its programming. For example, JTAG [2].

III. CHOOSING THE HARDWARE

In order to make a choice that balances the above characteristics, you should first analyze the hardware platform requirements in detail.

- First, since the main way to transmit signals in these boards is through I/O ports, the hardware module responsible for transmitting signals to and from the FPGA must have such ports. A microcontroller, another FPGA, or a single-board computer are suitable for this purpose.
- Secondly, the platform must be able to connect to other components of the system using network interfaces. This is difficult to do on an FPGA, somewhat easier on a microcontroller by using libraries for network protocols such as LwIP, and much easier and faster on single-board computers that can run programs written in languages higher than C.
- Thirdly, to scale and develop the project in the future, the platform should provide the ability to update the program code or firmware. This is quite convenient and easy to do on single-board computers running the Linux operating system, which allows remote system management, such as the SSH protocol, and data transfer, such as the FTP protocol.
- Fourthly, as mentioned above, the hardware platform must be able to flash the FPGA, and therefore have interfaces that allow you to connect special programmers. For example, USB-JTAG.

Fig. 1. Raspberry Pi connected to FGPA [3].

Thus, the use of a single-board Raspberry Pi computer as a hardware platform is suitable for this system, since it:

- allows you to write an algorithm in all popular programming languages, which, first of all, increases the speed of development, allows you to use ready-made libraries, and thus reduces the cost of development.
- runs on the Linux operating system, which makes it easy to update the code or transfer files (for example, log files) using special remote control protocols.
- has more computing power than microcontrollers.
- has USB ports that allows using a USB-JTAG FPGA programmers.

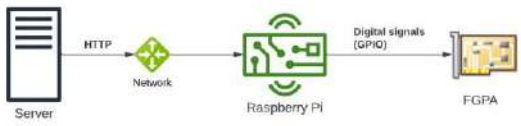

Fig. 2. Structural scheme.

IV. STRUCTURAL SCHEME

Fig. 2 shows the hardware components of the system, namely:

- The Server block is a computer that runs all the programs of the server part.
- The Network block, which is any variant of a computer network that implements the TCP/IP model.
- The Raspberry Pi unit, which, accordingly, is the hardware part of the system that is responsible for communication with the FPGA.
- FPGA unit, which is an FPGA.

Communication between the server and the Rasbperry Pi takes place via the Network computer network and uses the HTTP protocol.

The Rasbperry Pi communicates with the FPGA via GPIOs on both boards, creating a digital communication channel.

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Image Clustering Method on FPGA

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***Abstract*— This study examines the method of clustering in image processing algorithms implemented on programmable logic integrated circuits (FPGAs). The main steps of developing a clustering algorithm are considered, and the choice of clustering approach is justified. Additionally, the steps for analyzing the results obtained from image processing using this method are discussed.**

Keywords—clustering method, FPGA, image processing, k-means,

I. Introduction

In recent years, with the continuous advancement of computer vision and image analysis, there has been an increasing interest in clustering methods for efficient processing and classification of large volumes of data. Field-Programmable Gate Arrays (FPGAs) have emerged as powerful tools for implementing high-performance image processing algorithms, offering parallel processing and low latency [1-8].

This article focuses on a method for image clustering based on the utilization of FPGAs. The method provides an effective solution for automatic image segmentation and grouping, enabling the discovery of hidden patterns and features in large datasets. Applying clustering methods on FPGAs ensures high processing speed and the ability to perform operations in parallel, significantly enhancing the performance and efficiency of image processing systems. This article provides an overview of the image clustering method on FPGA, algorithm development for its implementation, and a step-by-step algorithm for verifying the functionality of the image clustering method.

II. Development of an Image Clustering Algorithm

Developing an image clustering algorithm involves several steps. Below is a general procedure for developing such an algorithm:

A. Defining image features:

First, you need to determine which image features you want to use for clustering. These can be features such as color histograms, texture descriptions, geometric features, and so on. The choice of the right features depends on the specific task and the type of images you are working with.

B. Data preprocessing and preparation:

The image needs to be processed to extract the desired features. This step may involve reducing the dimensionality of the image, normalizing the lighting, removing noise, or other image processing techniques.

C. Choosing a clustering algorithm:

There are various clustering algorithms available, such as k-means, hierarchical clustering, DBSCAN, and others. The choice of algorithm depends on your task, the amount of data, the type of images, and other factors. A detailed study of different algorithms will help you determine the most suitable one for your task.

D. Algorithm implementation:

Implement the chosen clustering algorithm using the selected features and preprocessed image data. This involves developing the program code that implements the algorithm and processes the input images.

E. Evaluation and parameter tuning::

The parameters of the clustering algorithm can affect the quality of the results. It is important to evaluate and tune the algorithm's parameters using metrics such as internal coherence, external coherence, or other clustering quality metrics.

F. Result evaluation:

After performing the clustering, it is important to evaluate the results and provide feedback. Use quality metrics, compare the obtained clusters with expert knowledge, consider task-specific characteristics, and measure how successfully the algorithm achieves its goal.

G. Refinement and optimization::

Based on the result evaluation, you can refine the algorithm, make changes to the features, parameters, or image processing to achieve better results.

This process of developing an image clustering algorithm can be iterative, where the engineer revisits and improves each of the mentioned steps to achieve optimal results for a specific task.

III. Methods of Image Clustering on FPGAs

There are several methods for clustering images on field-programmable gate arrays (FPGAs). Here are some of them:

A. K-means on FPGA:

The k-means method is one of the most popular clustering algorithms. It involves partitioning the data into a pre-determined number of clusters, where each object is assigned to the nearest cluster centroid. K-means can be implemented on an FPGA using hardware blocks for computing distances between objects and centroids, as well as for updating centroids at each iteration.

B. Hierarchical clustering on FPGA:

Hierarchical clustering is based on building clusters hierarchically by merging or splitting close objects. This method can be implemented on an FPGA using a tree-like structure for storing and processing hierarchical information, as well as hardware blocks for performing merge and split operations.

C. DBSCAN on FPGA::

DBSCAN (Density-Based Spatial Clustering of Applications with Noise) is a clustering method that relies on the density of objects in the data space. It identifies regions of high density as clusters and can detect outliers. DBSCAN can be implemented on an FPGA using specialized hardware blocks for computing distances and determining object densities.

D. Spectral clustering on FPGA:

Spectral clustering is based on analyzing the eigenvalues and eigenvectors of the similarity graph between objects. This method can be implemented on an FPGA using hardware blocks for performing matrix operations and computing eigenvalues.

It's important to note that implementing these methods on an FPGA requires developing specialized hardware code and optimization for specific image clustering tasks. The specific choice of method and its implementation on an FPGA depends on the characteristics of the image data, available resources, and performance requirements.

IV. Methods Analysis of the Performance Results of the Clustering Method

The analysis of the performance results of image clustering method implemented on an FPGA may include the following steps:

1) Result validation: It is necessary to verify if the obtained clusters align with the expected results. This may involve comparing them with pre-labeled data or comparing them with the results of other clustering methods.

2) Clustering quality evaluation: Metrics can be used to assess the quality of clustering, such as silhouette index, Davies-Bouldin index, or Rand index. These metrics help evaluate how well the clustering method performs on the given data.

3) Computation time estimation: Measure the execution time of the clustering method on the FPGA. This is important for evaluating the performance and efficiency of the hardware implementation.

4) FPGA resource utilization assessment: Analyze the utilization of FPGA resources, including logic elements (LE), memory blocks, and DSP blocks. It is crucial to ensure that the implementation of the clustering method does not exceed the available FPGA resources.

5) Testing on different datasets: Test the clustering method on various datasets to evaluate its generalization capability and robustness under different conditions.

6) Comparison with other methods: If there are other clustering methods available for comparison, conduct a comparative analysis to determine which method is better suited for specific image processing tasks on the FPGA.

It is also important to consider the limitations and peculiarities of the FPGA when analyzing the performance results. This may include analyzing power consumption, throughput, and signal delays associated with FPGA usage.

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Sobel Algorithm for Processing Medical Images on FPGA

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***Abstract*—FPGAs are gaining interest in microchip manufacturing due to their high computational power and parallelization capabilities. This makes them suitable for compact, integrated devices handling diverse computational tasks, particularly in the medical field. The Sobel operator is a simple method for determining image contours. It utilizes 2D convolution with kernel matrices to approximate brightness derivatives along horizontal and vertical axes. FPGA implementation allows for easy parallelization. However, as a standalone algorithm, it is not ideal for medical image processing due to limited accuracy and noise sensitivity. Instead, it can be used as an additional filter to enhance edges in conjunction with other algorithms, improving diagnostic detail. FPGA implementation enables rapid edge detection, making it suitable for integration into medical image recognition systems.**

Keywords—Image processing, medical images, optimization, Sobel operator, parallelization

I. INTRODUCTION

In modern medicine, the processing and analysis of medical images play a crucial role in diagnosis, treatment planning, and patient monitoring [1-4]. One of the most commonly used algorithms for image processing is the Sobel operator. This operator allows for the detection of edges and contours in images, providing important information for physicians and specialists in the field of medical visualization.

For efficient implementation of the Sobel algorithm in practice, programmable logic devices such as Xilinx FPGAs are widely employed. FPGAs offer high computational power and parallel processing capabilities, which accelerate the processing of medical images. With the flexibility of FPGA configuration, the Sobel algorithm can be optimized to meet the specific requirements and tasks of medical systems, enabling fast and accurate image processing in real-time [5-13].

II. THE SOBEL OPERATOR

As the field of microchip manufacturing continues to evolve, there is also a growing interest in the use of FPGAs. These platforms currently offer high computational power and parallelization capabilities, making them a great choice for creating integrated devices that handle various computational tasks. Particularly, these devices can be of interest in the medical field, where compact solutions for processing images obtained through various methods are needed.

The Sobel operator is a relatively simple method for determining the contours of images in most types. Let's consider its mathematical essence. The Sobel operator uses two square kernel matrices to perform a 2D convolution on the image. This is done to approximate the derivative values of pixel brightness along the horizontal and vertical axes. The expressions for these operations can be formulated in the form of equations:

$$G_y = \begin{bmatrix} +1 & +2 & +1 \\ 0 & 0 & 0 \\ -1 & -2 & -1 \end{bmatrix} * A \text{ and } G_x = \begin{bmatrix} -1 & +2 & +1 \\ -2 & 0 & +2 \\ -1 & -2 & +1 \end{bmatrix} * A \quad (1)$$

where A is the input image, G_x, G_y is images where each point represents the approximate derivatives along the x and y axes.

n the formula (1), the symbol "*" represents the operation of two-dimensional convolution. The approximate gradient value of brightness can be obtained by element-wise summation of the resulting images:

$$G = \sqrt{{G_x}^2 + {G_y}^2}$$

As can be seen, this operator involves relatively simple calculations: to approximate the gradient vector, only eight pixels around each image point and integer arithmetic are needed. Moreover, the filters (1) can be separated, further reducing the number of required arithmetic operations per pixel.

This is a mathematical description of how the Sobel operator works. It is evident that in its software implementation, it can be easily parallelized across any number of threads. For example, with two computational cores, the upper half-frame can process the first core, while the lower half-frame can process the second core.

All of this enables a simple and fast implementation of the operator on an FPGA, thanks to its inherent parallelization capabilities. Figure 1 shows an example of Sobel operator processing on a medical image.

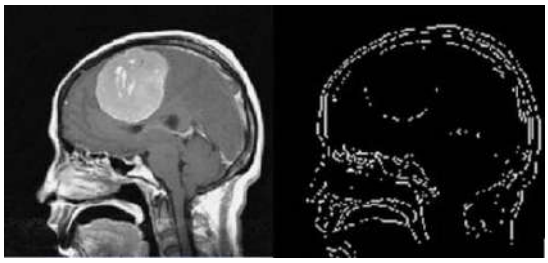

Fig. 1. Head scan before (left) and after (right) applying the Sobel operator.

FPGAs offer several advantages for implementing the Sobel operator [14]:

The ability to process multiple operations simultaneously, enabling parallelism. This accelerates the mathematical operations associated with image processing.

The flexibility to reconfigure the FPGA to optimize the algorithm execution for specific task requirements, allowing hardware optimization according to computational demands.

FPGAs are known for their high speed, making them a good choice for implementing image processing algorithms.

To implement the Sobel operator calculation on an FPGA, the logic and hardware resources need to be configured to perform each stage of the calculations. Additionally, image smoothing using a Gaussian filter can be applied to improve the results.

If we consider the characteristics of the Sobel algorithm, it is not suitable for standalone use in medical image processing [15]. This is due to its relatively low accuracy and the presence of significant amounts of noise. Additionally, if an image has sharp brightness transitions, the algorithm may also detect those transitions as edges.

However, as a standalone algorithm, it can be used as an additional filter to enhance edges in images processed by other algorithms, thereby improving their level of detail. This can be particularly important for medical images obtained through various methods (such as X-rays or positron emission tomography) that contain many fine details crucial for accurate diagnosis [15].

III. Conclusion

In conclusion, implementing the Sobel operator calculation on an FPGA enables fast and easy edge detection. FPGAs provide parallel processing capabilities and compact size, making them attractive for integration into medical image recognition systems that interface with external devices. However, the algorithm utilizing the Sobel operator cannot be used as a standalone tool due to its limitations in accuracy and sensitivity to noise. Instead, it can be employed as an additional filter to enhance edge sharpness in medical images processed by other methods (such as the Canny algorithm). This, in turn, improves the level of detail critical for accurate diagnosis [3].

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Trends and Innovations in Energy-Efficient Microprocessor Development: a Comprehensive Analysis

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***Abstract*—This article explores trends and innovations in the development of energy-efficient microprocessors. It analyzes energy management methods, including voltage reduction and frequency control algorithm optimization. Architectural enhancements such as parallel computing and decentralized architectures are also examined. The use of new materials, such as graphene, perovskites, and quantum dots, to improve energy efficiency in microprocessors is highlighted. The aim of the article is to create more energy-efficient and productive devices that meet the demands of modern society and contribute to sustainable technological advancement.**

Keywords—Architectural enhancements, decentralized architectures, energy-efficient microprocessors, energy management methods, materials, technological advancement

I. Introduction

Development of energy-efficient microprocessors is an important area of research in the field of information technology. Over time and with increasing consumer demands, achieving energy efficiency has become a key factor in ensuring the long-term operation of devices and reducing energy consumption [1-3].

This article examines trends and innovations in the development of energy-efficient microprocessors and analyzes energy management methods and architectural enhancements aimed at achieving this goal [4-5].

II. Voltage Reduction Technologies

Voltage reduction technologies play a key role in the development of energy-efficient microprocessors. Reducing the operating voltage has a significant impact on the energy efficiency and performance of microprocessors. Let's take a look at the importance of voltage reduction, threshold voltage reduction methods, and the benefits and challenges of using low-voltage microprocessors [6-9].

Voltage reduction has several important meanings for energy-efficient microprocessors. First, lowering the operating voltage reduces power consumption, as power consumption is proportional to the square of the voltage. This can extend battery life in portable devices and reduce energy costs in other areas, such as server centers.

The second important value of lowering the voltage is to reduce the thermal load. High operating voltage causes significant energy loss from heat due to conductor resistance and the conversion of electrical energy into heat. Lowering the voltage reduces the heat generated in the processor and reduces the need for cooling systems. This is especially important in today's high-performance computing systems, where efficient cooling can be a challenge.

Various methods are used to reduce the threshold voltage. One of them is downscaling technology, which involves reducing the size of transistors. Reducing the size of the transistors reduces the threshold voltage, which leads to lower power consumption when they are activated. Voltage reduction technologies such as dynamic voltage control, optimization of power supply circuits, and the use of special transistors with a variable voltage threshold are also used.

The use of low-voltage microprocessors has several advantages, but also faces challenges. One of the advantages is lower power consumption, which leads to longer battery life in portable devices and lower energy costs in general. Low-voltage microprocessors also generate less heat, which makes cooling easier.

However, the use of low-voltage microprocessors also comes with challenges. Low-voltage processors can have limited performance, especially in the field of high-performance computing. Also, lower voltage can lead to increased noise and signal distortion, which requires additional measures to ensure signal reliability and quality.

In general, voltage reduction and the use of low-voltage microprocessors are important for achieving energy efficiency and improving the performance of computing systems. The development of voltage reduction technologies and the use of new materials, along with the challenges associated with these technologies, is an important step towards creating more energy-efficient and powerful microprocessors.

III. Use of New Materials

The role of new materials in the development of energy-efficient microprocessors is important. The use of new

materials can improve the energy efficiency and performance of microprocessors.

One such material, graphene, has great potential for reducing energy consumption. Graphene, which is a single layer of carbon atoms, has unique properties, including high electrical conductivity and mechanical strength. The use of graphene in microprocessors can reduce resistance and energy losses, improving the energy efficiency of devices.

Also, perovskites and quantum dots are other new materials that are being used in microprocessors. Perovskites, in particular perovskite oxides, have photovoltaic properties that can be used to improve the energy efficiency of devices. Quantum dots are nanostructures that have unique optical and electronic properties. The use of perovskites and quantum dots in microprocessors can improve energy efficiency, performance, and display color gamut.

The use of new materials in microprocessor design opens up new opportunities to create more energy-efficient and productive devices. Research and development of these materials is an important area for progress in microprocessor technology.

IV. Energy Management Methods

One of the key aspects of energy efficiency in microprocessors is optimizing voltage and frequency control algorithms. Traditional processors operate at a constant voltage and frequency, which can result in unnecessary energy consumption. Optimization of control algorithms allows for dynamically adjusting voltage and frequency based on the workload.

For example, during low workload periods, the processor can operate at lower frequency and voltage, significantly reducing energy consumption. Energy-efficient sleep modes are also being developed, allowing the processor to enter a state of minimal energy consumption during periods of inactivity.

V. Architectural Enhancements

The microprocessor architecture plays a crucial role in ensuring energy efficiency. The use of parallel computing and decentralized architectures is one way to achieve this goal. Parallel computing allows for task distribution among different parts of the processor, thereby enabling more efficient resource utilization and reduced energy consumption. Decentralized architectures also prove to be more efficient in executing computations as they distribute tasks among different nodes of the system, reducing the load on individual components.

Optimization of execution algorithms is also an important aspect of developing energy-efficient microprocessors. Optimization approaches may include the use of specialized instructions, improved data processing algorithms, and the utilization of cache memory to reduce the amount of data that needs to be transferred between different processor components. Optimizing execution algorithms reduces the number of operations and allows for more efficient utilization of processor resources, resulting in lower energy consumption.

VI. Conclusion

The development of energy-efficient microprocessors is a significant task in today's world where there is an increasing demand for device performance and mobility. Implementing energy-efficient technologies and energy management methods allows for longer device operation, reduced energy consumption, and promotes sustainable technological development. The use of parallel computing, decentralized architectures, and optimized execution algorithms opens up new possibilities for energy-efficient microprocessors. The prospects for further development in the field of energy-efficient microprocessor design lie in continuous improvement of energy management algorithms, the adoption of new architectural solutions, and the implementation of innovative technologies.

Research in materials science and nanotechnology may lead to the creation of new materials and structures that improve microprocessor energy efficiency. Additionally, the development of artificial intelligence and machine learning presents new opportunities for optimizing processor performance and ensuring energy efficiency.

All these trends and innovations in the field of energy-efficient microprocessor development are aimed at creating more durable, productive, and energy-efficient devices that meet the needs of modern society and contribute to sustainable technological advancement. Ensuring energy efficiency is becoming an increasingly important task for microprocessor developers, and further advancements in this field promise interesting and promising solutions.

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FPGA-based Architecture for Image Processing using Convolutional Neural Networks

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***Abstract*—This article explores the architecture of FPGA-based Convolutional Neural Networks (CNN) for image processing. It examines the key characteristics of FPGA platforms and their impact on the performance and efficiency of CNN implementation. Special attention is given to hardware optimization, including the use of specialized blocks and algorithmic optimizations. The article also discusses interfaces and interactions with other system components, as well as software aspects for the development, debugging, and integration of FPGA-based CNNs. Examples of applications in medical imaging, automotive industry, video surveillance, and other fields are provided. This article provides an overview of the architecture and optimization of FPGA-based CNNs for image processing, highlighting their potential in various computer vision applications.**

Keywords—Applications, architecture, CNN, FPGA, hardware, image processing, interfaces, software

I. FPGA Platforms

FPGA platforms are a key component in implementing FPGA-based Convolutional Neural Networks (CNN) for image processing. There are several leading FPGA manufacturers, such as Xilinx, Intel, Microsemi, and others. Each manufacturer offers different models and series of FPGAs with various characteristics and functionalities. Each FPGA model and series has its unique features. Characteristics such as the size of the logic element matrix, the number of memory blocks, signal processing speed, and the presence of specialized data processing blocks can impact the performance and efficiency of CNN implementation [1-15].

FPGA platforms have limited resources, such as logic elements, memory blocks, multiplexers, and so on. Some platforms may also have specialized data processing blocks, such as DSP blocks or blocks for convolution and pooling, which contribute to acceleration of computations. Additionally, FPGA platforms have different input and output interfaces, which may include image input standards such as HDMI, Camera Link, or Ethernet [1, 5, 8-12].

II. The architecture of a Convolutional Neural Network

The architecture of a Convolutional Neural Network (CNN) is a structure and organization of layers used for image processing in computer vision tasks. The key feature of CNN architecture is the use of convolutional layers for automatic detection of various features in images. The components of the CNN architecture include:

A. Convolutional Layers:

These layers apply filters to the input image to extract important features. Each filter scans the image using a sliding window, performing a dot product operation to produce a feature map. Multiple filters are applied to capture different features.

B. Activation Function:

After each convolutional layer, an activation function is applied element-wise to introduce non-linearity into the network. Common activation functions include ReLU (Rectified Linear Unit), sigmoid, and tanh.

C. Pooling Layers:

These layers reduce the spatial dimensions of the feature maps, reducing the number of parameters and controlling overfitting. Max pooling and average pooling are commonly used to downsample the feature maps.

D. Fully Connected Layers:

These layers are typically placed at the end of the network and connect every neuron from the previous layer to the next layer. They capture high-level features and perform classification or regression based on the learned representations.

E. Output Layer:

The final layer produces the network's output, which depends on the specific task. For image classification, it may use softmax activation to produce class probabilities..

F. Dropout:

Dropout is a regularization technique used to prevent overfitting. It randomly sets a fraction of the input units to zero during training, which helps the network generalize better.

The overall architecture of a CNN allows it to automatically learn hierarchical representations of image

data, capturing both low-level features (edges, textures) and high-level semantics (objects, shapes). This makes CNNs well-suited for tasks such as image classification, object detection, and image segmentation.

III. Hardware Optimization

Hardware optimization allows for increasing system performance, efficiency, and speed. This can be achieved through several means, such as:

• Breaking down the network into individual modules or layers can enable efficient distribution of computations and FPGA resource optimization. Each module can be implemented as a separate hardware block with its own input and output interfaces.

• Efficient memory management is an important aspect of optimization. Using local memory buffers can reduce the number of accesses to the main memory and improve speed.

• The weights of the neural network can be quantized or compressed to reduce the number of bits required for weight storage and operations. This can help reduce memory footprint and FPGA computational requirements.

• Optimizing the image processing algorithm itself may involve using more efficient operations, replacing computationally expensive operations with lightweight alternatives, or employing additional approximations or simplifications.

• Utilizing powerful FPGA development tools and platforms with appropriate libraries and frameworks can simplify the development and optimization of hardware architecture.

IV. Interfaces and Interactions with Other Components

When implementing FPGA-based Convolutional Neural Networks (CNN) for image processing, interfaces and interactions with other system components are important factors. Here are several interfaces and interactions used in FPGA-CNN:

1) Input and output interface: The FPGA-based CNN can have various types of interfaces depending on the system. Interfaces with image transmission standards like HDMI, DisplayPort, or Camera Link can be used for image processing.

2) Data exchange interfaces: The FPGA-based CNN can interact with other system components such as processors, memory, sensors, data storage, etc.

3) Control and configuration: Interfaces for controlling and configuring the FPGA-based CNN can be implemented through interaction with other system components or dedicated interfaces like UART (Universal Asynchronous Receiver-Transmitter) or SPI.

4) Integration with software: FPGA-based CNN can interact with software that manages the system or performs higher-level data processing. This may involve driver development or even the implementation of relevant libraries.

5) Data transfer and synchronization: Data transmission between different components and synchronization are crucial aspects of interfaces. This may require the use of data transfer protocols such as FIFO (First-In-First-Out) or DMA (Direct Memory Access) for fast and efficient data transfer between the FPGA and other components.

V. Software

Software in the context of FPGA-based Convolutional Neural Networks (CNN) for image processing encompasses various components, tools, and libraries that aid in the development, debugging, and operation of the system. Software includes the following:

A) CNN Model Development:

To develop CNN models for image processing, specific software tools are required that allow for the creation and training of CNN models. Popular frameworks for CNN model development include TensorFlow, PyTorch, Keras, and Caffe. These frameworks provide extensive functionality for model development and training [3, 4, 6].

B) Model Conversion to FPGA Format:

After developing and training a CNN model in a machine learning framework, it needs to be converted into a format suitable for execution on an FPGA. Tools are used to convert the model from the respective framework into Hardware Description Language (HDL) code, such as VHDL or Verilog.

C) Verification and Simulation:

Before deploying a CNN model on an FPGA, it is recommended to perform verification and simulation to ensure the correctness and efficiency of the model. This may involve creating test vectors, conducting simulations, and analyzing results to verify the model's operation before executing it on the FPGA.

D) Interaction with FPGA:

Software can facilitate the interaction between the CNN model and FPGA. This may involve data transfer between the model and FPGA, controlling hardware implementation parameters, configuring inputs/outputs, and retrieving image processing results from the FPGA.

E) Debugging and Profiling:

After deploying the model on an FPGA, debugging and profiling of the system may be necessary to optimize performance and identify potential issues. Profiling tools allow for analyzing execution speed, FPGA resource utilization, and energy efficiency to optimize the system.

F) Integration with Other Systems:

Software can also facilitate integration with other systems, such as control systems, data storage, or other image processing components. This may involve driver development, implementation of network protocols, or other interfaces for data exchange between FPGA-based CNN and other system components.

VI. Examples of Usage

CNNs for image processing have a wide range of applications.

• FPGA-based CNNs can be used for analyzing medical images such as X-rays, MRI or CT scans. They can help detect pathologies, classify cancer indicators, analyze organ structures, and more. FPGAs provide real-time image processing, allowing operators to obtain fast and accurate results [2,8].

• FPGA-based CNNs can be used for image processing in vehicle driving systems. They can assist in obstacle detection, recognizing road signs, identifying pedestrians, and other objects on the road. This enhances safety systems and supports smart functions such as automatic braking and driver assistance.

• FPGA-based CNNs can be used for analyzing video streams from surveillance cameras. They can detect suspicious activities, track object movements, recognize faces, and other objects in video recordings.

• FPGA-based CNNs can be used for image recognition in various domains, such as character recognition in text documents, object recognition in photographs, or object detection in drone images. This can be useful in automated sorting systems, robotics, data analysis, and many other fields.

• FPGA-based CNNs can be used for developing smart cameras and systems that respond to face recognition, human emotion detection, or detection of domestic animals. This can be useful for home security systems, personalized lighting control systems, and other home devices.

VII. Conclusion

The architecture combines the advantages of convolutional neural networks with the capabilities of FPGA to accelerate computations. It allows for efficient image processing by distributing computations between the software and hardware levels. This architecture requires hardware optimization to ensure speed and efficiency in image processing. This may involve the use of specialized blocks for convolutions, pooling, and other operations, as well as optimization of image processing algorithms for FPGA utilization.

Overall, it provides power and speed in image processing by combining convolutional neural networks with FPGA. It paves the way for efficient solutions in the field of image processing and machine learning.

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Pseudo Random Value Generation in STM32 Cube

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***Abstract*—This article is devoted to the description of the random number generator (RNG) in STM22 processors and study of the statistical properties of the values set being generated by the RNG. The analysis of the sequence of random numbers by statistical methods using the possibility of Matlab is given.**

Keywords—STM32, true random number, pseudo random number, random number generator (RNG), Matlab statistics toolbox

I. INTRODUCTION

Many STM32 processor families have a random number generation node on a board. According to the manufacturer datasheet [1], the random number is generated based on a physical sensor, that is, it is physically random. In any case, in the program interface there is no such thing as the initial value of the sequence (seed).

By the hardware cost, being compared to the processor part, RNG is a simple thing. But even for a simple node should be a reason why is it placed into the system [2-13].

II. DESCRIPTION OF THE RND HARDWARE PART

The block diagram from the manufacturer's documentation is as follows (Fig. 1).

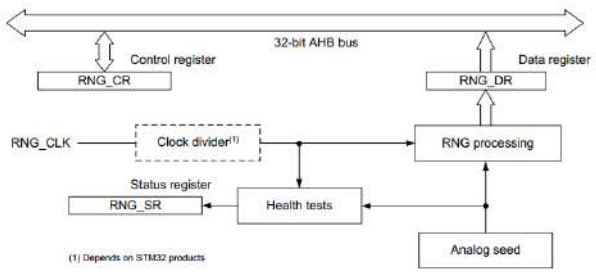

Fig. 1. STM32 true RNG block diagram.

Manufacturer sertified the RND by the NIST SP800-22rev1a test suite.

The NIST SP800-22rev1a statistical test suite is used to probe the quality of RNGs for cryptographic applications [2]. A comprehensive description of the suite is presented in the NIST document entitled A Statistical Test Suite for the Validation of Random Number Generators and Pseudo Random Number Generators for Cryptographic Applications.

The NIST SP800-22rev1a statistical test suite "sts-2.1.1" is a software package developed by NIST that can be downloaded from the NIST web site (search for download the NIST Statistical Test Suite at csrc.nist.gov). The source code has been written in ANSI C. The NIST statistical test suite consists of 15 tests that verify the randomness of a binary sequence. These tests focus on various types of non-randomness that can exist in a sequence.

These test can be classified as follows:

- Frequency tests
  - Frequency (Monobit) test. To measure the distribution of 0's and 1's in a sequence and to check if the result is similar to the one expected for a truly random sequence.
  - Frequency test within a block To check whether the frequency of 1's in an Mbit block is approximately M/2, as expected from the theory of randomness.
  - Run tests To assess if the expected total number of runs of 1's and 0's of various lengths is as expected for a random sequence.
  - Test of the longest run of 1's in a block To examine the long runs of 1's in a sequence.
- Test of linearity
  - Binary matrix rank test To assess the distribution of the rank for 32 x 32 binary matrices.
  - Linear complexity test To determine the linear complexity of a finite sequence.
- Test of correlation (by means of Fourier transform)
  - Discrete Fourier transform (spectral) test To assess the spectral frequency of a bit string via the spectral test based on the discrete Fourier transform. It is sensitive to the periodicity in the sequence.
- Test of finding some special strings
  - Non-overlapping template matching test To assess the frequency of Mbit non-periodic patterns
  - Overlapping template matching test To assess the frequency of Mbit periodic templates
- Entropy tests
  - Maurer's "Universal Statistical" test To assess the compressibility of a binary sequence of L-bit blocks
  - Serial test To assess the distribution of all 2m Mbit blocks.

If results of the test are good then RNG values are random certified and life is beautiful.

III. MATLAB OFFERS

But nothing can stop us from generating good run from STM32F407VG microprocessor that is installed on STM32F4Discovery board to check it in the Matlab Statistics toolbox (Fig. 2).

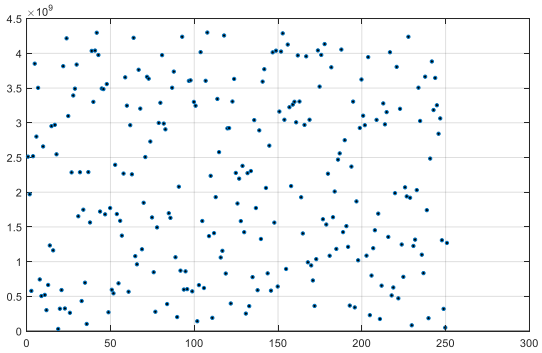

Fig. 2. Small set of random numbers.

The set that is screened on the Fig. 1 consists of 32 bit numbers, that is why the factor x10^9 on the vertical axes.

Distribution and disperse parameters for the set normalized to 1 are presented in the following Table 1.

TABLE I. STATISTICAL PARAMETERS

mean	median	range	standard deviation	geometric mean	harmonical mean
0.4980	0.0061	0.9939	0.2956	0.3721	0.1926

One can see that the mean is close to 0.5 and standard deviation is close to the theoretical value. These values are typical for the uniform distribution.

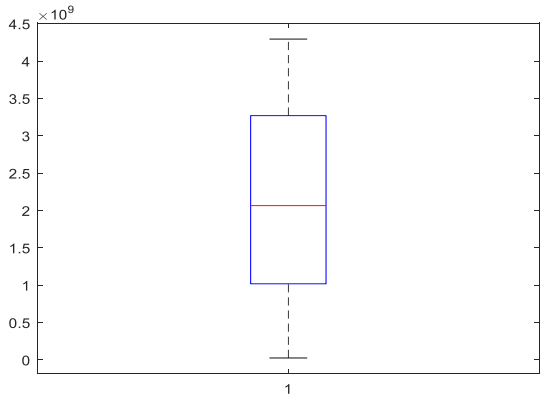

Fig. 3. Box and whiskers plot for non normalized case.

On the box plot one can see a complete coverage of the interval by the set members. The mean and 25% and 75% quartiles are symmetrically distributed as it should be for uniform distribution.

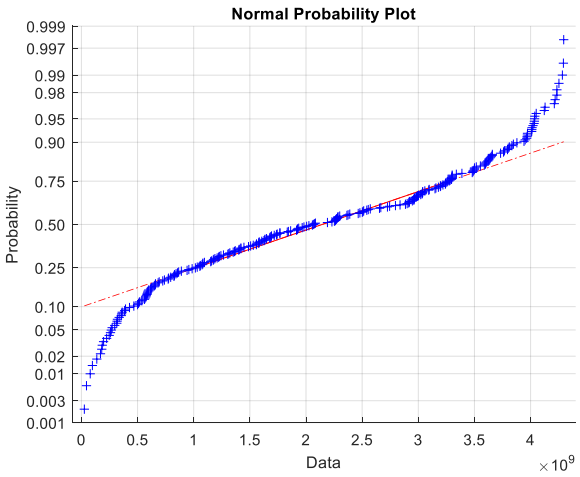

Fig. 4. Normal probability plot.

The Fig. 4 shows the discrepancy to the Gaussian distribution.

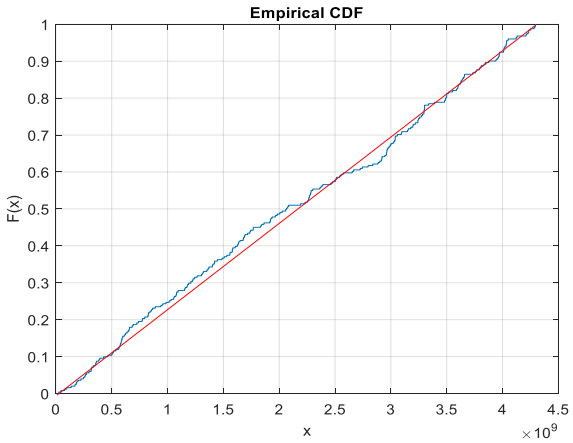

Fig. 5. Cumulative distribution plot.

Fig. 5 shows the empirical cumulative distribution function (cdf) for the data in the vector X. The empirical cdf *F(x)* is defined as the proportion of Xvalues less than or equal to *x*. On the Fig. 5 blue line corresponds to data points and red line is for the uniform distribution case.

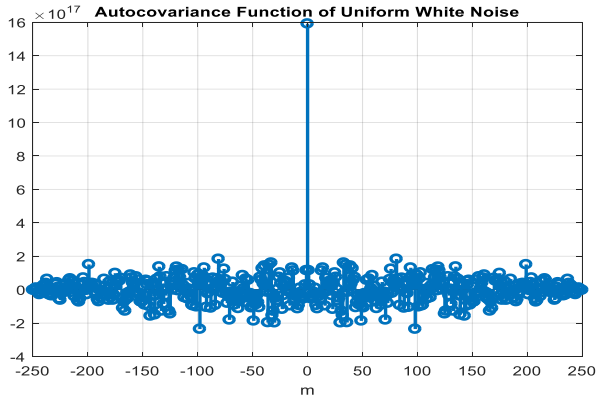

Fig. 6. Autocorrelation function.

Fig.6 is similar to the Delta function.

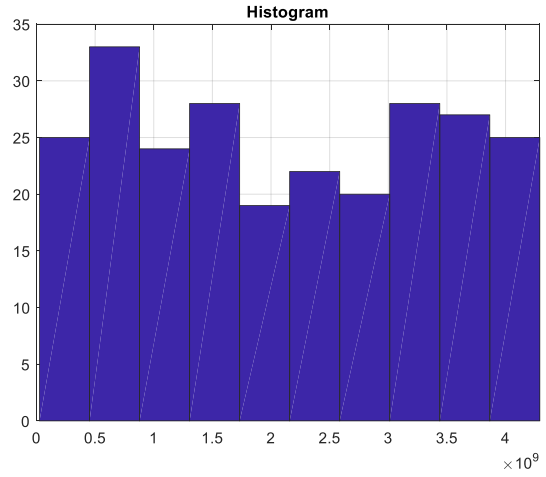

Fig. 7. Histogram of the random values set.

The histogram shown on the Fig. 7 is somewhat close to the uniform distribution. The difference from the uniform can be partially explained by small size of the set. The small size was chosen on purpose for the pattern on the Fig. 1 to be seen.

IV. Further Application

Among security problems, the official Random Number Generator document [3] provides application benefits of utilizing of RNG generated numbers:

- Increase the randomness of numbers,
- Strongly decrease the possibility of guessing values.

And all that was mentioned above seems to be promising, but why manufacturers insert such a device in the system? Among fields where hardware generated random value can be utilized are Monte Carlo something, white uniform noise generation and the base sequence generation for cryptographic purposes to name a few.

Cryptographic purposes seem to be resource consuming for a microcontroller and may require additional hardware support. But truly it must be linked to the good random number generator with a long length of sequence.

Using noise-like signal for modulation purposes is promising topic and requires separate research.

But to use source of physical noise for telecommunication purposes presumes two separated by long distance sites. And a problem of secret random sequence synchronization is appeared. And during exchange by the random sequence between two sites they may stop to be a secret.

V. Conclusion

Usually, to imitate the random value, the congruent method is used [4]. The algorithm is simple and fits the modeling condition: for debug purposes it is suitable to use the same sequence. It will not work for true random values unless one can store it in a good place. Disadvantage of the congruent method for cryptographic purposes is widely known – the sequence can be easily cracked.

More complex procedures of pseudo random value generation exists, but they either can be cracked or are required of serious hardware resources and can be cracked.

Random value generator on a board with microcontroller is a good thing, taking into account that it is not just a linear feedback shift register, but a linear feedback shift register that uses a physical random seed value from analog sensor. Besides, the entropy influence is regulated. In fact the more time interval in between two separate values the better theirs randomness.

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Methods for Processing Medical Images on FPGA

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***Abstract*—This article provides an overview of image processing methods in the field of medical imaging using Field-Programmable Gate Arrays (FPGA). The article analyzes various methods for the analysis of medical images, with a focus on the utilization of FPGA for efficient processing.**

In recent decades, medical image processing has become an integral part of diagnosis, monitoring, and treatment in the medical industry. With the continuous development of new technologies and the increasing volume of medical image data, it has become critically important to have efficient analysis and processing methods that can ensure high accuracy and performance.

Keywords—Canny algorithm, FPGA, Haralick algorithm, image processing, LBP, Renyi dimension, Sobel algorithm

I. Introduction

The relevance of this work is determined by the fact that medical images are a fundamental element of medical diagnosis and treatment, as they reveal the internal anatomy of patients. The analysis of methods for medical image processing on FPGA involves examining and evaluating various techniques and algorithms tailored specifically for medical imaging tasks. This analysis encompasses areas such as image enhancement, segmentation, registration, feature extraction, and classification. The goal is to assess the effectiveness, efficiency, and applicability of these methods in addressing the unique challenges posed by medical image data [1-8].

The aim of this work is to summarize and analyze existing methods for processing and analyzing medical images in order to improve them and practically apply them in medicine. It involves the examination and analysis of key methods for the segmentation of medical images, including comparisons of their effectiveness and accuracy. The practical application of developed methods and algorithms on real medical images aims to enhance diagnostic accuracy and improve the quality of patient care.

By exploring and evaluating various image processing techniques, this work aims to contribute to the advancement of medical imaging technologies and their effective utilization in clinical practice. The findings and insights gained from this study can potentially enhance the accuracy and efficiency of medical diagnoses, leading to improved patient outcomes and overall healthcare quality [1-8].

II. Analysis of Methods for Medical Image Processing on FPGA

Key aspects of the analysis include evaluating the computational efficiency of FPGA-based implementations, assessing the accuracy and robustness of the processing methods, and considering the resource utilization of the FPGA device. As a result of the research, five commonly used methods have been identified:

A. The Canny algorithm:

The Canny algorithm is one of the most widely used image processing algorithms for edge detection. It consists of several stages: image smoothing, calculation of brightness gradients, noise suppression, thresholding, and edge linking.

In the first stage, the algorithm starts by smoothing the image to reduce noise and prepare it for further analysis. Typically, a Gaussian filter is applied to blur the image.

In the second stage, using the smoothed image, gradients of intensity are computed at each pixel. This indicates the rate of change of intensity and helps identify potential edges. Differential filters like the Sobel or Prewitt filters are often used for this purpose..

In the third stage, in order to eliminate insignificant gradients caused by noise, a thresholding technique is applied. Gradients below a certain threshold are considered noise and discarded.

In the fourth stage, a threshold value is determined to separate significant edges from the rest of the image. This threshold can be a static value or dynamically computed based on statistical properties of the image.

In the fifth stage, The individual gradient responses that correspond to edges are connected to form continuous edge segments. Various approaches such as edge grouping algorithms or edge tracing algorithms can be used for this step.

This algorithm is used for edge detection in images and for determining the shape of objects in an image.

B. The Sobel algorithm:

The Sobel algorithm is a popular method for processing medical images to detect edges and contours of objects. It is based on computing the gradients of brightness in the image and consists of the following steps:

- Preprocessing of the image: Before applying the Sobel algorithm, preprocessing of the image is often performed to smooth out noise and improve image quality. This may involve applying smoothing filters, such as a Gaussian filter.
- Computing brightness gradients: In this step, two Sobel operators are applied - one for computing the vertical gradient and another for computing the horizontal gradient at each point in the image. The Sobel operators are used to highlight changes in brightness between neighboring pixels.
- Computing absolute gradient values and directions: After computing the vertical and horizontal gradients, the absolute gradient values are calculated for each point. The direction of the gradient is also determined, which helps determine the orientation of the edge.
- Applying a threshold value: To extract significant edges and suppress noise, thresholding is applied. Pixels with absolute gradient values below a certain threshold are considered noise and discarded, while pixels with higher values are preserved as object edges.
- Edge linking: Finally, the detected edges are linked to form continuous object contours in the image. This can be achieved through operations like connected component labeling or edge tracing.

C. Renyi dimension:

Renyi dimension is determined by estimating the entropy or information distribution within the image. It measures the degree of non-uniformity or variability of pixel intensities in the image. A higher Rényi dimension indicates more complex structures or images with a greater number of details and textures.

For processing medical images on FPGA, the Rényi dimension algorithm can be implemented by computing the informational content of pixels or using specific formulas for entropy estimation. FPGA provides high computational power and the ability for parallel processing, enabling efficient calculation of the Rényi dimension on medical images in real-time.

Applying Renyi dimension for processing medical images on FPGA can aid in analyzing structural features, detecting important details, and highlighting regions of interest in the images. This can be beneficial for diagnosis, measurement of object sizes, or assessing the complexity of pathological changes.

D. Local Binary Pattern, LBP:

The Local Binary Pattern (LBP) method is a technique for comparing the intensity of pixels at a specific pixel with their neighbors, which provides information about local texture features. The LBP method is based on comparing the pixel intensities at a central pixel with its neighbors. Typically, this comparison is performed using binary encoding. The application of LBP allows for the extraction of various local texture features such as spots, lines, and circles.

The LBP method can be used to determine certain image characteristics, such as texture energy, contrast, and smoothness. Its application in practical medicine can aid in the diagnosis and monitoring of diseases such as breast cancer, lung cancer, hepatitis, tuberculosis, and others.

E. The Haralick algorithm:

This is a method for analyzing texture in an image based on its statistical properties. The main idea is to identify a set of statistical characteristics of the texture in the image and use them for image classification. The Haralick method can be used to describe textures in images and determine their characteristics. Statistical features such as energy, contrast, homogeneity, and others are utilized to describe textures.

The application of the Haralick method can be beneficial in the processing of medical images, such as X-ray images, magnetic resonance imaging (MRI), and other fields related to image processing. One of the advantages of the Haralick method is its ability to assess textures from various directions and scales.

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Role of Web Application Security in the Modern Educational Process at Higher Education Institutions

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***Abstract*—The purpose of the presentation is to raise awareness about the security issues of web applications, provide an overview of potential threats, and offer recommendations for effective protection methods.**

Keywords—web applications, cybersecurity, web application security, protection methods

I. Introduction

The role of web application security in the modern higher education process is crucial and cannot be underestimated. Web applications, such as distance learning platforms, electronic document management systems, student accounting programs, and others, provide convenience and greatly enhance the quality of education for students and teachers [1]. However, if the security of these systems is not properly considered, it can lead to significant consequences.

II. Web Application Security: Reducing Risks and Protecting Confidentiality

The main security risks of web applications include system breaches, leakage of confidential information, viruses, and other types of malicious software [2]. Firstly, web application security is important for ensuring the confidentiality, integrity, and availability of the information transmitted and stored within the application. Students and teachers must have confidence that their data is protected from unauthorized access and malicious attacks.

The second most important aspect of web application security is protection against cyber-attacks and data breaches. In today's digital world, where attackers are constantly seeking ways to infiltrate systems, it is essential to have effective security measures in place to prevent data leaks and theft [3-6].

III. Conclusion

Therefore, implementing effective security strategies and practices, educating students and teachers about the basics of cybersecurity, and ensuring secure learning environments are important steps in improving the educational process [7-11]. The development of advanced technologies and collaboration between universities and experts are also key factors in ensuring web application security in higher education. Implementing effective security measures enhances the quality of education and learning experience, allowing students to learn safely.

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Cooperation with the University of Limoges on Teaching the Discipline "Designing Devices on Microcontrollers and FPGAs"

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***Abstract*—The paper analyzes the cooperation of the Department of Microprocessor Technologies and Systems of the Kharkiv National University of Radio Electronics with ENSIL-ENSCI University of Limoges in the direction of educational activities related to the design of devices on microcontrollers and programmable logic integrated circuits. The results of the fruitful cooperation of universities regarding the implementation of training aimed at training specialists in the field of development of digital devices are shown.**

Keywords—NURE, ENSIL-ENSCI, University of Limoges, Department of MTS, training, exchange of experience, FPGA, VHDL, Matlab, design, digital scheme, goals of sustainable development.

I. INTRODUCTION

Cooperation of the Kharkiv National University of Radio Electronics (NURE) with institutions of higher education and institutions of other countries is based on the principles of the priority of national interests, the development of the educational and scientific potential of the university, the systemic and mutually beneficial nature of cooperation, the conclusion of contracts with foreign legal entities and individuals regarding student education, training of scientific personnel, internships, conducting scientific and research works, etc.

The internationalization strategy of NURE, which is an integral part of NURE's development strategy, is aimed at: ensuring sustainable development, promoting the achievement of sustainable development goals, strengthening academic positions, improving the quality of education and competitiveness at the national and international levels.

The internationalization strategy of NURE is designed to prepare students for the future realization of potential in the global world and to teach them to be competitive in the labor market.

II. THE COOPERATION

The Department of Microprocessor Technologies and Systems (MTS) of the Kharkiv National University of Radio Electronics trains specialists in the field of designing devices on microcontrollers and field programmable gate arrays circuits (FPGAs) [1-5]. The main task of the fundamental department of MTS is to strengthen the quality of training of professional engineering personnel in accordance with European standards in the field of microprocessor technologies and systems [6-10].

Since 2018, the Department of MTS has been cooperating with ENSIL-ENSCI University of Limoges (Limoges, France) on the development and coordination of educational materials for the discipline "Device Design on Microcontrollers and FPGAs". The discipline "Designing devices on microcontrollers and FPGAs" includes three modules [11-15]:

- The module "Modeling digital signals using Matlab and VHDL" aims to study the mathematical principles of digital signal processing and master the basic algorithms used for the analysis and synthesis of digital signal filtering devices.
- The "Microcontrollers" module is aimed at: studying programming of modern STM32F4xx microprocessors produced by the ST company for programming on C++ language, in-circuit debugging of the microprocessor- based software controlled electronic system. Considerable attention is paid to learning the programming language, working with

different software, the STM32Cube packages and the IAR Embedded Workbench for ARM software for writing and debugging programs, as well as the use of these microprocessors in digital systems for transmitting and processing information.

- The FPGA module aims to study the architecture and programming of modern Artix-7 of Xilinx FPGA family (Fig. 1), the VHDL digital device design language, and debugging methods and tools using Vivado CAD software as well as the use of FPGAs for the development of digital signal processing systems.

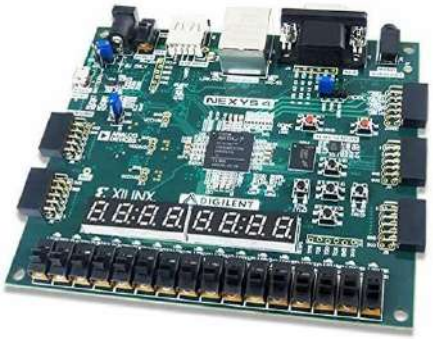

Fig. 1. Nexys 4 DDR Artix-7 FPGA Trainer Board.

The following disciplines are studied at ENSIL-ENSCI University of Limoges:

- "Digital Circuit Design" aims to: study FPGA architecture, VHDL programming, combinational and synchronous circuits on a Digilent Basys 3 training board containing Artix 7 FPGAs (Fig. 2) and Xilinx Vivado software.
- "Systems on a crystal (SoC)" aims to: study the structure and architecture of embedded systems, the basics of SoC, the advantages of API using PicoBlaze VHDL.
- "Introduction to analog and digital filtering" aims to designing filters in the continuous time domain, designing filters in the discrete time domain (digital filters) using Matlab.

Fig. 2. Artix-7 training board from Digilent Basys 3.

Both collaborating parties carefully and carefully approached the choice of hardware and software, on the basis of which the training programs are built. In all parts of the courses mentioned, we see market leaders - Matlab from MatWorks, STM32 from ST.com, Artix 7 from Xilinx. In all these cases, players in their segments have held more than 35% of their respective markets for a long time. The use of software processors PicoBlaze and MicroBlaze allows students to be trained as specialists for companies that create advanced electronics using modern and worthy examples.

Within the framework of cooperation between universities, there is a regular exchange of experience in the direction of designing digital devices, modernization of the content of educational disciplines, the content of laboratory-practical classes, participation in conferences and forums et.

The discipline "Designing devices on microcontrollers and FPGAs" is studied in the set of general and special professional training for students of the first (bachelor's) level of higher education of the university faculties: Faculty of Automatics and Computerized Technologies; Faculty of Information Radio Technologies and Technical Information Security; Faculty of Electronic and Biomedical Engineering; Faculty of Information Communications. The discipline is studied by students of the following specialties: 171 Electronics, 172 Electronic communications and radio engineering, 173 Avionics, 174 Automation, computer-integrated technologies and robotics, 175 Information and measurement technologies, 163 Biomedical engineering, 125 Cyber security and information protection.

NURE students who studied the discipline "Designing devices on microcontrollers and FPGAs" have the opportunity to participate in the selection for studies under the program "International semester at ENSIL-ENSCI University of Limoges for NURE students.

Students of NURE as partners of the academic exchange can apply for [16]:

- for the "international semester" (course in English);
- for the "classic academic semester" (course in French);
- internship.

The maximum length of stay for exchange students at the host university is one academic year or an equivalent period. Continuation must be approved by both universities.

NURE students admitted to ENSIL-ENSCI under the exchange program within the framework of the "classical" academic semester can study in the "Electronics and Telecommunications" and "Mechatronics" specialties. They can also register for the international semester.

The study program at the host university will be determined by the exchange students in agreement with the academic supervisors of the host and sending universities. Academic evaluation is carried out in accordance with the rules of the host university, languages, knowledge of digital device design, circuitry, etc. Both universities participate in the competitive selection process [16].

Both partner universities facilitate the exchange of students for internships. Transfer and accumulation of subjects during the internship, which can replace practical training (or graduation projects), are agreed according to the credits (ECTS) of the host university. The subject of the internship is determined by the host university and will be confirmed by the referring university. A student applying for an internship must have a sufficient level of English/French.

The selection of students to participate in the program "International Semester at ENSIL-ENSCI University of

Limoges for NURE Students" takes place on a competitive basis, which includes: average score for studies, level of knowledge of a foreign language, knowledge of designing digital devices, circuit technology, etc. Both universities participate in the competitive selection process.

As a result of the cooperation between NURE and ENSIL-ENSCI, dozens of students have been trained and are currently studying under the "international semester", "classical academic semester" and internship programs. Scientific and pedagogical workers of NURE were also involved in international programs and research. Despite the difficult situation in Ukraine caused by the Russian-Ukrainian war, fruitful cooperation between partner universities continues even now.

III. Conclusions

International activity in the system of higher education and science was and remains an important component of the functioning of our university. In the conditions of globalization, full-fledged activity of higher education institutions is possible only thanks to their internationalization. Globalization of higher education contributes to achieving the goals of sustainable development.

The cooperation of Kharkiv National University of Radio Electronics with ENSIL-ENSCI University of Limoges demonstrates the high level of training of students of the second (bachelor) level of higher education in the field of designing devices on microcontrollers and programmable logic integrated circuits. What contributes to the successful study of NURE students under international exchange programs with the ENSIL-ENSCI university.

The participation of students, graduate students, scientific and pedagogical workers of NURE in programs of international training, internships and scientific research contributes to the achievement of the following goals: integration of higher education into the European space; exchange of best practices and experience in the fields of education and science; modernization of the higher education system; digitization of education and management; improving the quality of higher education and the effectiveness of scientific research; increasing the competitiveness of the educational and scientific community; development of professional skills and personal qualities of program participants.

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Neuron Networks Design in STM32 Cube

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***Abstract*—This article is devoted to analyzing the possibilities of using a neural network in a project based on STM32 microcontrollers. Support for many different libraries is discussed. The limited RAM size can be mitigated by using external flash memory connected to the USB port.**

Keywords—AI, neural network, STM32.

I. Introduction

Today, the use of neural networks in technical applications is no longer surprising. In various projects, these tasks can be implemented using a variety of methods, including with the support of a neural network [1-5]. In some cases, it gives an advantage in the efficiency of solving the problem [1].

In terms of general applications for artificial intelligence, it seems that the best field for AI is to intelligently search very large data sets and format information, for example, from text form to visual form; or processing of sound, speech, etc. On the contrary, st.com in its ever-expanding portfolio already has several utilities for using pre-trained neural networks to implement user projects.

II. State of the Art in the Neuron Networks

To create a working neural network, one should complete a list of steps [1, 6]. The main stages of creating an artificial neural network:

- Data collection.
- Preprocessing.
- Building and training the model.
- Quality analysis and interpretation of the model.

Even in the conditions of the modern proliferation of computers, the implementation of the listed stages is associated with a significant expenditure of time and money, primarily human ones.

One cannot get rid of the data collecting stage. It can be automated, but it is strongly recommended that the data should be preprocessed and labeled for training purposes. It is this stage that takes time and supervising. These two stages are considered as a data preparation [7].

As for the building and training the network, this process is not completely formalized, but strong support can be easily found. There are well-built programs of deep learning. Among them there are propriety software and free software. It is Keras, Microsoft Cognitive Toolkit, ML.NET, OpenNN, PyTorch, TensorFlow, ONNX to name some from free software (Fig. 1).

For example, using link of Kears and Tensor Flow one can prepare well-structured and trained and neural network model, but it is not enough to start a technical project.

Fig. 1. AI model libraries that can be supported by current ST utilites.

III. ST Offers

To start your work with hardware, one should have the utility. It is better to be some good one like STM32 Cube AI. And to load your pretrained model, it is better should be optimized and validated.

So, the STM32Cube AI. It can be used together with CubeMX or through command line interface. It provides the tool to build step by step a complete Artificial Intelligence (AI) IDE-based project for STM32 microcontrollers with automatic conversion of pretrained Neural Networks (NN) and integration of the generated optimized library. The X-CUBE-AI Expansion Package is fully integrated with the STM32CubeMX tool. Its user manual also describes optional add-on AI test applications or utilities for AI system performance and validation.

It is announced that it is supported by various boards of ST production, not only STM32G4, STM32L4, STM32L4+, STM32L5, STM32F7, STM32H7 lineage, but by STM32WB, or STM32WL and even STM32F0, STM32F3, STM32F4and STM32G0.

Its core engine provides an automatic and advanced NN mapping tool to generate and deploy an optimized and robust C-model implementation of a pretrained Neural Network (DL model) for the embedded systems with limited and constrained hardware resources. The generated STM32 NN library (both specialized and generic parts) can be directly integrated in an IDE project or makefile-based build system. A well-defined and specific inference client API is also exported to develop a client AI-based application. Various frameworks (DL toolbox) and layers for Deep Learning are supported. All X-CUBE-AI core features are available through a complete and unified Command Line Interface (console level) to perform the main steps to analyze, validate, and generate an optimized NN C-library for STM32. It provides also a post-training quantization support for the Keras model [7].

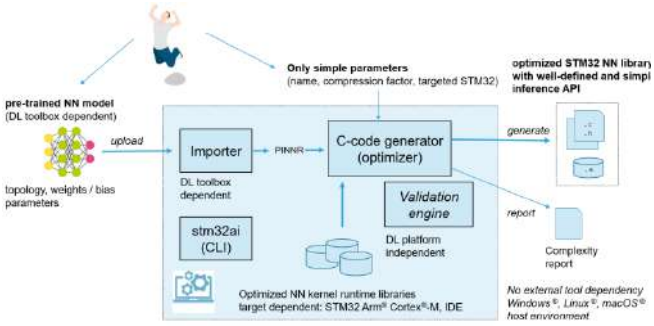

Fig. 2. X-CUBE-AI core engine.

To keep the whole system on diet, X-CUBE-AI code generator can be used to generate and deploy a prequantized 8-bit fixed-point/integer Keras model and the quantized TensorFlow™ Lite model. For the Keras model, a reshaped model file (h5*) and a proprietary tensor-format configuration file (json) are required [7].

The code generator quantizes weights and bias, and associated activations from floating point to 8-bit precision. These are mapped on the optimized and specialized C implementation for the supported kernels. Otherwise, the floating-point version of the operator is used and float-to-8-bit and 8-bit-to-float convert operators are automatically inserted. The objective of this technique is to reduce the model size while also improving the CPU and hardware accelerator latency (including power consumption aspects) with little degradation in model accuracy [7].

The component X-Cube-AI got variety of controls (Fig. 3)

From the user point of view, the integration of the X-CUBE-AI Expansion Package can be considered as the addition of a peripheral or middleware software component. On top of X-CUBE-AI core, the following main functionalities are provided:

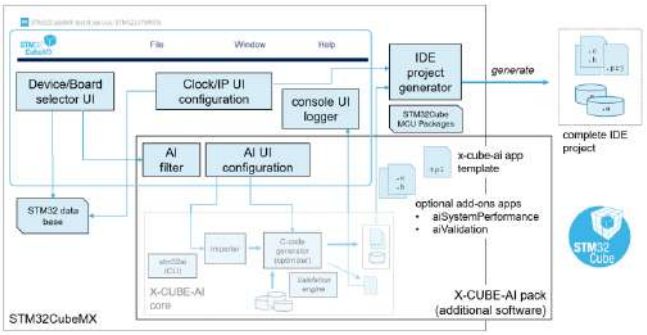

Fig. 3. X-CUBE-AI core in STM32CubeMX.

- MCU filter selector is extended with an optional specific AI filter to remove the devices that do not have enough memory. If enabled, STM32 devices without Arm® Cortex®-M4, -M7, or -M33 core are directly filtered out.
- Provides a complete AI UI configuration wizard allowing the upload of multiple DL models. Includes a validation process of the generated C code on the desktop PC and on the target.
- Extends the IDE project generator to assist the generation of the optimized STM32 NN library and its integration for the selected STM32 Arm® Cortex®-M core and IDE.
- Optional add-on applications allow the generation of a complete and ready-to-use AI test application project including the generated NN libraries. The user must just have imported it inside the favorite IDE to generate the firmware image and program it. No additional code or modification is requested from the end user.
- Generation using STM32Cube.AI runtime or TensorFlow™ Lite for Microcontrollers runtime when the Neural Network file is a TensorFlow™ Lite file [7].

The plan is that optimized C-code may be obtained and loaded into some ST microcontroller. By this way one can achieve neural network realization on ST micro controller.

But it is not an end of the story. Once one has a code one has a chance to improve it.

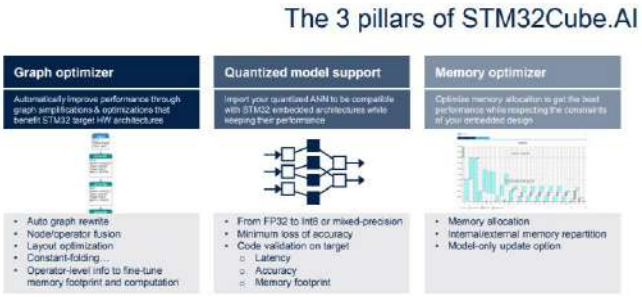

Fig. 4. More advantages.

Usually, the ST utilities are well documented and X-Cube AI is not an exception. There is step by step documentation [7], that starts from installing the X-Cube – AI, considering an idea of neural network, taking the data from the open source and implementing it on F410 board (not H747). Among actions, in a process of completing the project, the AI part announced that there is not enough memory to store even optimized NN parameters into. And in order to fix the issue one can attach USB flesh memory module. Quite a situation.

More, there was an interesting workshop about X-Cube-AI utilization. Again, it covers the NN building from scratch to its installing and optimization and further check on practice [8, 9].

Among projects, one project is Fast Downsampling MobileNet Food Recogninion on STM32H747 Discovery board. Its facilities were:

A. Neural Network

- FD-MobileNet topology from public paper.
- Mixed dataset Food-101, FoodNet, ST.

B. Implementation

- Exploits Camera in continuous mode 5.5 fps or one shot.
- 18 food classes.
- Pre-processing: rescaling from 640x480 to 224x224 RGB 8 bit image.

C. The results obtained are: STM32 Cube.AI NN

- Memory footprint: 205 KB RAM, 191 KB Flash.

D. Performance on STM32H747

- 1 inference per image.
- STM32H747 400 MHz Cortex-M7F.
- Mix model Fix/Floating Point.
- 60 MHz / 150 ms per inference.
- Accuracy: 78.8% (vs 77.7% in float).

This accuracy seems to be not flawless but quite useful for purposes of recognition.

Also, the workshop announced FP-AI sensing support through practical example (Fig. 5) [10].

FP-AI-SENSING1 is an STM32Cube function pack featuring examples that let you connect your IoT node to a smartphone via BLE and use a suitable Android™ or iOS™ application, like the STBLESensor app, to configure the device. The package enables advanced applications such as human activity recognition or audio scene classification, on the basis of outputs generated by neural networks (NN). The NN are implemented by a multi-network library supporting both floating and fixed point arithmetics, generated by the X-CUBE-AI extension for STM32CubeMX tool. The NN provided in this package are just examples of what can be achieved by combining the output of X-CUBE-AI with connectivity and sensing components from ST.

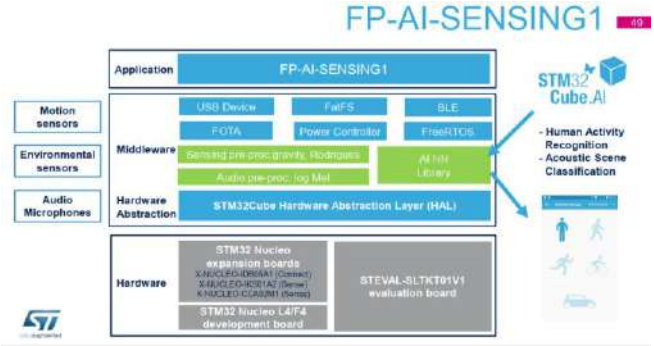

Fig. 5. FP-AI Sensing.

The package comes with an AI utility for data logging and annotation on SD card. You can record the data from the sensors and define which classes or events to record. With the recorded annotated data, you can train your own neural network on your PC/GPU/cloud, get the model, use X-CUBE-AI extension for STM32CubeMX tool for conversion, and then run it on the STM32 platform.

This package, together with the suggested combination of STM32 and ST devices, can be used to develop specific wearable AI applications, industrial predictive maintenance applications, smart things and building applications in general, where ultra-low power consumption is a key requirement.

The software runs on the STM32 microcontroller and includes all the necessary drivers for the STM32 Nucleo development board and expansion boards, as well as for the STEVAL-STLKT01V1 and STEVAL-MKSBOX1V1 evaluation boards and the B-L475E-IOT01A STM32L4 Discovery kit IoT node.

The paper materials span all the stages of NN model creation: collection of data, its preprocessing, model creation in Keras, selecting parameters of the model, data preparation for training, model creation in Python, policies of splitting the dataset onto training validation and exam parts, analyzing the model obtained. It is during evaluation of the model. Some optimization of the model can be involved.

Its Features:

- Complete firmware to develop an IoT node with BLE connectivity, digital microphone, environmental and motion sensors, and perform real-time monitoring of sensors and audio data.
- Middleware library generated thanks to STM32CubeMX extension called X-CUBE-AI, featuring example implementation of neural networks for realtime human activity recognition (HAR) and acoustic scene classification (ASC) applications.
- Multi-network support: concurrent execution of several neural networks.
- AI utility for data logging and annotation on SD card or QSPI Flash memory.
- Ultra-low power implementation based on the use of an RTOS.

- Compatible with STBLESensor application for Android/iOS, to perform sensor data reading, audio and motion algorithm feature demo, and firmware update over the air (full and partial FOTA).
- Easy portability across different MCU families, thanks to STM32Cube.
- Free, user-friendly license terms.

IV. Conclusion

So, it is practically possible to implement a neural network into a project on a not very powerful microprocessor, which has built-in support for using an already trained pre-trained neural network. Optimization of the parameters of such a network, implemented in the component, is very important.

Impress by the support for multiple "neural blocs", the adjustment of multiple parameters for training, the evaluation of the model and its optimization after training, both in a general sense and to improve compatibility with the microprocessor system.

It is not entirely clear whether additional training of the neural network is implemented during operation in the microprocessor system, or maybe this is too much?

And there is one more tool of ST. Automated ML software for end-to-end Edge AI solution design on STM32. But it will be to need another research.

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Development of a Clustered Flying Sensor Network Collection Model

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***Abstract*—With the increasing interest in unmanned aerial vehicles and wireless sensor networks, there is a growing need to enhance methods for information gathering in flying sensor networks. This article focuses on the development of a collection model for a flying sensor network, with an emphasis on the impact of clustering on its functionality. Tasks encompass the exploration of existing collection models in wireless and flying sensor networks, an analysis of the clustering influence on flying sensors, the development and adequacy verification of a new collection model, and simulation modeling for result validation. This research aims to open new avenues for improving unmanned and wireless technology systems, ensuring reliable and efficient data collection in diverse conditions.**

Keywords—flying sensor networks, clustering impact, collection model development, adequacy verification, simulation modeling.

I. INTRODUCTION

In the realm of wireless communication and networking, understanding the roles of FFD (Full Function Device) and RFD (Reduced Function Device) is paramount. FFDs, equipped with versatile capabilities, perform crucial functions such as coordination, routing, and end-device operations. On the other hand, RFDs, designed for more specific and streamlined tasks, operate with reduced functionality. This article delves into the dynamics of these two device types, exploring their roles and significance in wireless networks. Additionally, we will examine two fundamental topologies: the star topology, characterized by a central hub facilitating communication, and the peer-to-peer topology (Fig. 1), where devices communicate directly with one another, fostering decentralized and redundant structures. By unraveling the intricacies of FFDs, RFDs, and these topologies, we aim to provide valuable insights into the foundations of wireless networking, offering a comprehensive understanding that can inform the design and optimization of wireless communication systems.

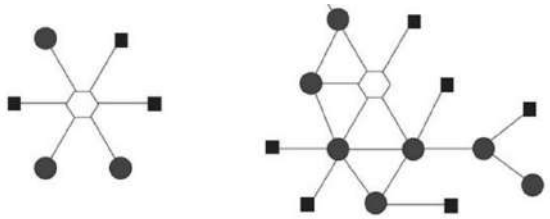

Fig. 1. Star and the peer-to-peer topology of WSN.

In the landscape of wireless networks, the utilization of clustering (Fig. 2) introduces a strategic approach to address uneven consumption patterns. By employing a clustering technique, the concept of a "sink" becomes instrumental in mitigating the irregularities in resource usage within the network. A sink, in this context, serves as a centralized point that efficiently manages and balances the distribution of resources among the various clusters. This article explores the role of clustering, particularly focusing on how strategically placing sinks aids in reducing consumption disparities.

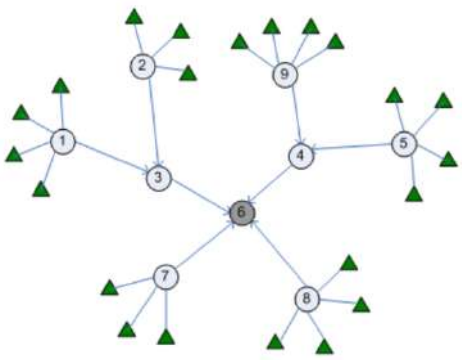

Fig. 2. Wireless sensor networks with flow.

The utilization of sinks as centralized entities enhances network efficiency, minimizes energy imbalances, and contributes to the overall optimization of resource utilization in wireless environments.

II. Flying Sensor Network

A Flying Sensor Network (FSN) is a type of mobile sensor network that involves the use of autonomous flying vehicles equipped with sensors for data collection and communication. These flying vehicles can be drones, unmanned aerial vehicles (UAVs), or any other type of aerial platform capable of carrying sensors and communication equipment.

FSNs are designed to operate autonomously, meaning they can navigate and perform tasks without human intervention. This autonomy allows them to adapt to changing environments and conditions. Flying vehicles in the network are equipped with various sensors to collect data from the environment. These sensors can include cameras, thermal imaging devices, environmental sensors, and other specialized sensors depending on the application. FSN nodes communicate with each other and with a central control system. Communication is crucial for coordination, data sharing, and decision-making. Wireless communication technologies such as Wi-Fi, Bluetooth, or specialized communication protocols are often used. FSNs leverage the collaborative capabilities of multiple flying vehicles. By working together, they can cover larger areas, collect more comprehensive data, and provide redundancy in case of failures. FSNs can be deployed to monitor environmental conditions, such as air quality, temperature, and pollution levels. In the event of natural disasters or emergencies, FSNs can be used for rapid assessment and search-and-rescue operations. FSNs can monitor crop health, assess soil conditions, and optimize farming practices. FSNs can be employed for surveillance in critical areas, border control, and security monitoring. FSNs often incorporate energy-efficient technologies to extend flight times and maximize the coverage area. This can include efficient propulsion systems, lightweight materials, and optimized energy management.

The integration of aerial platforms not only augments mobility but also plays a pivotal role in enhancing coverage and data accuracy [1]. In the context of emergency scenarios, optimal control strategies for telecommunication aeroplatforms become paramount [2]. The hierarchical deep reinforcement learning techniques tailored for data collection in Wireless Sensor Networks (WSNs) utilizing multiple Unmanned Aerial Vehicles (UAVs) [3]. A crucial aspect in addressing the challenge of power consumption in WSN nodes is the development of a model aimed at reducing energy usage in embedded control systems [4]. By establishing dynamic airborne communication networks, this research pioneers an innovative approach to surmount the limitations of static WSNs, especially in challenging terrains or disaster-stricken areas [5]. The amalgamation of intelligent aeroplatforms and inventive methodologies underscores a dynamic and interdisciplinary approach to confronting the challenges and elevating the capabilities of wireless sensor networks [6-7]. Within the realm of WSNs, the efficient aggregation of data stands out as a critical facet, directly influencing the network's overall performance, energy consumption, and data accuracy [8]. In the realm of Wireless Sensor Networks (WSNs), the utilization of Unmanned Aerial Vehicles (UAVs) introduces a dynamic dimension to data collection strategies [9]. The design of Flying Sensor Networks (FSNs) is a critical undertaking, and at its core lies the functional scheme that delineates the architecture [10]. In the realm of ubiquitous sensor networking, the adoption of a Software-Defined Architecture for Flying Sensor Networks (FSNs) marks a significant paradigm shift [11]. The localization of ground targets stands as a pivotal challenge in the domain of surveillance [12]. By examining the principles that govern these networks [13], our research aims to contribute insights that advance the understanding and optimization of Flying Ad-Hoc Networks in diverse scenarios, from aerial surveillance to disaster response. Efficient data collection is a cornerstone in the realm of Wireless Sensor Networks (WSNs) [14]. Creating a robust testbench is integral to the development and validation of Wireless Sensor Networks (WSNs) utilizing the CC2530 transceiver [15]. Analyzing the power consumption of nodes within Wireless Sensor Networks (WSNs) is a pivotal endeavor for optimizing energy efficiency [16]. By scrutinizing these consumption dynamics, seeks to contribute valuable insights into strategies for reducing power consumption, prolonging node lifetimes, and ultimately enhancing the sustainability and performance of Wireless Sensor Networks.

A typical clustered FSN system is shown in (Fig. 3) [17].

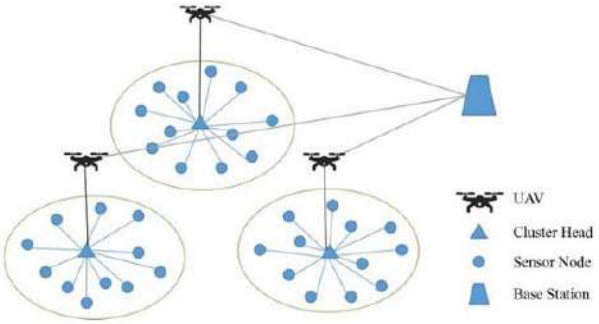

Fig. 3. FSN data colection.

III. Reconfigurable Network and Data Collection Model

Different methods of energy balancing are used to equalize the power consumption of all network nodes. Software methods include the use of routing protocols based on the residual energy metric of nodes or virtual coordinates, alternating long-distance and short-distance transmission, positioning nodes, and clustering. It is known that the routing protocols of traditional networks use metrics aimed at increasing the bandwidth of the network or reducing the delays of the transmitted data. Similar metrics can be the number of intermediate nodes (hops) to the addressee, bandwidth of the communication channel, line load level. In sensor networks, the residual energy metric of nodes on the downstream path is often used. In this case, the one with the nodes having or greater residual energy is selected from the set of alternative routes. The use of mobility of individual network components is considered a promising method of balancing. In a number of analyzed works, it is shown that potentially mobility can provide the greatest advantage in terms of increasing the duration of autonomous operation of the network. Therefore, this approach was taken as a basis in this work.

In our study, with the aim of increasing the connectivity of "problematic" areas of the ground, it is proposed networks

to use the UAV network, which acts as a backbone network to ensure the connectivity of remote unconnected areas of ground nodes. In this case, each LSM UAV node is equipped with two sets of receiving and transmitting equipment and antenna systems (for communication with ground subscribers and for communication between UAVs), a network processor (router), a buffer storage device, a GPS navigator. We will distinguish 4 levels of functionality of UAV repeaters:

- UAV - gateway;
- UAV – router;
- UAV - bridge;
- UAV - switch.

A. Model of the Flying Sensor Network

With direct data collection, the UAV flies up for monitoring from each node. -The UAV flies around the sensor field along the calculated route and collects data from each sensor node, which stores the monitoring data of the given territory for a certain time. In fact, the transmission route consists of one UAV node relay. The data is then transmitted from the UAV to the data collection point. Advantages of this method: minimal delay in data transmission during one retransmission. Disadvantages are high power consumption. In indirect data collection, the flying segment can collect data from drains. Advantages of this method: High energy efficiency. Disadvantages: Lower collection speed. Taking into account the balancing itself when choosing a drain, this method is more relevant for the topic of the work, since there is clustering of the network.

Based on the proposed approaches, our Flying Sensor Network model implements:

- Packet transmission of information messages.
- Retransmission of packets through intermediate nodes.
- Organization of multiple access of subscribers to the network.
- Determination of routes for the transmission of information over the network.
- Organization of channels along the selected route.
- Topology management (location).

B. A reconfigured Network Model

The model of the reconfigured network and data collection is shown in the form of a graph of the network (Fig. 4) configuration in the form of a 4x4 grid, flow transitions are possible only horizontally and vertically between neighboring vertices.

As we know, with a large number of sensors, it is advisable to use a cluster organization of ground users to increase the life cycle.

Sensors connected to a network can monitor environmental parameters: movement, light, temperature, pressure, humidity. Monitoring can be carried out over a large area, because the sensors transmit information in a chain from neighbor to neighbor and then to the UAV. The basic idea is to divide the collection field into a grid to find the optimal mobile flow (Fig. 5) according to the legend of the UAV.

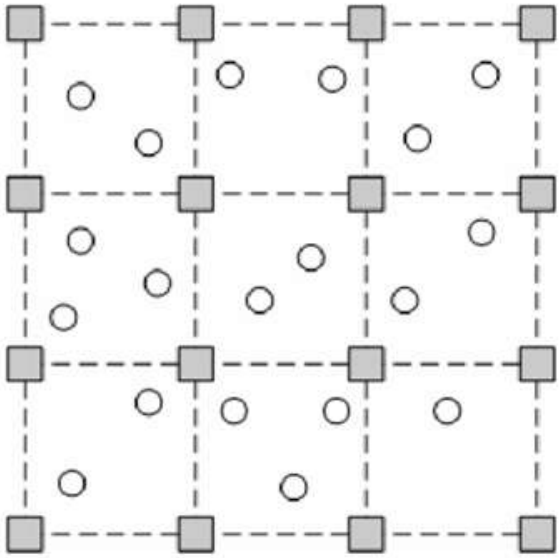

Fig. 4. Reconfigurable network.

Overall, the concept of mobile flow is a fundamental aspect of designing and developing FSN.

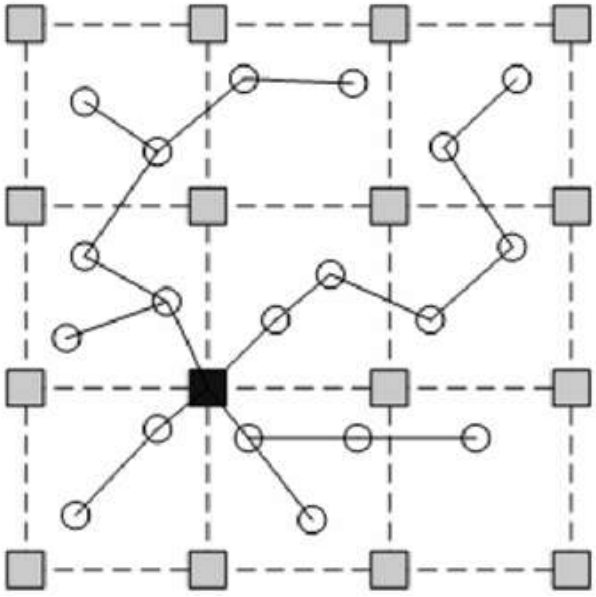

Fig. 5. Data collection model with mobile flow.

IV. Modeling and Verification

Modeling and verification of the adequacy of the model was carried out taking into account the dependence of the life time of the repeaters on the number of connected cluster nodes and power in standby mode.

Dependence (Fig. 5) showing the limits of application of the model proposed in this paper. It can be seen from the graph that with a large value of the idle mode, close to the consumption during transmission or reception, the life time does not depend on the number of connected devices.

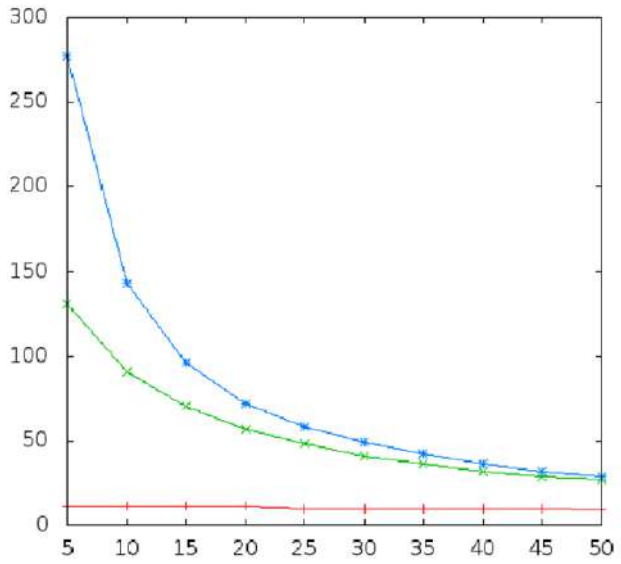

Fig. 6. Reconfigurable network and data collection model.

At the same time, with small values, it is possible to reconfigure the network in such a way as to increase its lifetime. In Fig.5 Y – days, X is the number of connected nodes. Which fully shows the adequacy of the proposed model. Simulation models of flying sensor networks (FSN) open wide opportunities for research and optimization of these technologies without resorting to physical tests in a real environment. In summary, modeling and verification are indispensable processes for ensuring the effectiveness, reliability, and optimal performance of Flying Sensor Networks. They provide a systematic approach to design, test, and refine FSNs, ultimately contributing to their successful deployment in a variety of applications.

V. Conclusion

In conclusion, this study provides a comprehensive overview of flying sensor networks (FSNs), elucidating the intricacies of their structure and functionality. The research specifically delves into the impact of clustering on FSNs, conducting a thorough analysis to unveil its implications. A novel data collection model was meticulously developed, considering the intricacies of clustering in FSNs. The adequacy of the proposed model was rigorously checked, and the study culminated with simulation modeling, offering practical insights into the real-world applicability and performance of clustered FSNs. This multifaceted approach contributes to a deeper understanding of FSNs and their optimization, paving the way for advancements in aerial sensor network technologies.

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Development of a Model for Determining the Coordinates of Clustered Flying Sensor Network Nodes

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***Abstract*—This research explores the fundamental capability of determining the coordinates of individual objects within a network, presenting a compelling case for the attractiveness of such systems. The potential to determine coordinates becomes a key advantage, leading to cost reduction and diminished energy consumption of individual devices, notably by eliminating the need for GPS sensors. Additionally, the deployment of these networks is simplified, envisioning scenarios such as aerial dispersion of devices from aircraft. The adaptability of these sensor networks in challenging terrains further underscores their appeal. Although coordinate determination is integral to various wireless telecommunication networks, including cellular networks, the unique characteristics of each network necessitate distinct approaches to coordinate resolution, even when based on common principles such as geometric triangulation. Therefore, the task of determining coordinates for nodes in a clustered flying sensor network remains pertinent. The study discusses the contemporary relevance and significance of this challenge, emphasizing its potential to enhance the efficiency and applicability of wireless sensor networks, particularly in scenarios where conventional methods face limitations.**

Keywords—flying sensor networks, coordinate determination, clustered networks, energy-efficient devices, deployment optimization.

I. INTRODUCTION

In the ever-evolving landscape of wireless sensor networks, the integration of airborne sensors has emerged as a transformative paradigm, introducing unprecedented mobility, coverage, and data accuracy. Within this realm, the concept of Clustered Flying Sensor Networks (CFSNs) has gained considerable attention, promising enhanced efficiency and adaptability. One of the pivotal challenges in harnessing the full potential of CFSNs lies in the precise determination of the coordinates of individual nodes within the clustered architecture.

Traditional methods often rely on GPS sensors for geolocation, but the inherent limitations and associated costs have spurred a quest for alternative strategies. This article embarks on the exploration and development of a robust model specifically tailored for determining the coordinates of nodes in Clustered Flying Sensor Networks. By delving into the intricacies of coordinate determination within a clustered context, the research aims to contribute not only to the theoretical advancements in wireless sensor networks but also to the practical optimization of these networks for diverse applications.

As we delve into the intricacies of this model development, we unravel the complexities and nuances involved in achieving precise geolocation within a clustered airborne sensor network. The potential implications of such advancements are vast, ranging from cost-effective deployment strategies to increased energy efficiency in individual devices. This research seeks to bridge the gap between theoretical considerations and practical implementation, fostering a deeper understanding of the challenges and opportunities in the realm of clustered flying sensor networks.

On the other hand, RFDs, designed for more specific and streamlined tasks, operate with reduced functionality. This article delves into the dynamics of these two device types, exploring their roles and significance in wireless networks. Additionally, we will examine two fundamental topologies: the star topology, characterized by a central hub facilitating communication, and the peer-to-peer topology (Fig. 1), where devices communicate directly with one another, fostering decentralized and redundant structures. By unraveling the intricacies of FFDs, RFDs, and these topologies, we aim to provide valuable insights into the foundations of wireless networking, offering a comprehensive understanding that can inform the design and optimization of wireless communication systems.

In recent days, wireless sensor networks (WSN) are catching the spotlights in networking and other emerging fields like large data communication, artificial intelligence, automation systems etc [1]. Clustering, a machine learning

technique, is an effective way to extend the lifecycle and reduce power consumption of wireless sensor networks [2]. In paper [3] descibed novel framework to realize efficient data collection from wireless sensor networks, where an unmanned aerial vehicle (UAV) is dispatched to collect the aggregated data from cluster heads and an unmanned ground vehicle carrying backup batteries moves along with the UAV to compensate for the shortage of UAV energy. The combination of a large number of nodes into a network, the requirements for minimizing the energy consumption of nodes and the network as a whole lead to the need for additional structural solutions when creating wireless sensor networks. The most important of these is network clustering, which also implies constant rotation of the cluster head node during the network life cycle [4]. Possible also optimise of structure the node for reducing energy consumption [5]. Test mockups or testbenches [6] can be used to study real networks [7]. Wireless sensor networks can effectively reduce complexity, weight, and costs of aerospace onboard communication systems [8]. However, it is necessary to optimize these networks in order to extend their autonomous lifetime[9] with power consumption [10].

Typically, the sensor network is important not only to detect or measure the value of an event parameter of interest, but also to correlate it to a specific point in space. As the location of sensors on the ground can be random in nature, there is a question of finding the coordinates of all nodes [11]. The possible idea is to expand the set of localizable nodes starting from the set of anchor nodes cluster by cluster rather than node by node [12]. Thus, the main tasks of the research can be reduced to:

- Perform a survey of flying sensor networks.
- Determine the structure of the flying sensor network.
- Consider the issue of network clustering.
- To develop the determination of the coordinates of the nodes of the clustered flying sensor network.
- Check the adequacy of the model.

Thus, the task of determining the coordinates of nodes for a clustered flying sensor network is relevant.

II. Methods of Determining Coordinates

The main methods of determining coordinates include:

- Trilateration method (Fig.1).
- Multilateration method (Fig.2).
- Triangulation method (Fig.3).

Trilateration relies on distance measurements from three or more known points to determine the coordinates of an unknown point. It is commonly used in wireless communication and indoor positioning systems, often utilizing signal strength or time-of-flight measurements.

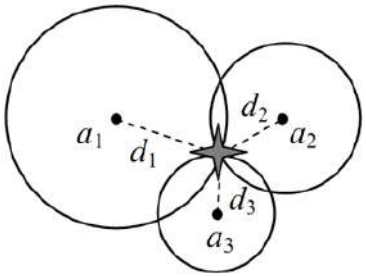

Fig. 1. Trilateration method.

Similar to trilateration, multilateration determines position by measuring the time difference of arrival (TDOA) or phase difference of signals from multiple known locations. This method is often used in radar systems and air traffic control. (Fig. 2).

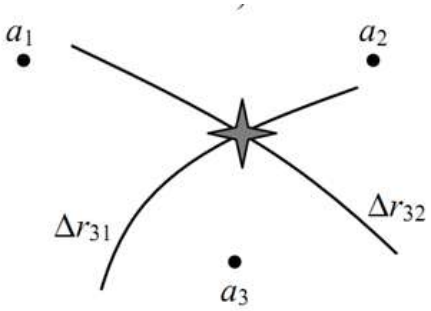

Fig. 2. Multilateration method.

Triangulation method involves measuring the angles between a known baseline and the lines to the target from two or more points. By using trigonometry, the coordinates of the target can be determined. Triangulation is commonly used in surveying and navigation.

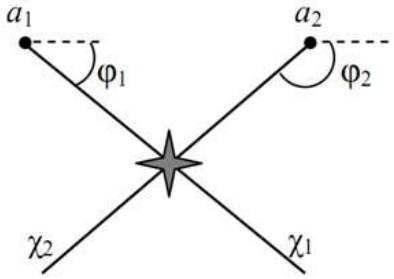

Fig. 3. Triangulation method.

The choice of method depends on the specific application, environmental conditions [13-18], and the level of accuracy required for the task at hand.

III. Symmetrical Double-Sided Two Way Ranging

A Flying Symmetric two-way ranging (SDS-TWR) [14] is a ranging method that uses two delays that naturally occur during signal transmission to determine the range between two nodes: repeaters (Fig.4):

- Signal propagation delay between two wireless devices.

- Confirmation processing delay in the wireless device.

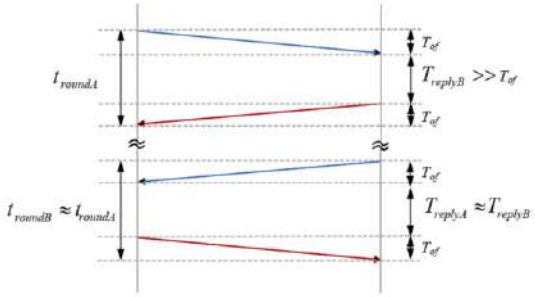

Fig. 4. SDS-TWR.

This method is called symmetric bilateral because: It is symmetric because the measurement from station A to station B is a mirror image of the measurement from station B to station A (ABA to BAB). It is two-way because only two stations are used to measure the range, station A and station B. It is two-way because it uses a data packet (called a test packet) and an ACK packet. Conditions for using the method. The absence of strict requirements for synchronization (characteristic of TOF and TDOA) with high accuracy of state estimation between nodes (much higher than that of RSSI) allows considering this method as the main method of radio ranging in the development of a method of spatial positioning.

IV. Proposed Model

To account for the lack of responses from nodes in our model, we propose introducing a specific function, referred to as a penalty function, to calculate the computation costs of estimates. This function should lead to an increase in the value of the minimized expression for those points, denoted as "I," situated in the vicinity of antenna locations through which signals from nodes were not received.

V. Conclusion

In this article, we explored a model for determining coordinates in clustered flying sensor networks. The proposed model incorporates a penalty function to account for nodes that do not provide responses, thereby enhancing the accuracy and efficiency of coordinate determination. Simulation results affirm the model's effectiveness in real-world scenarios. The introduction of the penalty function proves to be a promising approach for optimizing computations within network nodes, especially in locations where signal reception was challenging.

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