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Edge-Processing Architecture for Enhanced Noise Immunity in Optical Airspace Monitoring Systems

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Abstract— Alongside radar systems, optical and thermal imaging sensors play a vital role in local airspace surveillance. However, visual monitoring is highly susceptible to environmental interference (clouds, precipitation, sensor noise). Transmitting raw, noisy video feeds to central servers consumes immense bandwidth and reduces system reliability. This paper explores an edge-computing architecture combining FPGAs and microcontrollers to enhance the visual noise immunity of optical monitoring nodes. By performing spatial filtering and background subtraction directly on the FPGA at the sensor level, only relevant target coordinates are transmitted by the MCU. This approach drastically reduces network load and improves the overall resilience of the airspace surveillance network.

Keywords— Optical surveillance, visual noise reduction, FPGA, edge computing, computer vision, interference immunity.

I. Introduction

Comprehensive airspace monitoring requires multi-spectral approaches, combining RF tracking with optical and infrared cameras to detect targets like UAVs or non-transmitting aircraft. A major limitation of optical systems is their sensitivity to environmental interference—such as fog, heavy rain, or glare—which acts as visual noise.

Sending raw, uncompressed video streams from remote subscriber nodes to a central server for processing requires high-bandwidth connections, which are prone to failure. To improve the overall stability and interference immunity of the system, data must be processed at the edge. FPGAs, with their capability to perform operations on thousands of pixels simultaneously, are perfectly suited for this pre-processing task alongside a managing MCU.

II. Problem Statement

The objective is to design a visual processing node that maximizes optical interference immunity while minimizing the data payload sent over the network. We must:

- Define the roles of the FPGA and MCU in a video-processing pipeline;
- Identify techniques for hardware-accelerated visual noise reduction;
- Evaluate the reduction in network bandwidth requirements compared to centralized processing.

III. Video Processing Techniques in FPGAs

To clean the optical signal and detect targets, the FPGA implements a dedicated computer vision pipeline in hardware:

1. Spatial Filtering: The FPGA applies matrix convolution (e.g., Gaussian or Median filters) to every incoming frame in real-time. This eliminates random sensor noise and artifacts caused by precipitation.

2. Background Subtraction: The FPGA maintains a reference frame of the empty sky. By comparing incoming frames to this reference, it isolates moving objects (targets) and ignores static visual clutter (clouds).

3. Data Reduction: Once a target is isolated, the FPGA calculates its bounding box coordinates. The MCU reads only these lightweight coordinate matrices rather than the full video frame.

Furthermore, this edge-processing architecture ensures high adaptability to varying weather conditions and ambient lighting. Since the visual noise profile of heavy precipitation differs drastically from that of low-light sensor artifacts, the MCU can dynamically reconfigure the FPGA fabric with specific spatial filters optimized for the current environment. Additionally, as more efficient background subtraction models or advanced computer vision algorithms are developed, updated configuration bitstreams can be deployed to the remote nodes via secure over-the-air (OTA) updates. This inherent flexibility significantly extends the operational lifespan and adaptability of the deployed optical monitoring nodes without necessitating costly physical hardware replacements at remote installation sites.

IV. Comparative Evaluation

TABLE I. Evaluation Matrix

Criterion	Centralized Processing (Raw Video Transmission)	Edge Processing (FPGA + MCU Node)
Network Bandwidth Required	> 20 Mbps per camera	< 0.1 Mbps (Telemetry only)
Latency to Detection	High (Network dependent)	Ultra-low (On-sensor processing)
Immunity to Weather Noise	Handled remotely (risks data loss)	Handled locally (High immunity)
Power Consumption at Node	Moderate (Camera + Transmitter)	Slightly Higher (Includes FPGA processing)

The comparison highlights that moving the visual filtering to the edge via an FPGA drastically reduces network dependency. Even if the communication channel is degraded by electronic warfare or poor connectivity, the MCU can still transmit tiny packets containing critical target coordinates, thereby maintaining high system-level interference immunity.

V. Case Study: Remote UAV Detection Node

A theoretical model of a remote UAV tracking camera was analyzed. The node utilizes a high-definition image sensor feeding directly into a Xilinx Spartan-7 FPGA, managed by a standard 32-bit MCU.

During a simulated scenario involving light rain (visual noise), a traditional MCU-based system would attempt to compress the noisy video, resulting in heavy artifacting and dropped frames over a 4G/LoRa link. In the proposed FPGA-accelerated node, the FPGA applies a median filter to remove the rain noise and isolates the moving UAV. The MCU then receives a simple data string: *Timestamp, Target ID, X: 1024, Y: 768, Confidence: 95%.* This tiny payload is easily transmitted over a low-bandwidth, highly encrypted radio link, ensuring uninterrupted airspace surveillance regardless of visual or network interference.

VI. Conclusions

The application of FPGA-based edge computing to optical airspace surveillance nodes introduces a fundamental paradigm shift in how visual noise and environmental interference are managed. This study demonstrates that relying on centralized servers to process raw, uncompressed video streams from remote subscriber systems is highly inefficient and vulnerable to network degradation. By deploying a hybrid hardware-software architecture at the sensor level, the proposed system successfully isolates the heavy computational workload of image processing from the communication channel, ensuring continuous operation even under constrained bandwidth conditions.

The integration of a Field-Programmable Gate Array (FPGA) alongside a managing microcontroller (MCU) provides an optimal balance between parallel processing power and system-level control. The FPGA efficiently executes mathematical pixel-level operations—such as spatial filtering to eliminate weather-induced visual artifacts and dynamic background subtraction—in real time. Consequently, the visual noise immunity of the node is significantly enhanced, as environmental interference is filtered out at the source. The MCU is thereby relieved of impossible video-compression tasks, allowing it to focus exclusively on packaging and transmitting lightweight, highly encrypted target coordinates (telemetry) over the network.

Ultimately, this decentralized approach drastically reduces the dependency on high-bandwidth data links, making the surveillance network far more resilient to both electronic warfare and adverse weather conditions. The inherent reconfigurability of the FPGA fabric also ensures that edge nodes remain scalable; they can be updated over-the-air with advanced computer vision algorithms without necessitating hardware replacements. Future research will explore the implementation of lightweight Convolutional Neural Networks (CNNs) directly onto the FPGA fabric to enable autonomous target classification (e.g., distinguishing UAVs from biological targets) while maintaining the strict power constraints of remote, battery-operated surveillance deployments.

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