DOI: 10.35598/mcfpga.2026.021

Reliability assessment of AMD FPGA Artix 7

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***Abstract*—The work evaluates the reliability of AMD FPGA Artix 7. It is shown that the mean time between failures of FPGA Artix 7 XC7A100T with FITs=2 is more than a thousand years, which is diagnosed by built-in crystal monitoring tools. According to the reliability characteristics, FPGA Artix 7 can be used to develop critical devices.**

Keywords— FPGA, Artix 7, AMD, reliability, evaluation, stress tests , service life, mean time between failures

I. Introduction

AMD product reliability meets industry requirements through world-class methodologies and advanced technologies AMD products are rigorously evaluated to meet customer lifespan and performance expectations. AMD uses accelerated load and lifespan simulation to ensuring reliable operation.

Typical AMD's reliability stress tests include, but are not limited to:

- high temperature durability test;
- test of previous preparation;
- temperature cycling test;
- high-acceleration load test;
- temperature and humidity shift;
- storage at high temperatures;
- mechanical shocks and vibrations;
- electrostatic discharge;
- hanging;
- soft error rate estimation;
- reliability characteristics at board levels.

Based on this, AMD is constantly improving its own products, methods and means of testing. Today, AMD answers the highest standards set in this industry.

When designing devices on field programmed gate array circuits (FPGAs), it is important to know the reliability parameters of the chip and the mean time between failures.

II. The Main Part

Reliability is defined as the conformity of a product's performance to specifications over time in response to a variety of (applied) environmental stress conditions. The objective of a reliability measurement program is to achieve continuous improvement in the robustness of each product evaluated.

This program periodically measures the reliability of the finished product to ensure that performance meets or exceeds regulatory reliability specifications. Reliability programs are run in conjunction with AMD's internal programs.

Reliability qualification of new devices, board manufacturing processes and enclosures is designed to ensure that AMD products meet reliability requirements before being released into production. Reliability stress tests are conducted according to the conditions specified in the JEDEC Solid State Reliability Test Methods State Technology Association for packaged devices, JESD22, etc.

The board manufacturing process reliability monitoring program is based on board manufacturing process maturity, device operating hours, and failure in time (FIT) rate.

FIT factor calculations are based on approximately one million hours of device operation (at TJ = 125°C) before failure.

The AMD SEU Estimator (SEU) is designed to estimate the reliability characteristics and service life of products based on specified die parameters and usage conditions. The calculator estimates the failure interval (FIT) for different usage conditions and durations.

The main parameters of the SEU tool include:

- dividing the microcircuit into small components according to their characteristics and applications;

- calculation of the failure rate of each component using an aging model;
- taking into account the reliability physics for the gate material oxide, transistor and connections, and:
    - design characteristics (voltage, current, area, complexity);
    - failure physics: wear data;
    - parametric drift data from CAD simulations, softened by a test guard band.

When assessing the failure rate of modern FPGAs with programmable logic, it should be noted that manufacturers provide this rate in units of FITs (Failure per Interval of Time), which actually corresponds to one failure per 10^9 device hours. For example, expecting five failures when operating one million FPGAs for a thousand hours corresponds to a failure rate of 5 FITs. The following is a method for calculating the failure rate [1]:

$$Failure\ \ Rete = \frac{x^2 \cdot 10^9}{2(No.\ of\ \ Deviese)(No.\ of\ \ Hours)} \quad (1)$$

where: x^2 is the chi-square value at the desired level of confidence and $(2f+2)$ are degrees of freedom, and f is the number of refusals.

The acceleration factor A is calculated using the expression:

$$A = \exp\left\{\frac{E_a}{k}\cdot\left(\frac{1}{T_{J1}} - \frac{1}{T_{J2}}\right)\right\}, \quad (2)$$

where: $E_a$is the thermal activation energy (assuming 0.7 eV is used in the failure rate calculation, except for EPROM, which uses 0.58 eV); A is the acceleration factor; $k$is the Boltzmann constant, 8.617164 x 10^{-6} eV/K; $T_{J1}$is the transition temperature in Kelvin $(K = C + 273.16)$; T_{J2} is the voltage transition temperature in Kelvin $(K = C + 273.16)$.

Summary of Artix 7 failure rates is given in Table 1 [2].

TABLE I. EXPERIMENTAL BEAM TESTING AND REAL-TIME SOFT ERROR RATES FOR CRAM

Tech Node	Product Family	LANSCE Neutron Cross-Section per Bit		FIT/Mb (Thermal Neutrons)		FIT/Mb (Alpha Particle)		FIT/Mb (Real-Time Soft Error Rate Per Event)	
		CRAM	Error	CRAM	Error	CRAM	Error	CRAM	Error

All measurements were made by the manufacturer at room temperature and with typical supply voltages.

The Artix 7 XC7A100T-1CSG324C FPGA has a failure rate of (FITs) – 2 at 9,117,988 device hours.

With round-the-clock operation of the crystal, this is 379,916 days of operation (or 54,274 weeks, or 1,043 years) in the presence of 2 failures, which are diagnosed by the built-in crystal control means.

In general, the reliability of the crystal will be limited by the reliability of other elements on the board that provide power, frequency stabilization, etc.

III. CONCLUSIONS

When using FPGAs in the development of devices for critical or military applications, it is necessary to take into account the reliability characteristics of the device as a whole and of each element individually.

The Artix 7 FPGA crystal has built-in self-monitoring tools. Such monitoring is aimed at assessing operability before starting operation. Since built-in monitoring and diagnostic tools are usually more effective than other tools, such an assessment is completely sufficient from the point of view of FPGA integration into a specific system.

According to the analysis carried out in the FPGA Artix 7 XC7A100T with FITs=2, the mean time between failures is more than a thousand years, which is diagnosed by the built-in crystal monitoring tools.

The analysis shows that the reliability indicators of the Artix 7 XC7A100T FPGA meet all the requirements for the development of critical devices.

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// Перспективні напрямки сучасної електроніки, інформаційних і комп'ютерних систем (MEICS-2019): 27-29 листопада 2019 р., м. Дніпро. – Дніпро, Дніпровський національний університет імені Олеся Гончара, Кременчук: ПП Щербатих О. В., 2019. – С. 94-95.

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