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Adaptive Hardware-Software Architecture for Interference Mitigation in Airspace Surveillance Networks

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Abstract— This paper proposes a hybrid FPGA-MCU architecture designed to improve the interference immunity of subscriber systems in airspace surveillance networks. Modern airspace monitoring relies heavily on continuous radio communication, which is increasingly vulnerable to both intentional jamming and unintentional electromagnetic noise. The proposed edge-computing node utilizes a Field-Programmable Gate Array (FPGA) for real-time digital signal processing (DSP) and adaptive filtering, while a low-power microcontroller (MCU) handles high-level decision-making and network routing. Experimental concepts show that delegating heavy mathematical filtering to the FPGA significantly enhances signal-to-noise ratios without overloading the MCU, ensuring stable data transmission in hostile environments.

Keywords— FPGA, microcontroller, interference mitigation, airspace surveillance, adaptive filtering, edge computing.

I. Introduction

Airspace surveillance systems are fundamental to modern aviation safety and security. These networks consist of numerous subscriber nodes that transmit telemetry, location data, and status reports. However, the radio frequency (RF) spectrum is becoming increasingly crowded, leading to a higher risk of signal degradation due to weather conditions, cross-talk, and active electronic interference. Improving the interference immunity of these nodes is a critical priority.

Traditional nodes relying solely on general-purpose microcontrollers often lack the computational bandwidth required to perform complex noise-filtering algorithms in real time. FPGAs present an ideal solution by offering parallel processing capabilities perfectly suited for digital signal processing, provided they are integrated efficiently with control-oriented MCUs.

II. Problem Statement

The primary challenge is designing a surveillance node capable of dynamically suppressing RF interference without introducing unacceptable latency or requiring excessive power. Specifically, this paper aims to:

- Outline the architectural division of labor between the FPGA and MCU;
- Describe mechanisms for real-time adaptive noise filtering;
- Compare the proposed hybrid architecture's filtering throughput against traditional MCU-only systems;

III. Hardware-Software Mitigation Techniques

To achieve high interference immunity, the system employs a two-stage processing pipeline:

1. High-Speed Data Path (FPGA): The FPGA receives raw digital data from the Analog-to-Digital Converter (ADC). It implements parallel Finite Impulse Response (FIR) filters and Fast Fourier Transform (FFT) blocks to isolate the target signal from background noise.

2. Control and Adaptation Path (MCU): The MCU monitors the quality of the filtered signal. If the MCU detects a new jamming pattern or shifting noise frequencies, it calculates new filter coefficients and dynamically updates the FPGA configuration, allowing the system to adapt to changing electromagnetic environments on the fly.

Furthermore, this dual-path approach ensures that the system remains highly scalable. As new interference profiles or jamming patterns are identified, updated filter coefficient libraries can be deployed to the MCU via secure over-the-air (OTA) updates. The MCU can then apply these updates to the FPGA fabric dynamically, without requiring a complete system reboot. This flexibility significantly extends the operational lifespan and adaptability of the deployed edge nodes in rapidly evolving electromagnetic environments.

IV. Comparative Evaluation

TABLE I. Evaluation Matrix

Criterion	MCU-Only Node (ARM	Hybrid Node (MCU + Low-

	Cortex-M4)	Power FPGA)
Real-Time FFT Capability	Low (Sequential processing)	High (Parallel processing)
Filter Adaptation Latency	~45 ms	~2 ms
Throughput under Heavy Noise	0.5 Mbps	8.0 Mbps
System Complexity	Low	High
Interference Immunity Level	Basic (Static filters only)	Advanced (Dynamic coefficient updates)

This table illustrates the performance gap between a standard MCU approach and the proposed hybrid model. While the MCU struggles to maintain throughput under heavy noise due to processing bottlenecks, the FPGA handles the high-frequency data streams effortlessly, resulting in significantly lower adaptation latency and superior interference immunity.

V. Adaptive ADS-B Receiver Node

To demonstrate the concept, an architecture was modeled based on an ADS-B (Automatic Dependent Surveillance-Broadcast) receiver node operating in an urban environment with high RF interference. The system utilizes a lightweight FPGA (e.g., Lattice iCE40) paired with an STM32 MCU.

During normal operation, the FPGA applies a standard band-pass filter. When the system is subjected to simulated wideband interference, the MCU detects a drop in message integrity. Within milliseconds, the MCU calculates targeted notch-filter coefficients and pushes them to the FPGA. The FPGA immediately suppresses the interfering frequencies, restoring the ADS-B signal reception. This dynamic response prevents data loss and maintains continuous tracking of airspace targets.

VI. Conclusions

The integration of Field-Programmable Gate Arrays (FPGAs) into the edge-computing subscriber nodes of airspace surveillance networks represents a significant advancement in achieving robust interference immunity. This study has demonstrated that traditional, single-processor architectures relying solely on general-purpose microcontrollers are inherently bottlenecked when subjected to intense radio frequency (RF) interference or intentional electronic jamming. By implementing a hybrid hardware-software co-design, where mathematically intensive digital signal processing (DSP) tasks—such as real-time parallel Fast Fourier Transforms (FFT) and Finite Impulse Response (FIR) filtering—are offloaded to the programmable logic fabric, the system achieves deterministic, ultra-low latency filtering that remains completely independent of the main application workload.

Furthermore, the synergy between the FPGA's high-throughput parallel data path and the microcontroller's flexible control path enables a truly adaptive defensive mechanism. Instead of relying on static filter configurations that can be easily bypassed by dynamic or wideband jamming patterns, the proposed architecture allows the microcontroller to actively monitor signal integrity metrics and compute optimal filter coefficients on the fly. Pushing these updated coefficients into the FPGA fabric within milliseconds ensures that the communication and tracking capabilities of airspace surveillance subscribers remain operational even in highly volatile and hostile electromagnetic environments, effectively mitigating data loss.

Finally, the architectural scalability inherent in this approach provides a future-proof solution for remote and autonomous deployments. Because the filtering mechanisms are implemented in reconfigurable logic, the edge nodes can be updated over-the-air to counter newly emerging electronic threats without requiring physical hardware modifications. Future research directions will focus on optimizing the power consumption of this hybrid model during maximum-throughput scenarios and exploring the integration of lightweight, hardware-accelerated machine learning algorithms within the FPGA fabric to predict and preemptively suppress complex interference patterns before they can degrade system performance.

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