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An Experimental Platform for Digital Communication Based on SDR and FPGA (ZedBoard + AD9361)

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Abstract – This paper describes the design and development of a low-cost, reconfigurable experimental platform for physical-layer research in software-defined radio. The system is built around the Xilinx ZedBoard (Zynq-7020 SoC) and an FMC-LPC SDR module based on the AD9361 transceiver. The primary objectives include the implementation and evaluation of modulation schemes (BPSK, QPSK, QAM), convolutional coding with Trellis-based Viterbi decoding, and bit-error-rate (BER) performance under additive white Gaussian noise and interference. Key hardware considerations — power supply limitations, clock quality, and clone board risks — are discussed, along with a structured software workflow using Vivado 2018.2 and the Analog Devices HDL reference design. The proposed architecture partitions heavy signal processing into the FPGA fabric, while the ARM core handles only monitoring, control, and statistical output. The platform supports both cable-based laboratory measurements and over-the-air experiments in the 868 MHz ISM band, offering a scalable foundation for future research on advanced coding and modulation techniques.

Keywords – SDR, ZedBoard, AD9361, FPGA, Zynq-7020, physical layer, modulation, Viterbi decoder, Trellis coding, BER measurement, FPGA DSP, Vivado HLS

I. Introduction

The growing complexity of modern wireless communication systems demands flexible and cost-effective testbeds that can bridge the gap between theoretical signal processing algorithms and practical radio-frequency implementation. Commercial test equipment, while highly accurate, is often prohibitively expensive and lacks the reconfigurability required for rapid prototyping of novel physical-layer techniques. An alternative approach is to build a dedicated software-defined radio (SDR) platform using a combination of a powerful system-on-chip (SoC) and a wideband transceiver. Such a platform can serve as a self-contained laboratory for investigating modulation, coding, synchronisation, and channel impairments.

In this work, we propose a practical implementation of an SDR testbed based on the Xilinx ZedBoard (Zynq-7020) and the Analog Devices AD9361 transceiver in an FMC-LPC form factor. The ZedBoard provides a balanced mix of programmable logic (Artix-7 FPGA) and a dual-core ARM Cortex-A9 processor, while the AD9361 covers a frequency range of 70 MHz to 6 GHz with bandwidth up to 56 MHz. This combination is well-supported by open-source reference designs, making it an attractive choice for academic and industrial research laboratories.

The main goals of the project are threefold: (i) to implement and test common modulation schemes (BPSK, QPSK, and higher-order QAM) in real hardware; (ii) to develop a convolutional encoder and a Trellis-based Viterbi decoder, starting with hard-decision and progressing to soft-decision algorithms for improved coding gain; and (iii) to perform systematic BER measurements under controlled AWGN and interference conditions. The system is designed to operate in two modes — a cable-connected laboratory mode with precision attenuators for repeatable SNR control, and an over-the-air mode using ISM bands for real-world propagation studies.

This paper is organised as follows. Section 2 describes the hardware platform, with a focus on critical selection criteria and potential pitfalls. Section 3 presents the experimental architecture and the trade-offs between cable and over-the-air configurations. Section 4 details the software environment, the SoC partitioning strategy, and the phased development plan. Section 5 highlights the key risks and open questions that require careful consideration during implementation. Finally, Section 6 concludes the paper and outlines the immediate next steps.

II. Hardware Platform and Selection Criteria

2.1. The ZedBoard as the Core Processor

The ZedBoard, developed by Avnet and Digilent in partnership with Xilinx, is built around the Zynq-7020 SoC (XC7Z020-1CLG484C). This device integrates a processing system (PS) with a dual-core ARM Cortex-A9 running at up to 667 MHz, and a programmable logic (PL) based on the Artix-7 FPGA fabric, containing approximately 85,000 logic cells, 220 DSP slices, and 4.9 Mb of block RAM. The board offers 512 MB of DDR3 memory, a rich set of peripherals (Gigabit Ethernet, USB, HDMI, audio codec, and multiple Pmod connectors), and, most importantly, an FMC LPC (Low Pin Count) connector with 68 user-defined I/O lines. This connector serves as the primary interface for the SDR

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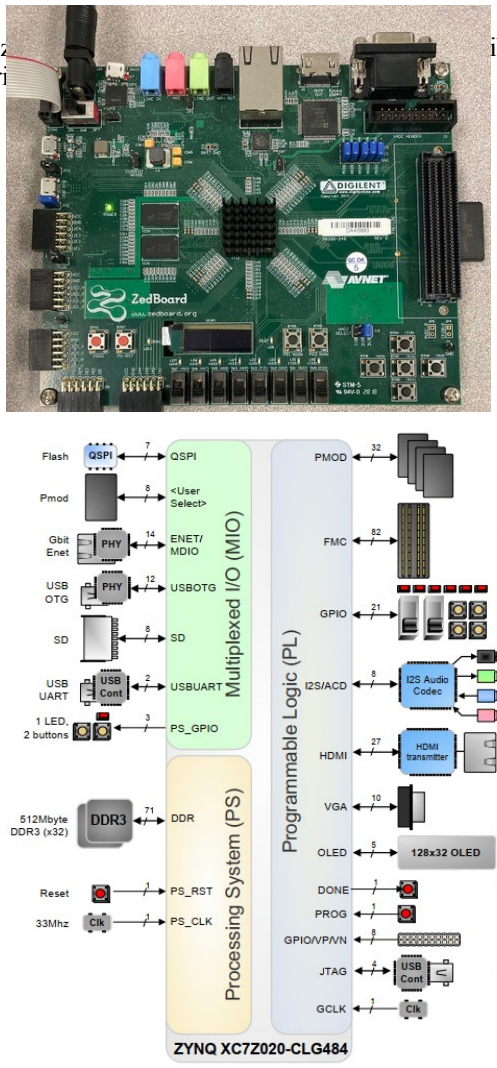

Fig. 2. Architecture of the ZedBoard.

2.2. Choosing the SDR Transceiver Module

The FMC LPC connector imposes a significant constraint: it provides fewer high-speed serial lines than the FMC HPC (High Pin Count) variant. Consequently, transceivers that rely on JESD204B interfaces, such as the AD9371, are not directly compatible without complex and unreliable adapter boards. For the ZedBoard, two realistic options are available:

- AD9361 — a widely used, mature transceiver covering 70 MHz to 6 GHz with analogue bandwidth up to 56 MHz. It features a parallel CMOS/LVDS digital interface that is fully supported by the reference design (FMCOMMS2) provided by Analog Devices. This is the recommended choice for maximum flexibility and performance.
- AD9363 — a lower-cost derivative with a reduced frequency range (325 MHz to 3.8 GHz, though software-extendable) and a maximum bandwidth of 20 MHz. It is pin-compatible with the AD9361 and shares the same digital interface, making it a viable budget alternative for experiments that do not require the full 56 MHz bandwidth.

Given the project's focus on high-order modulation and coding, the AD9361 is preferred if the budget allows. However, the AD9363 may still be sufficient for initial investigations at lower symbol rates.

2.3. Critical Hardware Considerations

When sourcing the SDR module, especially from secondary markets (e.g., AliExpress), several physical-layer vulnerabilities must be addressed:

- Power supply — The FMC LPC connector on the ZedBoard is rated for approximately 1 A at 3.3 V and 0.5 A at 12 V. Many clone boards, however, draw 1.2–1.5 A during full-power transmission. To avoid overloading the board or causing instability, it is essential to select a module that includes a separate external power input (typically a 5–6 V barrel jack) and to power the SFR front-end independently from an external power supply.
- Clock source — The frequency accuracy and phase noise of the reference clock directly affect carrier stability and, consequently, the achievable BER. Cheap quartz oscillators found on low-cost clones introduce significant frequency drift. A high-stability TCXO (temperature-compensated crystal oscillator) at 40 MHz or 38.4 MHz is strongly recommended to ensure reliable demodulation and synchronisation.
- Clone quality — Many inexpensive modules mislabel the chip (AD9363 instead of AD9361), omit ESD protection on the RF ports, or deviate from the standard FMC pinout. Such deviations can lead to non-functional designs or permanent damage. Therefore, procurement must require verified schematics and explicit confirmation of compatibility with the FMCOMMS2 reference design for the ZedBoard.
- By carefully addressing these hardware risks, the platform can achieve the robustness required for reproducible scientific measurements.

III. Experimental Architecture and Operational Modes

The testbed is designed to support two distinct measurement configurations, each serving a different purpose in the research workflow.

3.1. Cable-Based Laboratory Mode

In this mode, the signal path is entirely conducted: the ZedBoard's transmitter output is connected via a high-quality SMA cable to a set of precision attenuators, and then to a spectrum analyser (or, in a future iteration, to a second SDR receiver). The attenuators allow precise control of the signal-to-noise ratio (SNR) by introducing calibrated losses. This configuration offers excellent repeatability, immunity to

multipath fading, and direct access to the transmitted spectrum. It is particularly suitable for measuring modulation accuracy (error vector magnitude), spectral masks, and the baseline BER performance of the coding schemes under controlled AWGN.

The only significant limitation is the upper frequency of the available spectrum analyser, which in our laboratory is 2 GHz. Therefore, all cable-based experiments must be conducted at carrier frequencies below 2 GHz, e.g., in the 868 MHz ISM band, which is also the preferred choice for over-the-air tests.

3.2. Over-the-Air (OTA) Mode

For real-world propagation studies, the testbed can be configured with antennas on both ends — a transmitting antenna connected to the ZedBoard and a receiving antenna connected either to a second SDR receiver or, for preliminary checks, to the same spectrum analyser (which can only measure power, not demodulate). The OTA mode introduces effects such as multipath, fading, Doppler shift, and interference from other devices, making it essential for evaluating the robustness of the coding and modulation schemes in realistic environments.

To operate legally without a license, the system is restricted to the ISM bands: 433 MHz, 868 MHz, and 2.4 GHz. The 868 MHz band is recommended for the initial phase because it lies within the analyser's range, antennas are readily available, and interference levels are generally lower than at 2.4 GHz. Future work may extend to 2.4 GHz if a suitable receiver or a rented 6 GHz analyser becomes available.

IV. Software Environment and Development Roadmap

4.1. Toolchain and Reference Design

To ensure reproducibility and minimise integration effort, the software development is based on Xilinx Vivado 2018.2 and the hdl_2018_r2 branch of the Analog Devices HDL repository. This combination is documented as the "golden" reference for the FMCOMMS2/3 boards and has been extensively tested by the community. Although newer versions of Vivado exist, they introduce additional compatibility issues that would prolong the debugging phase; hence, we strictly adhere to the specified version and a fixed commit hash.

The reference design provides all the necessary IP cores for interfacing with the AD9361, including the SPI configuration controller, the data interface (LVDS or CMOS), and the DMA engine for data transfer to/from DDR memory. We build upon this foundation and gradually replace or augment it with custom processing blocks.

4.2. System Partitioning: PL vs. PS

A key architectural decision concerns the division of labour between the programmable logic (FPGA) and the processing system (ARM). The AXI interconnect between the two domains has limited bandwidth — streaming raw I/Q samples at 56 MHz (with 16-bit resolution) would require over 1 Gbps, which is near the practical limit of the AXI buses. To avoid congestion and maintain deterministic timing, all computationally intensive DSP tasks are implemented in the FPGA fabric. These tasks include:

- Modulation and pulse shaping (e.g., raised-cosine filtering);
- Carrier and symbol synchronisation (using NCOs and CORDIC);
- Convolutional encoding and Viterbi decoding (both hard- and soft-decision);
- BER counting and statistical aggregation.

The ARM core, running in a bare-metal (No-OS) environment to guarantee latency predictability, is responsible only for high-level control: configuring the AD9361 registers, initiating transmission/reception, reading the final bit streams and BER counters, and sending results to a host via UART or Ethernet. This partitioning avoids the bottleneck of moving raw I/Q data to the Linux kernel and back, which would be impractical for real-time operation.

For initial debugging, we may temporarily use the IIO Oscilloscope via DMA to visualise the constellation and spectrum, but this is not intended for the production system.

4.3. Phased Development Plan

The implementation follows a stepwise integration strategy, with each phase building on the previous one:

1. Environment setup – Install Vivado 2018.2, clone the ADI HDL repository with the fixed commit, and synthesise the base fmcomms2/zed reference project. Verify basic functionality by testing the onboard LEDs and buttons.
2. Analog loopback – Generate a continuous sine wave using the built-in NCO, route it through the DAC, connect the TX output to the RX input via an external SMA cable (with attenuators), and capture the signal back through the ADC. Verify the received spectrum on the analyser and ensure correct amplitude and frequency.
3. Digital loopback – Implement an internal loopback within the FPGA, bypassing the RF front-end, to validate the digital interface to the AD9361 (including the data formatting and clocking).
4. Custom modulator IP – Develop a BPSK/QPSK modulator using Vivado HLS (C/C++ to RTL) and integrate it into the transmit path, replacing the default test pattern generator.
5. Coding and decoding – Add a convolutional encoder (Trellis) and a Viterbi decoder. Start with a hard-decision decoder for simplicity, then upgrade to a soft-decision decoder to obtain approximately 2 –3 dB coding gain.
6. BER measurement – Implement an automated BER counter that compares the transmitted and received bit sequences. Vary the SNR using the external attenuators and record BER curves for different modulation and coding configurations.
7. Host integration – Connect the ARM core to the BER counter and send the statistics via UART (or

Ethernet) to a host computer for plotting and analysis.

This incremental approach allows early detection of hardware and software issues, reducing the overall development risk.

V. Critical Issues and Open Questions

Before proceeding with the full implementation, the following points require careful consideration and team consensus.

Frequency plan — While both 433 MHz and 868 MHz are legal ISM bands, we recommend 868 MHz for the OTA experiments. It offers better antenna efficiency (quarter-wave monopole of about 8.6 cm) and typically has lower interference from consumer devices compared to 2.4 GHz. The frequency is also within the 2-GHz analyser limit.

Topology for BER measurements — A spectrum analyser can only measure power spectral density, not bit errors. To obtain BER over the air, a true receiver is needed. The options are: (a) a second ZedBoard with an identical SFR module; (b) a cheaper SDR dongle (e.g., RTL-SDR) that can be used with GNU Radio, but which may not support our custom modulation at higher symbol rates; or (c) using the same ZedBoard in a half-duplex mode with an RF switch, which limits the system to time-division experiments. For the initial phase, we can rely on the cable-based mode (with a spectrum analyser) for BER curves, since the SNR is precisely controlled. The OTA BER measurements are deferred to a later stage, when a second receiver board can be acquired.

Viterbi decoder implementation — Existing open-source Viterbi decoders (e.g., from OpenCores) are often written in Verilog/VHDL but may require substantial adaptation to fit the Zynq's clocking and interface conventions. An alternative is to implement the decoder directly in Vivado HLS, which allows rapid prototyping and automatic pipelining. The HLS approach also simplifies parameterisation for different constraint lengths and coding rates. We suggest starting with a custom HLS design to maintain full control over the architecture.

Procurement and budget — The success of the hardware phase depends on sourcing a reliable SDR module with the required specifications (separate power input, TCXO, correct FMC pinout). A budget must be allocated for high-quality SMA cables (e.g., RG316), a set of precision attenuators (1 dB and 10 dB steps), suitable antennas, and possibly an external TCXO upgrade. The timeline for the first milestone (analog loopback) is estimated at two weeks, with full BER characterisation requiring approximately one additional month.

VI. Points to discuss

1. Frequency Plan: Do we agree on 868 MHz over 433 MHz for the OTA tests? (868 MHz provides better antenna form factors and generally lower local interference).
2. System Topology: Should we invest in a dual-board setup (two ZedBoards for true Tx/Rx) to measure BER over the air, or is a single Tx board paired with a spectrum analyzer/RTL-SDR sufficient for the first milestone? (Note: Analyzers cannot measure BER, only spectral purity).
3. Viterbi Implementation: Open-source Verilog/VHDL implementations (e.g., from OpenCores) often require significant refactoring for Zynq. Should we allocate time to write a custom Viterbi decoder directly in HLS to ensure seamless integration?
4. Timeline and Budget: Can we realistically achieve the Analog/Digital Loopback and basic BPSK milestone within one month? What is the approved budget for high-quality SMA cables (RG316), precision attenuators (1 dB / 10 dB steps), and verified SDR modules?

It seems we can choose among the options:

- Option A: Analog Cable Loopback (Laboratory Mode). The signal path is ZedBoard (Tx) → SMA cable → precision attenuators → Spectrum Analyzer (≤ 2 GHz). Advantages: High repeatability and exact SNR control, making it ideal for foundational BER measurements. Limitation: Restricted to frequencies below 2 GHz due to analyzer constraints.
- Option B: Over-The-Air (OTA) ISM Band. Utilizing license-free ISM bands (433 MHz or 868 MHz). While 2.4 GHz is technically possible, it exceeds our 2 GHz analyzer limit, requiring additional RTL-SDR receivers or expensive 6 GHz analyzer rentals.
- Recommendation: We strongly suggest focusing on the 868 MHz band for the OTA phase, as it offers a superior compromise between antenna size, propagation characteristics, and environmental interference.

CONCLUSIONS

We have presented a comprehensive design for an experimental SDR testbed based on the ZedBoard and the AD9361 transceiver. The platform addresses the need for a flexible, repeatable, and cost-effective environment for physical-layer research, covering modulation, coding, and BER evaluation. By carefully selecting the hardware — with particular attention to power delivery, clock quality, and clone board authenticity — and by following a structured development plan that leverages Vivado 2018.2 and the ADI reference design, the system can achieve reliable and accurate measurements.

The proposed SoC partitioning, which places all heavy DSP in the FPGA and reserves the ARM core for control and monitoring, ensures deterministic real-time performance and avoids the bandwidth bottleneck of the AXI bus. The stepwise integration from analog loopback to full BER characterisation provides a clear roadmap that mitigates technical risks.

The immediate next step is to procure the SDR module, antennas, and accessories, followed by the installation of the development tools and the synthesis of the base reference

project. Once the hardware is validated, we will proceed with the custom IP development and subsequent coding and decoding stages. We anticipate that this platform will not only serve the current project objectives but also provide a reusable foundation for future investigations into advanced techniques such as adaptive modulation, MIMO, and machine-learning-aided equalisation.

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